A Fully-Integrated Wireless Bondwire Accelerometer With Closed-loop Readout Architecture

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***Abstract*—This paper presents a fully-integrated wireless bondwire accelerometer using a closed-loop readout interface that effectively reduces the noise from electrical circuits and long-term frequency drifts. The proposed accelerometer was fabricated using 0.18-μm CMOS technology without micro electromechanical systems (MEMS) processing. To reduce manufacturing errors, the bondwire inertial sensors are wire-bonded on the chip pads, thereby enabling a precisely-defined length and space between sensing bondwires. The proposed wireless accelerometer using a pair of 15.2 μm and 25.4 μm bondwires achieves a linear transducer gain of 33 mV/g, bandwidth of 5 kHz, a noise floor of 700 $\mu g/\sqrt{\text{Hz}}$, and 4.5 μg bias stability. The acceleration data is digitalized by an energy-efficient 10-bit SAR ADC and then wirelessly transmitted in real time to the external reader by a low-power on-off shift keying (OOK) transmitter. The proposed architecture consumes 9 mW and the chip area is 2 mm $\times$ 2.4 mm.**

***Index Terms*—Bondwire, CMOS, inertial sensing, resonant accelerometer, wireless accelerometer.**

I. Introduction

MEMS accelerometers have enjoyed translational success in a wide range of applications, such as infrastructure monitoring, automotive systems, wearable healthcare devices, and customer electronics for gaming and mobiles. Most inertial sensors rely on changes in material characteristics or mechanical structures to detect force and acceleration, and usually cannot be directly fabricated by a conventional CMOS process. With the advent of advanced CMOS-MEMS technologies, sensors and interface circuits can be integrated on a small silicon chip using special post-processing mechanisms. Capacitive [1], [2] and resonant [3]–[5] are the most commonly used MEMS accelerometer types that sense capacitance changes and resonant frequency deviations caused by applied acceleration, respectively. The capacitive MEMS accelerometer has been widely-used in automotive systems and consumer electronics due to its low temperature sensitivity, miniature size, and low power consumption. In comparison, the resonant accelerometer can achieve high precision, a dynamic input range, and radiation insensitivity [4]. However, both types of MEMS accelerometers suffer from low-frequency drifts, special fabrication processing, and offsets from package or interface parasitics, such as bondwires and lead capacitance [6].

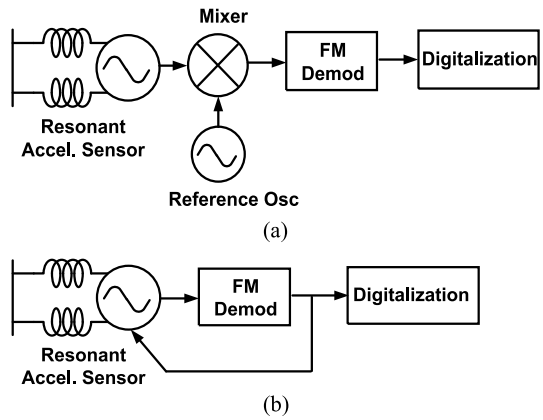

Fig. 1. (a) Receiver-based downconversion readout architecture [12]. (b) Closed-loop readout architecture.

Wirebonding technology plays an important role in IC packaging for creating either mechanical and electrical interconnections between silicon chips and packages due to its low cost, compliance with thermal and bending stress conditions, and well-developed supporting instruments [7]. Apart from being used to create interconnections, bondwires can be used as RF antennas [8], [9], magnetic coupling coils for DC-DC converters [10], and hotwire anemometers for air-flow sensing [11]. Using parallel bondwires as an inertial sensor has been proposed to avoid MEMS/IC integration and fabrication [12], [13]. A pair of gold and aluminum bondwires is employed as the sensing device that converts the acceleration-induced displacement to inductance changes. The receiver-based readout architecture with free-running oscillators suffers from frequency drifts caused by temperature and environmental variations. Consequently, the down-conversion readout architecture, shown in Fig. 1(a), requires two oscillators—one for sensing and the other one for reference generation—leading to high power consumption and potential frequency pulling between them.

In this paper, a CMOS accelerometer using 15.2 μm and 25.4 μm gold bondwire inertial sensors and a closed-loop readout interface is proposed. Fig. 1(b) illustrates the proposed readout architecture. The demodulated signal stabilizes the sensing component using a negative feedback loop, which can reduce frequency drifts as well as residual vibrations in the sensor. Furthermore, a wireless transmitter is integrated on the chip to avoid measurement inaccuracy caused by the wiring. The proposed bondwire accelerometer can resolve the following limitations listed in prior works: 1) manufacturing deviations, 2) detection

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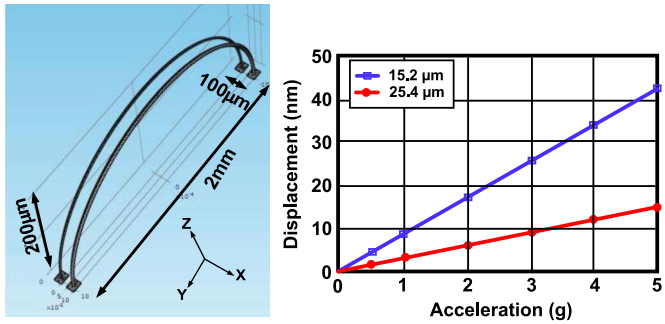


(a) (b)

Fig. 2. (a) Bondwire FEM model and (b) simulated bondwire displacements under acceleration.

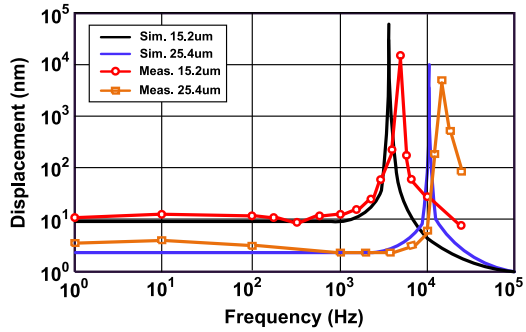


Fig. 3. Frequency response of bondwire inertial sensors (diameter = 15.2 μm and 25.4 μm).

errors from package/board stress and wire connections, 3) environment-caused frequency drifts, and 4) high power dissipation.

The remainder of this paper is organized in the following manner. Section II describes the mechanical and electrical model of a bondwire accelerometer. Section III presents the proposed readout system. Section IV presents the experimental results. Section V briefly concludes this paper.

II. Sensor Element

A. Mechanical Model of Bondwire Inertial Sensors

Wire-bonding technology has been widely used in creating interconnection between bare silicon dies to other silicon dies or to the packages. Bondwires exhibit self-inductance and mutual-inductance to neighboring wires; they also exhibit mechanical deflections while experiencing a force [14]. The displacement of a parabolic bondwire due to acceleration can be expressed as [12]

$$\frac{\Delta X}{g} = \frac{\rho R^4}{Er^2}(\pi^2 + 2\pi) \tag{1}$$

where ρ is the density of material, E is Young's modulus, R represents the radius of the bondwire arch, and r represents the inner radius of the bondwire. From (1), two bondwires with different diameters, structures, or materials, can create a relative displacement during acceleration. In contrast to prior studies that used bondwires with different materials [12], [13], we adopt sensing bondwires with different radii since the relative displacement is squarely proportional to the radius ratio between two sensing bondwires instead of linear relation to the density of materials. Fig. 2 depicts the bondwire sensor model and the simulated displacement of a pair of 2-mm-long gold bondwires with a diameter (d) of 15.2 μm and 25.4 μm at various accelerations, respectively. The transducer gain is 8.5 nm/g and 3 nm/g for the thin and thick bondwires, respectively.

B. Mechanical Resonant Frequency

Mechanical resonant frequency is where the oscillation frequency matches the natural frequency at which maximum displacements occur. For a bondwire sensor, the system bandwidth of flat gain is limited by the mechanical resonant frequency ($\omega_{\rm r}$) of the bondwire. A simple calculation of the mechanical resonant frequency of a bondwire is derived as [15]

$$\omega_r = C_n \frac{r}{l^2 \cdot 2}\sqrt{\frac{E}{\rho}} \tag{2}$$

where l is the length of wire, and C_n represents a constant related to l/h, where h is the arc height. When a ratio of l and$h$ is ten times, C_n is about 3.5 for the lateral vibration mode [15]. The mechanical resonant frequency is proportional to the radii of the bondwires and inversely proportional to the length of the bondwire. Therefore, thin bondwire has a lower mechanical resonance frequency that sets the operational bandwidth of the bondwire inertial sensor. Fig. 3 illustrates the simulated and measured frequency response of a pair of gold bondwires with diameters of 15.2 μm and 25.4 μm. The bondwire sensors are bonded on chip-to-chip pads of a silicon chip, the length and separation between which are 2 mm and 90 μm, respectively. The simulated resonant frequencies using finite element method (FEM) are 6.12 kHz and 10.3 kHz for the thin and thick bondwires, respectively. To verify the results, fabricated bondwire sensors are actuated by a piezoelectric vibrator and the displacement is measured by an in-plane vibration analyzer. The displacement is recorded by a high-speed camera. Similar results are observed. The displacement deviations are found in the measurement at resonance, mainly limited by the resolution of equipment.

C. Bondwire Inductance

The electrical properties of bondwires also depend on their geometrical shapes or materials, such as the height above the ground plane, the horizontal length, and distance between two adjacent bondwires. Since the height of the bondwire sensor is much smaller than the length of the bondwire, the bondwire can be modeled approximately as two parallel wires. For two bondwires with the same horizontal length, the self-inductance and mutual-inductance are approximately as

$$L = \frac{\mu_o l}{2\pi}\left[\ln\left(\frac{4h}{d}\cdot\frac{l+\sqrt{l^2+\frac{d^2}{4}}}{l+\sqrt{l^2+4h^2}}\right)+\sqrt{1+\frac{4h^2}{l^2}} -\sqrt{1+\frac{d^2}{4l^2}}-\frac{4h-d}{2l}\right] \tag{3}$$

$$M = \frac{\mu_o l}{2\pi}\left[\ln\left(\frac{l}{S}+\sqrt{1+\left(\frac{l}{S}\right)^2}\right)+\sqrt{1+\left(\frac{l}{S}\right)^2} -\sqrt{1+\left(\frac{S}{l}\right)^2}+\left(\frac{S}{l}\right)\right], \tag{4}$$

where $d$is the diameter, $h$is the height from the ground plane, Srepresents the separation between two wires, and l represents

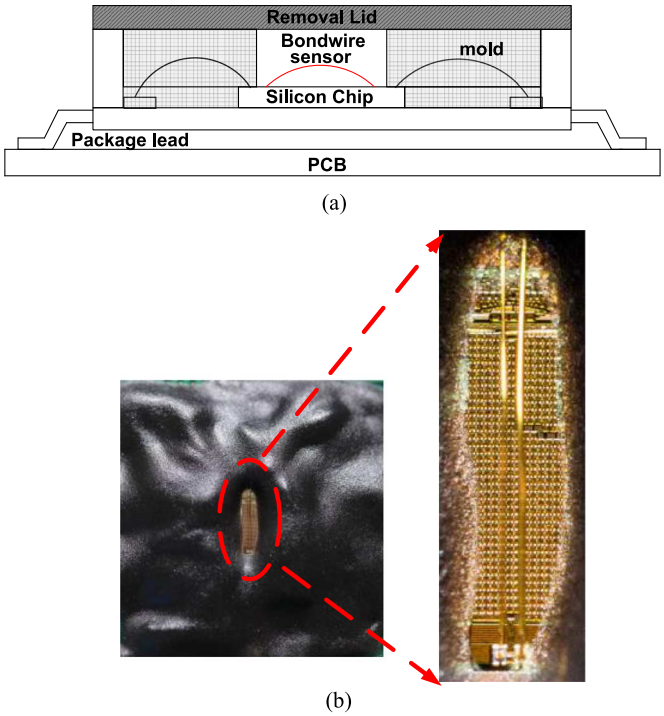


Fig. 4. (a) The plot of bondwire accelerometer packaging; (b) photograph of the molded bondwire accelerometer.

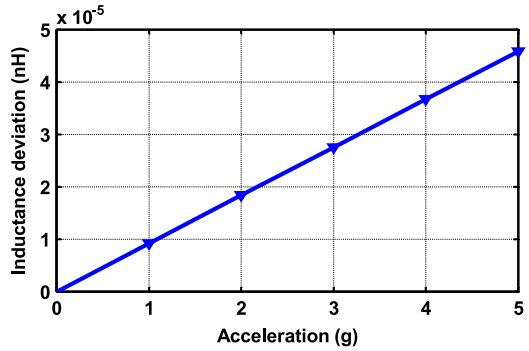


Fig. 5. Simulated inductance change versus acceleration (length = 2 mm, space = 90 μm, and height = 200 μm, center inductance = 1.1 nH).

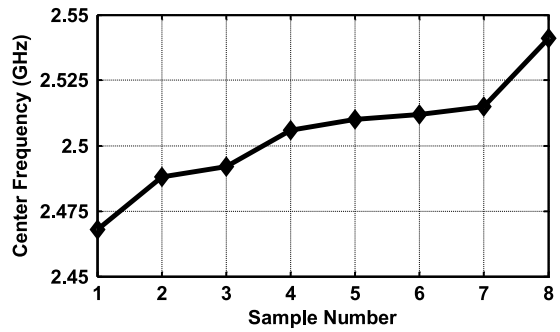


Fig. 6. Measured output frequency of eight bondwire oscillators (samples are numbered after measurement.).

the wire length. Considering the vertical connection on the pad, the vertical height variation of 150 μm of a bondwire only contributes 2% inductance changes [16]. For a pair of bondwires with the length of 2 mm, the separation of 90 μm, and the height of 200 μm, the inductance is approximately 1.1 nH from EM simulations. Fig. 5 shows the simulated inductance changes from acceleration. The inductance changes about 0.9×10^{-5} nH from 1.1 nH at 1-g acceleration, corresponding to 10 kHz/g conversion gain while the center frequency is 2.4 GHz.

A design summary is briefly concluded. Long bondwires can achieve large mechanical displacement, but lower resonant frequency that limits the operational bandwidth. In addition, the long bondwire has large self-inductance and mutual inductance. Although a long bondwire achieves large displacement and inductance changes during acceleration, the ratio between mutual inductance changes from accelerations and total inductance does not increase linearly as the length increases [13]. Therefore, a pair of bondwires with a length of 2 mm is chosen in this design for area efficiency (on-chip bonding), sufficient acceleration-induced inductance gain ($\sim$400 ppm/g) and bandwidth ($>$5 kHz).

D. Sensor Packaging

To reduce manufacturing deviations, the bondwire sensors are bonded on chip pads to chip pads, where the length and separation between two wires are precisely defined. Fig. 4(a) depicts the plot of proposed packaging for bondwire sensor. To protect the sensor from damages, the bondwires—except the sensing bondwire in the center—are molded. The partial encapsulation method and setup are shown in [17]. The silicon chip is encapsulated in a firm IC package that isolates external pollution, dust, and humidity. The removal lid is used for observing the bondwire sensor in the experiments. Fig. 4(b) presents photographs of the encapsulated bondwire sensors. The bondwire sensor was tested on a vertical shaker with 3-g acceleration at the mechanical resonant frequency of thin bondwires for 72 hours. There was no damage on the bondwire sensors in our experiments. In addition, modern wirebonding technology has been demonstrated to tolerate $>$1000 g acceleration in a high shock environment [18].

E. Variations and Reliability Analysis

To validate the process and manufacturing errors, we tested 8 chip samples. The measured output frequencies of bondwire oscillators are presented in Fig. 6. The frequency of the free-running oscillator over these 8 samples at the same bias voltage ranges from 2.467 GHz to 2.541 GHz, which is equal to 3% deviations across these samples. The frequency deviation can be calibrated back to the desired frequency using the on-chip switch capacitor bank.

III. Proposed Readout Circuitry

Fig. 7 illustrates a schematic of the proposed bondwire accelerometer. The interface circuits include a phase-locked loop (PLL), bandpass amplifier, 10-bit ADC, wireless transmitter, and low-dropout regulator. The PLL is used as the frequency demodulator, converting frequency deviations by acceleration to voltages. The voltage is filtered and amplified by the bandpass amplifier before digitalization. Thus, low-frequency drifts can be filtered out. In addition, since the frequency of the sensing oscillator follows the precise frequency (19 MHz) of the crystal oscillator, the temperature-caused frequency drifts are further eliminated by frequency tracking and correction of the PLL. The in-band noise is also suppressed by the loop. To further suppress the reference spurs and high-frequency fluctuations, the design adopts a low loop bandwidth of 10 kHz. After digitalization, the sensing data are wirelessly transmitted using the

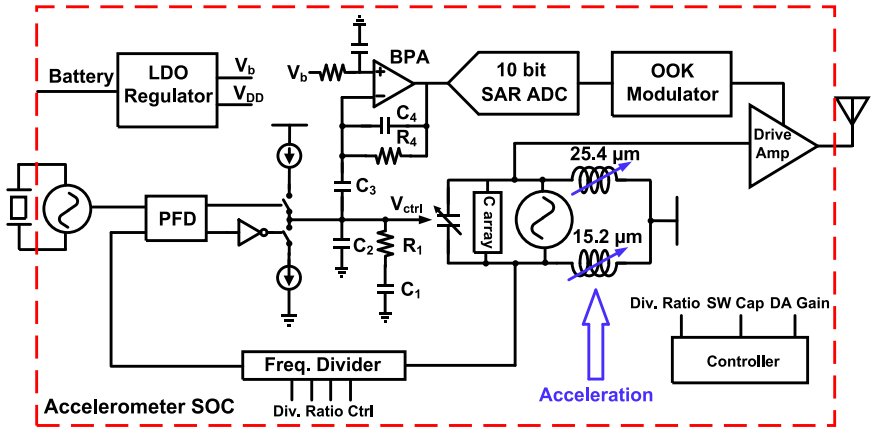


Fig. 7. Proposed readout interface circuitry for bondwire acceleration sensor.

2.4 GHz direct-conversion transmitter, which reuses hardware for the RF carrier signal generation. Therefore, the complexity and power consumption of the readout circuitry can be reduced effectively. An OOK scheme is used for data modulation and the frequency deviations from the acceleration is 110 kHz for an acceleration of 5 g. Therefore, the signal detection mask of the receiver was set at 200 kHz, which is sufficient to accommodate the frequency information for the prototype. The detailed circuit design is described below.

A. PLL-Based FM Demodulator

Compared to other FM demodulators—such as the slope detector, ratio detector, and quadrature signal detector—the PLL demodulator has the advantages of small size, low signal distortion, and low noise. The PLL demodulator comprises a phase frequency detector, charge pump, low-pass filter, oscillator, and frequency divider. The incoming FM signal is used to control the frequency of the VCO. As incoming frequency varies, the PLL generates a voltage signal to represent the frequency deviation caused by the oscillator. As the system is frequency/phase-locked, the control voltage can be used to demodulate the signal. Moreover, the PLL is designed to have a short time constant to track frequency modulation, and the locked range should be sufficiently large to allocate all the acceleration-caused frequency change. To enhance the frequency-to-voltage conversion gain, a low-gain (∼MHz/V) VCO using the smallest varactors in series with coupling capacitors is adopted in this design. The small gain factor is useful for improving the linearity of VCO and inducing lesser flicker noise from the tail current source.

B. Circuit Blocks of the PLL Demodulator

Fig. 8 illustrates the schematic of the digital phase frequency detector (PFD), which includes D flip-flop phase/frequency comparator, which is a delay cell that creates sufficient time for signal reset, and a glitch de-bounce circuitry. This circuitry helps reduce static errors and clock feedthrough in the charge pump (CP). The CP is used to transform the digital pulses at the output of the PFD to current that charges/discharges the loop filter according to the lag or lead frequency between reference clock and divide-down oscillator signals. However, the mismatches in the PMOS/NMOS switches may cause spikes at the control voltage (V_{CP}), thereby leading to high noise floor on the voltage control line. To reduce the mismatch between the up and down currents, a CP with a feedback loop

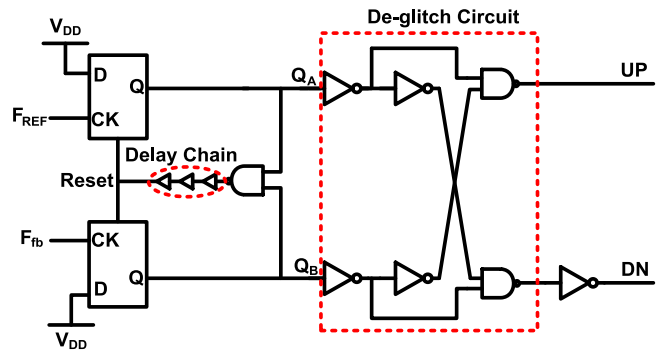


Fig. 8. Schematic of PFD.

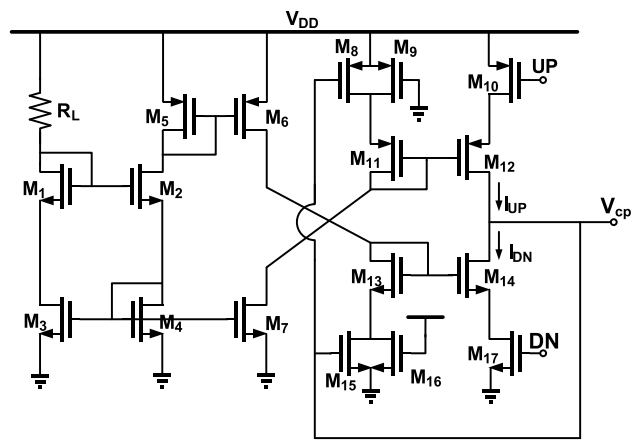


Fig. 9. Schematic of CP.

[19] is employed. Fig. 9 presents the schematic for the CP with a current balanced feedback loop. M_8 and M_{15} are added to compensate for the channel-length modulation effect of the up/down current mirrors via negative feedback. The amount of compensation is dynamically adjusted according to the CP output voltage (V_{cp}), which varies the source degeneration impedance of M_{11} and M_{13} in a reverse direction to keep the up and down currents matched in a wide voltage range. Fig. 10 depicts the simulation results of a current mismatch in the charge pump with and without feedback. The mismatching in the up and down currents is reduced considerably from 15% to 5% over the output voltage range from 0.25 V to 1.25 V.

Fig. 11 presents the schematic of the proposed voltage controlled oscillator, with PMOS differential pair and PMOS current source to reduce flicker noise. The resonant tank

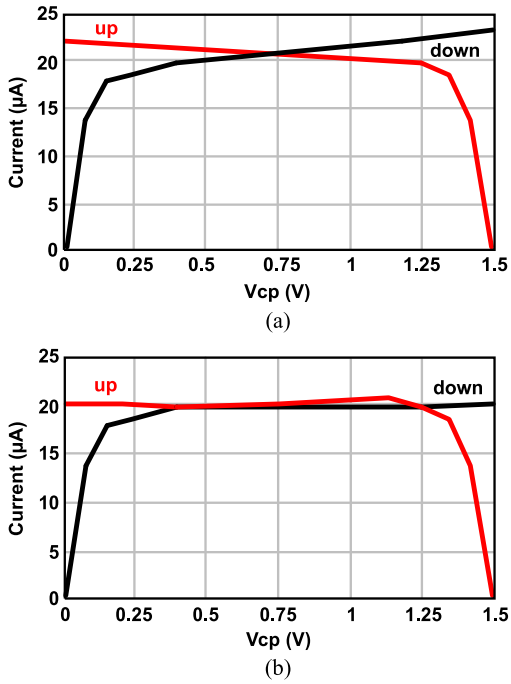


Fig. 10. Simulated Up/down current of the CP (a) without feedback; (b) with feedback.

comprises a pair of bondwires and on-chip capacitors. The bondwires are bonded from chip pads to chip pads with a 2-mm length and diameters of 15.2 μm and 25.4 μm, respectively, thereby yielding an equivalent inductance of 1.1 nH. The asymmetry in two bondwires may cause in-band noise up-conversion. From simulation, $\pm 18\%$ inductance deviations between two bondwires cause 0.7 dB and 2.3 dB phase noise degradation at 1 kHz and 1 MHz offsets, respectively. The in-band noise is suppressed by the loop and the far-away noise has less effect on the detection resolution. To improve the frequency-to-voltage conversion gain, the smallest varactor in the process with a series capacitor is used. In addition, a 6-bit bank of switching capacitors provides a tunable frequency range of 360 MHz from a central frequency of 2.4 GHz to overcome oscillation frequency deviations due to bondwire manufacturing variations. The differential outputs of oscillators drive the resistor-load buffer stage to generate an RF carrier signal for a wireless transmitter and PLL. The programmable frequency divider is implemented using high-speed true single phase clock logics and low-power static logics. The divider ratio can be programmed using the I^2C interface.

C. Bandpass Amplifier and SAR ADC

The output of the PLL-demodulator includes spurious signals in a wide frequency range, such as reference spurs (19 MHz), and oscillator signal (2.4 GHz) due to clock feedthrough and device mismatches. The acceleration signal is usually in the sub Hz to kHz range for the applications of human body motion and environmental monitoring. Therefore, a low-pass and low-noise amplifier [20] is employed to amplify the signal and filter out undesired interference. Fig. 12(a) presents a schematic of a low-power bandpass amplifier. The input of the bandpass amplifier is capacitively coupled from the voltage control line output for DC offset elimination. To achieve low cut-off frequency, a pair of reverse biased PMOS transistors $(M_{p1} - M_{p4})$

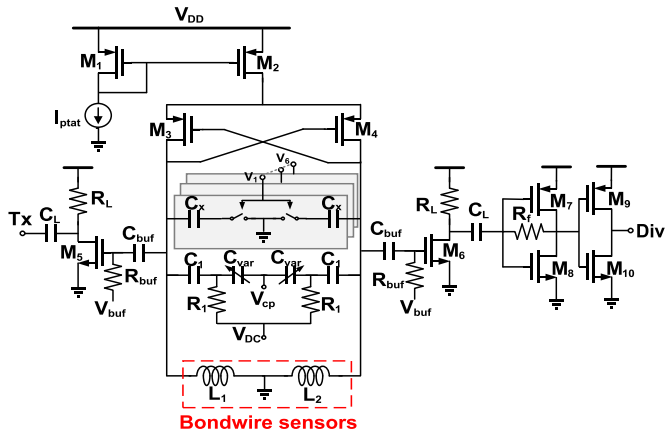


Fig. 11. Schematic of bondwire oscillator readout circuitry.

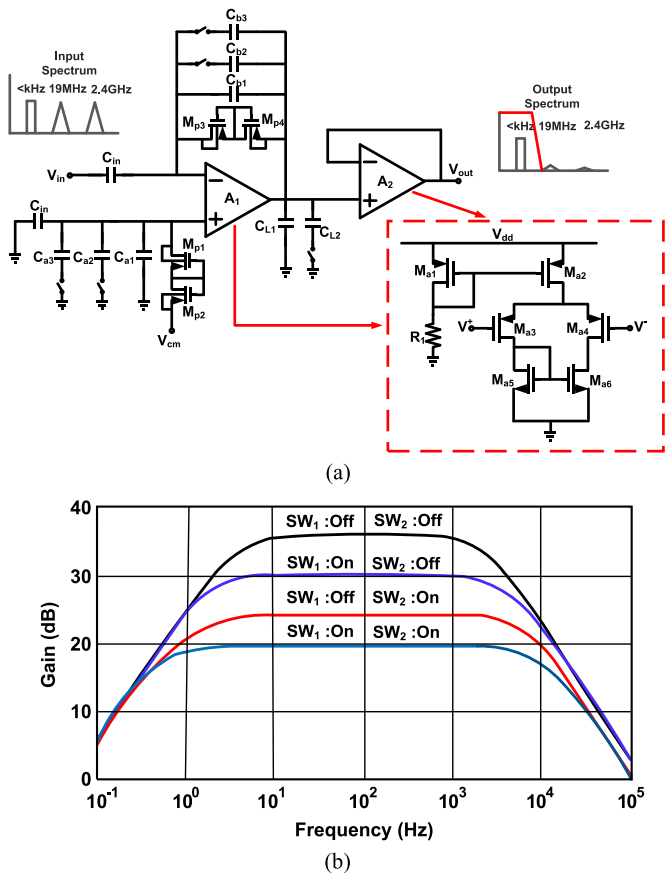


Fig. 12. (a) Schematic of the bandpass amplifier. (b) Simulation results of bandpass amplifier at various gain setting.

are used as a symmetric pseudo resistor with GΩ resistance [21]. In this manner, the chip area is effectively reduced. In order to adjust the bandwidth for various applications, $C_{a1} - C_{a4}$ and $C_{L1} - C_{L2}$ are added. Finally, a unit-gain buffer is employed between the bandpass amplifier and ADC to eliminate the load effects and shift the voltage to half supply, thereby providing an efficient voltage swing range before digitalization. Fig. 12(b) shows the simulation results of the bandpass amplifier at different gain settings. The amplifier gain can be adjusted from 20 dB to 37 dB.

A successive approximation register (SAR) architecture was chosen for the ADC to minimize power consumption. The 10-bit ADC was designed to operate at 10 kS/s. The clock signal of

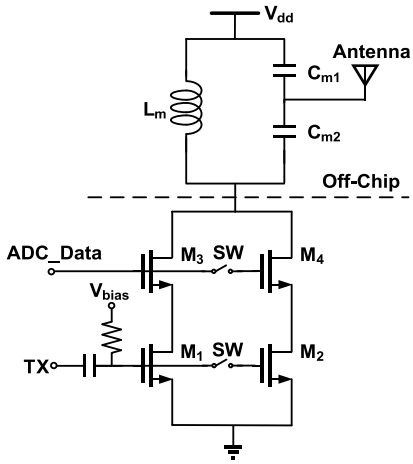


Fig. 13. Schematic of the driving amplifier.

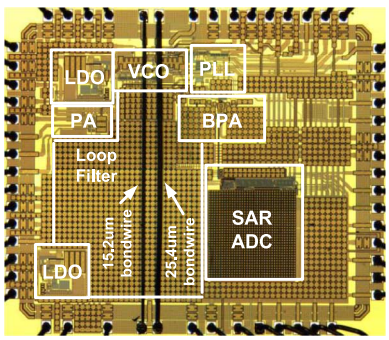


Fig. 14. Chip micrograph of a wireless bondwire accelerometer.

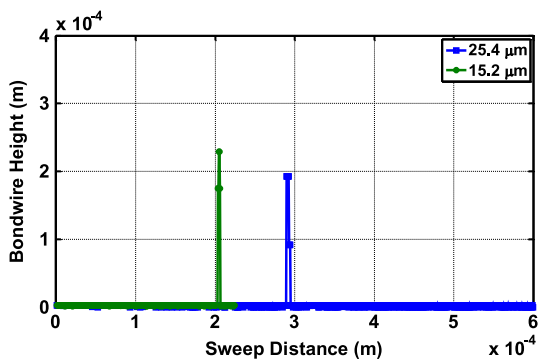
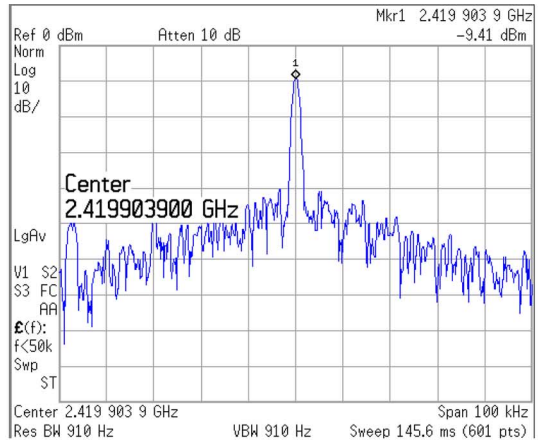


Fig. 15. Measured heights of thin and thick bondwire sensors.

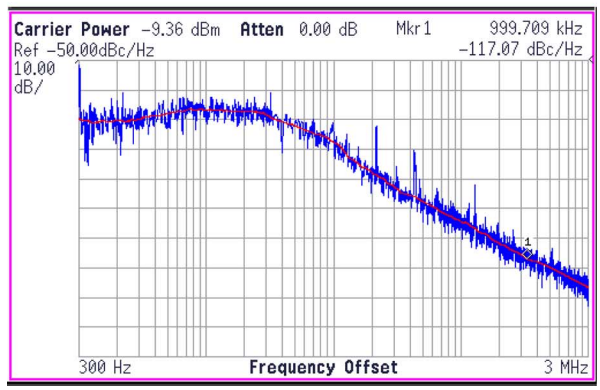
ADC comes from the divide-down signal of precise crystal oscillator (reference clock). The digital output is stored in a buffer and serially fed to the driving amplifier for wireless data transmission. The data transmission is activated by enabling a signal from the controller and synchronized with the reference clock.

D. Wireless Transmitter

Fig. 13 shows the schematic of driving amplifier. The driving amplifier is realized using cascode architecture to enhance the stability and isolation between output and input. An additional stage is added to adjust the output power of the driving amplifier, providing 6-dB power gain deviation in the low and high gain modes. A ladder-capacitor matching network is used to externally match a 50-Ω chip antenna on the PCB.



(a)



(b)

Fig. 16. Measured results of (a) spectrum (span:100 kHz); (b) phase noise of the PLL.

IV. Experimental Results

A. Sensor Characterization

The bondwire accelerometer is implemented in a 0.18-μm CMOS process without post processing. The chip micrograph is illustrated in Fig. 14. The accelerometer occupies a 2×2.4 mm^2 silicon area, including interface circuitry, loop filters, by-pass capacitors, and pads. To avoid the impact from board-induced stress and manufacturing variations, the 15.2 μm and 25.4 μm gold bondwire inertial sensors are bonded in parallel on the middle of the chip with a 2-mm-long trace. The precise ball-wedge wirebonding technology is used for fine pitch bonding on chip pad-to-pad. By on-chip bonding, the separation (90 μm) between two sensing bondwires is precisely defined. The separation is large enough to avoid wire sweeping by acceleration at mechanical resonance. The only mechanical deviation of the bondwire sensors is the height of the bondwires. The heights of thin (15.2 μm) and thick (25.4 μm) bondwires are measured using a 3D white light interferometer. Fig. 15 depicts the measured height of two bondwire sensors. The heights are 229 μm and 194 μm for thin and thick bondwire, respectively. The difference may result from the manufacturing variations and weight of the bondwires at different diameters.

B. Electrical Interface Characterization

Fig. 16 presents the measured output spectrum and phase noise of the PLL. The PLL bandwidth is set to 10 kHz for in-band noise and out-of-band spur suppression. The measured

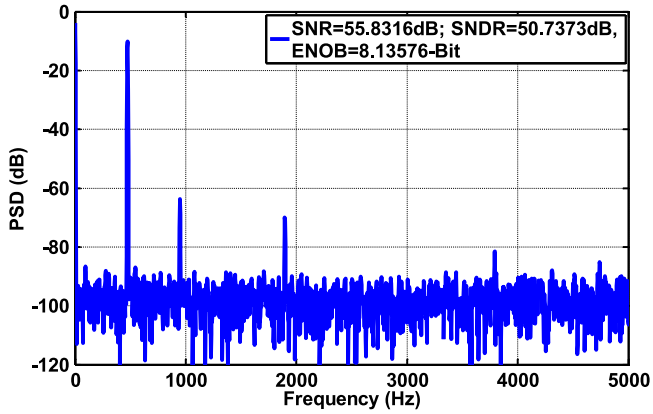


Fig. 17. Measured output spectrum of SAR ADC.

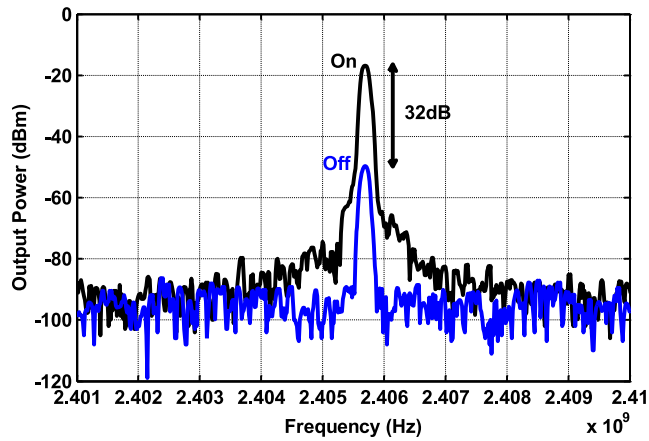


Fig. 18. Measured output spectrum of drive amplifier at on and off states.

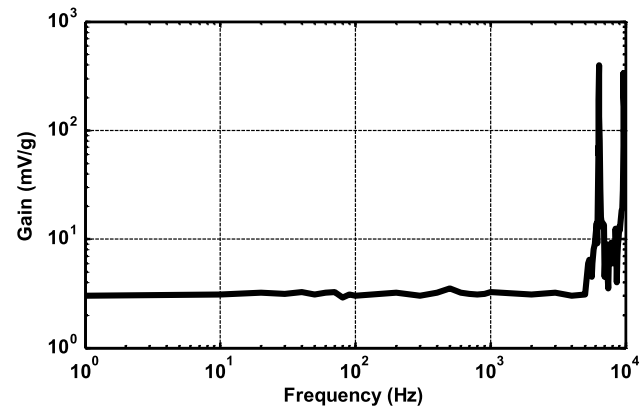


Fig. 19. Measured frequency response at the demodulator output (control line).

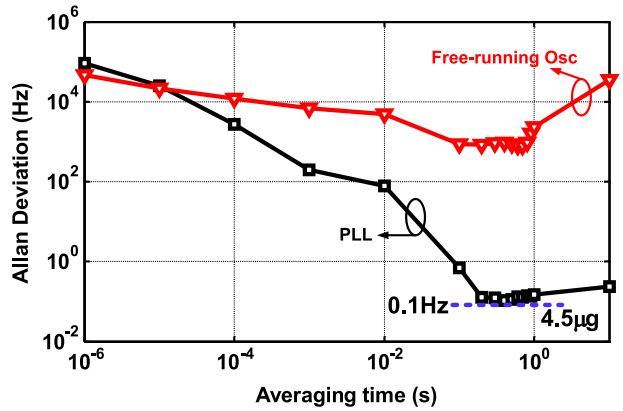


Fig. 20. Measured Allan deviation of the PLL-based demodulator.

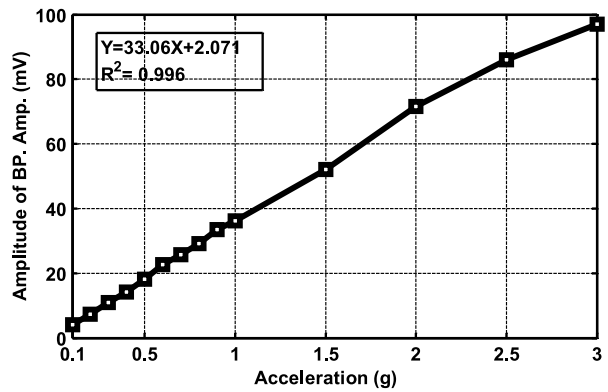


Fig. 21. Measured output amplitude of a bandpass amplifier vs. acceleration.

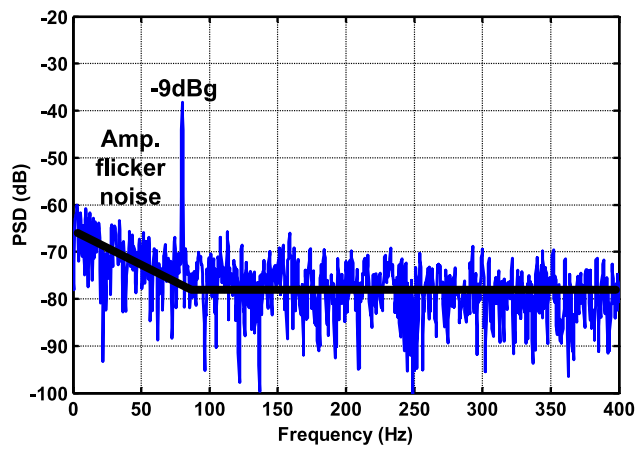


Fig. 22. Output power spectrum density of the bandpass amplifier at 80-Hz sinusoidal 0.5-g acceleration.

in-band (<10 kHz) signal-to-noise ratio is greater than 30 dB. The PLL achieves a phase noise of −117 dBc/Hz at 1-MHz offset. In order to achieve high frequency-to-voltage conversion gain, the KVCO of the oscillator should be minimized. Therefore, we used a small varactor ($9\ \mu\text{m} \times 9\ \mu\text{m}$) in series with a 93 fF capacitor. The measured KVCO is 3.7 MHz/V. However, the low KVCO may not be sufficient to overcome process variations. Therefore, a 6-bit capacitor bank is employed to extend the frequency range without sacrificing the KVCO. The frequency tuning range is 360 MHz from 2.4 GHz. Prior to further signal processing, the signal is digitalized by a low-noise bandpass amplifier and then digitalized by SAR ADC. The bandpass amplifier provides a tunable gain from 20 dB to 37 dB by switching the feedback capacitors. Fig. 17 presents the measured ENOB of the SAR ADC. The SAR ADC achieves an ENOB of 8.13 bits, which is sufficient for a resolution of 162 μg and 23 μg at the minimal and maximal gain setting, respectively. Digitalized data is transmitted wirelessly with on-off shifting key modulation. The output spectrum of a wireless transmitter is shown in Fig. 18. The deviation of output power between data "1" and "0" is 32 dB.

C. System Verification

For the acceleration test, the bondwire accelerometer was assembled on a PCB, which is mounted to a vertical shaker. To eliminate power line noise, the system is powered by a 1.8-V supply regulated from a 3-V on-board battery. Fig. 19 depicts

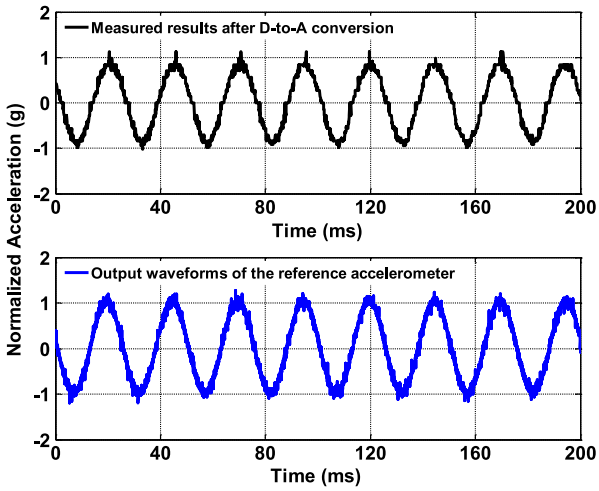


Fig. 23. Digital-to-analog conversion of received data from 40 Hz 1 g acceleration.

the measured frequency response at the control line of the PLL demodulator. The flat gain is 3 mV/g over a frequency range from 1 Hz to 5 kHz. Two resonant peaks occur at the mechanical resonance frequencies of 6.3 kHz and 9.6 kHz for the thin and thick gold bondwires, respectively. For long-term stability characterization of the bondwire accelerometer using a free-running oscillator and phase-locked loop demodulator, Allan deviation measurement is performed. Allan-variance measurement results are plotted in Fig. 20. We find that the PLL-based demodulator significantly improves the Allan deviation of output frequency from 950 Hz to 0.1 Hz at 0.4 second averaging time. The equivalent bias stability of the PLL-based demodulator is 4.5 μg at an integration time window of 0.4 seconds. Fig. 21 presents the measured outputs of the bandpass amplifier at the minimum gain setting over an acceleration range of up to 3 g, which is limited by the vertical shaker. The acceleration gain is 33 mV/g after 20 dB amplification and the R-square linearity is 0.996. Fig. 22 depicts the measured output spectrum (50-Ω load) of the bandpass amplifier at 80-Hz 0.5 g sinusoidal acceleration. The integral power signal-to-noise ratio is 28 dB. It corresponds to the average noise floor in the measurement bandwidth (400 Hz) of [5]

$$a_{ext,rms}10^{-SNR/20}/\sqrt{BW} = 0.7mg/\sqrt{Hz}, \qquad (5)$$

where $a_{ext,rms}$ is the root-mean-square excitation acceleration. The in-band noise performance can be further improved by using advanced noise reduction techniques, such as chopping [22] and correlated double sampling [23], at the amplifier stage. Fig. 23 depicts the wirelessly received 40-Hz 1-g acceleration data after digital-to-analog signal processing and output waveforms of the on-board reference accelerometer. Table I summarizes the performance of the proposed bondwire accelerometer and comparisons with state-of-the-art resonant accelerometers. Compared with the open-loop bondwire accelerometer, the proposed closed-loop bondwire accelerometer readout circuitry effectively improves the noise floor by 100 times and bias stability by over three orders through noise suppression and stabilization of a feedback loop. In addition, this design with no complicated fabrication has a performance that is comparable to MEMS accelerometers.

TABLE I
PERFORMANCE COMPARISON

	[4]	[5]	[12]	This work
Type	MEMS resonant	MEMS resonant	Bondwire resonant	Bondwire resonant
Readout	Closed-loop	Open-loop	Open-loop	Closed-loop
Tech. (μm)	0.35	0.18	0.13	0.18
Vdd (V)	3.3	1.8	1.2	1.8
B.W. (Hz)	N/A	6k	700	5k
Accel. Gain	0.825 kHz/g	3.62 MHz/g	10 kHz/g	11.1 kHz/g (33 mV/g)
Range (g)	2	N/A	3	3
Linearity(R^2)	N/A	0.988	0.99	0.996
NF ($\frac{\mu g}{\sqrt{Hz}}$)	20+	205	80000+	700
Bias stability	4 μg	3 mg	4 mg	4.5 μg
P_{diss} (mW)	23	N/A	13.5	*9
Wireless	No	No	No	Yes

*Include wireless transmitter and clock generation on the chip
+Estimated from Allan deviation without frequency-to-voltage conversion

V. CONCLUSION

This paper presented a fully-integrated wireless accelerometer using bondwire sensors on a 0.18-μm CMOS process without MEMS/IC integration. A pair of thin and thick gold bondwires was used as inertial sensors instead of using different materials. In the future, low-cost copper bondwires can be used for further cost reduction. A feedback readout architecture was implemented, thereby improving bias stability and providing noise suppression over 30 dB in required bandwidth. The wireless accelerometer system-on-a-chip achieved a bias stability of 4.5 μg, a noise floor of 700 $\mu g/\sqrt{\text{Hz}}$, and flat-gain bandwidth of 5 kHz, while only consuming 9 mW. To further save power consumption, the PLL was reused in the direct-conversion transmitter. The single chip accelerometer can enable advanced applications that require light-weight, low-cost wearable inertial sensing systems, such as consumer electronics for healthcare, gaming and mobiles.

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