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Implementation of TFET SPICE Model for Ultra-Low Power Circuit Analysis

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ABSTRACT We proposed a compact model for tunneling field effect transistors (TFETs), which combines BSIM4. Our proposed model for tunneling current is based on a drift-diffusion model under the gradual-channel approximation. The total charge for the drain current has been described by a weighted sum of the tunneling charge and the oxide charge for gate-to-source overlap region. In order to obtain TFETs compact model for circuit simulation that operates in every voltage region, the operating current under the various gate-to-source voltage and drain-to-source voltage conditions are considered. Verilog-A description for our proposed model are implemented in the circuit simulator. Model parameters are extracted for conventional TFETs structure by comparing with in-house 2-D TCAD simulation results. After the transistor-level verification, the circuit-level simulation of 81-stage ring-oscillator using our proposed model has been performed.

INDEX TERMS SPICE, semiconductor device modeling, field effect transistors.

I. INTRODUCTION

Tunneling field effect transistors (TFETs) are promising device structures for an ultra-low power circuits application [1]–[3]. The tunneling *p-n* junction in the gate-to-source overlap region leads to the steep subthreshold swing (*S.S.*) less than 60mV/decade [4]–[6]. Since the fabrication processes of Silicon (Si)-TFETs are compatible with conventional MOSFETs [7], it is expected to be the post Si-CMOS devices for low power technology. However, the circuit characteristics have not been understood yet, because the device structures and the operations of TFETs are different from that of MOSFETs [8]. Therefore, there are still some problems to be solved for the circuit design with TFETs, such as an interactive operation of the pass gate in SRAM [9], a correlation between the circuit operations and the device characteristics such as *S.S* and the threshold voltage (V_{th}), the body effect for staked circuits, and the variability in low voltage regime. In order to analyze the circuit performance using TFETs, few analytical models had been proposed [10]–[12]. In most published works, the on/off state of TFETs, which is dominated by the tunneling phenomenon, had been focused. In this work, we propose a TFETs compact model, which combines BSIM4 [13], that operates in every voltage region in order to apply it to the various circuit simulations with large number of transistors. Model parameters are extracted for a conventional TFETs structure by comparing with in-house 2D TCAD simulation results. Verilog-A description [14] for our proposed model are implemented in the circuit simulator in order to verify the usability of our model.

II. DEVICE MODELING

The schematic device structure and the energy-band diagram of TFET modeled in this study are shown in Fig. 1. The structure is conventional *n*-type TFET with a heavily doped *p*-type source with extension, an intrinsic channel and a *n*-type drain [15]. When the gate-to-source voltage (V_{gs}) is applied, the bias condition of *p-n* junction has a *reverse bias condition*. In this case, TFETs are set to "on state". Carriers are transported from source edge to channel region by the band-to-band (BTB) tunneling [16], [17], and then reach the drain region if the drain-to-source voltage (V_{ds}) is applied. When V_{gs} is set to be 0V of TFETs "off state",

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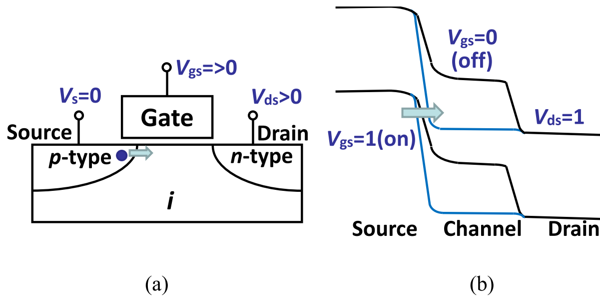

FIGURE 1. **(a) The schematic device structure and (b) the energy-band diagram for "conventional" *n*-type TFETs with a heavily doped *p*-type source with extension, an intrinsic channel and a *n*-type drain. When V_{ds}=1V, the device turns on if V_{gs} is applied. Carriers are transported from source edge to channel region by band-to-band (BTB) tunneling. When V_{gs}=0V, the device turns off even if V_{gs} is applied.**

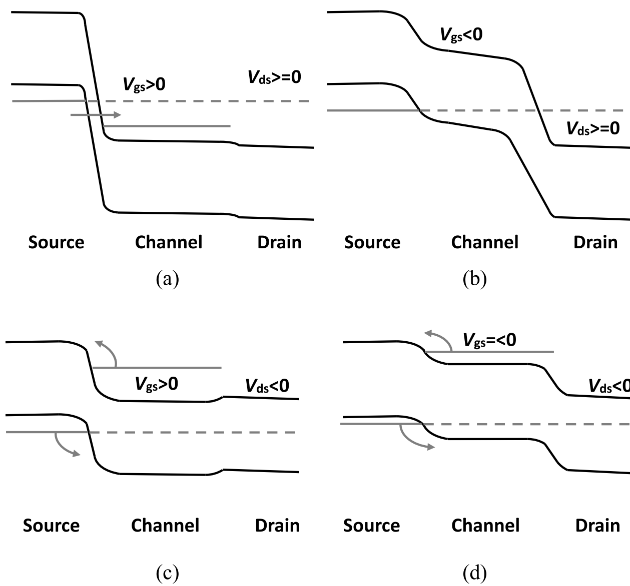

FIGURE 2. **Schematic energy-band diagram for *p*(source)-*i*(channel)-*n*(drain) junction: (a) V_{ds}>=0 and V_{gs}>0 (on state), (b) V_{ds}>=0 and V_{gs}<0 (off state), (c) V_{ds}<10 and V_{gs}>0, (d) V_{ds}<0 and V_{gs}=<0.**

carriers are inhibited tunneling from source valance band to channel conduction band even though V_{ds} > 0V. On the other hand, a *forward bias condition* for source-to-drain (S-D), *p-n* junction current flows by the injection of minority carrier [18]. In order to obtain TFETs compact model for circuit simulation, the operating current under the various V_{gs} and V_{ds} conditions are considered below (see Fig. 2):

1) *S-D reverse bias conditions (V_{ds}>=0)*
   a) *V_{gs}>0 (Fig. 2 (a))*
      BTB tunneling current is dominant, where the subthreshold current of TFETs has a steep *S.S.*
   b) *V_{gs}=<0 (Fig. 2 (b))*
      TFET is in the off state. The gate leakage current and the junction leakage current should be considered.

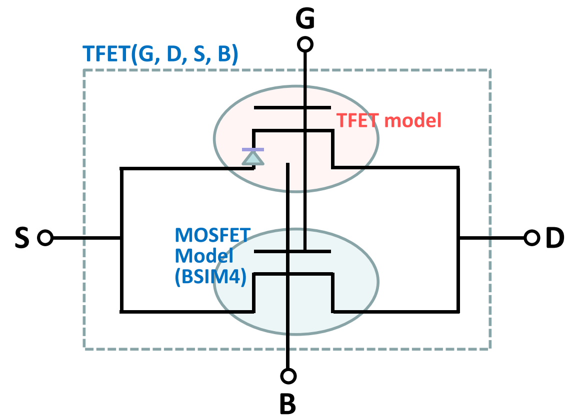

FIGURE 3. **Equivalent circuit model of TFET in this study. The drain current (I_d) of TFET(G, D, S, B) is a sum of the drain current of "TFET model" (I_{dTFET}) and "MOSFET model" ($I_{dMOSFET}$): $I_d(V_{gs}, V_{ds}) = I_{dTFET}(V_{gs}, V_{ds}) + I_{dMOSFET}(V_{gs}, V_{ds})$.**

2) *S-D forward bias conditions ($V_{ds<}$0)*
   a) *$V_{gs>}$0 (Fig. 2 (c))*
      The *p-n* diode current is dominant.
   b) *V_{gs}=<0 (Fig. 2 (d))*
      Not only the *p-n* diode current but also the gate leakage current should be considered.

It is difficult to express the steep *S.S.* of TFETs and the continuity of the transition region from weak inversion to strong inversion by using the existing model such as BSIM and HiSIM [19]. Figure 3 shows the equivalent circuit of "TFET" modeled in this study, which combines *"TFET model"* with the BTB tunneling current and the *p-n* diode current and *"MOSFET model"* using BSIM4 by parallel connection. The drain current (I_d) of TFET(G, D, S, B) is a sum of the drain current of "TFET model" (I_{dTFET}) and "MOSFET model" ($I_{dMOSFET}$), such as I_d (V_{gs},V_{ds}) = I_{dTFET}(V_{gs},V_{ds}) + $I_{dMOSFET}$(V_{gs}, V_{ds}).

A. MOSFET MODEL

"On current" and "off current" are determined by BTB tunneling current derived from "*TFET model*" and the leakage current derived from "*MOSFET model*". Figure 4 shows the current flow to the drain of TFETs. The gate leakage current (I_g) and the junction leakage current (I_j) are considered based on BSIM4. I_g represents the gate tunneling current between the gate and the drain diffusion region.

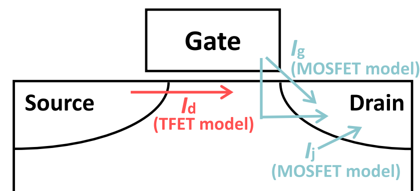

FIGURE 4. **Current flow to the drain of TFET. The gate leakage current (I_g) and the junction leakage current (I_j) are considered based on BSIM4.**

B. TFET MODEL

Under the following assumptions, we describe the drain current of "*TFET model*" with steep *S.S.*, namely:

- If the tunnel resistance is efficiently large, the channel charge capacitance of TFETs will be almost equals to that of the tunnel junction.

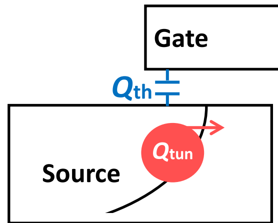

FIGURE 5. The schematic diagram of Q_{tun} and Q_{th}. Q_{tun} is related to the tunnel current and Q_{th} express the gate-to-source overlap region.

- As shown in Fig. 5, the total charge (Q_0) for the drain current (I_d) can be described by a weighted sum of the tunneling charge (Q_{tun}) and the oxide charge (Q_{th}) for the gate-to-source overlap region,

$$Q_0 = Q_{tun} \cdot f_1 + Q_{th} \cdot (1 - f_1), \qquad (1)$$

where f_1 is the smoothing function. Q_{tun} derived from BTB tunneling model [18], which includes the band gap energy and reverse bias voltage for the source side.

- In the reverse bias condition, I_d can be expressed by the product of Q_0 and the injection velocity (v_{inj}) of the source edge based on the drift-diffusion model under the charge sheet approximation, like short-channel MOSFETs model [20],

$$I_d = W \cdot Q_0 \cdot v_{inj}. \qquad (2)$$

The typical parameters for "*TFET model*" are listed in Table 1. "L", "W", and "N_{tun}" are process parameters defined by the targeted device structure. Although "μ_{tun}" and "μ_{th}" have the same dimension of the effective mobility of MOSFETs, it should be noted that they do not have a proportional relationship with I_d through Q_{tun} and Q_{th}. "μ_{tun}" can be expressed as $\mu_{tun} \sim d_{tran}/(E_s \cdot \tau_{tun})$, where E_s is the longitude electronic field for the tunnel junction and τ_{tun} shows the time required for the tunneling that include both the charging time and the carrier transit time near the tunnel junction. If it is assumed to be small enough to ignore the carrier transit time under some E_s, μ_{tun} will be dependent on the carrier charging time at the surface of the tunnel junction.

In order to analyze the circuit performance of TFETs, the tuning of parameter for *S.S.* and V_{th} is required, because the low power performance will be determined by its actual behavior in the circuit design. In our formation, it has been found that *S.S.* and V_{th} have a maximum correlation with "N_{tun}" and "V_{th0}", respectively. Furthermore, *p-n* diode current has been taken into account in case of S-D forward bias conditions ($V_{ds} < 0$). After the parameter for "on" and "off" current are determined by BTB tunneling current derived from "*TFET model*", that for the leakage current are determined by "*MOSFET model*" based on BSIM4. Also the extraction of *CV* model parameter has been calibrated with BSIM4 model.

TABLE 1. List of "*TFET model*" parameter for BTB tunneling current.

Symbol		*Unit*
ϕ_{bi}	Built-in potential	V
E_g	Band gap	eV
T	Temperature	K
L	Channel length	M
W	Channel width	M
D_{dibl}	Drain induced barrier lowering coefficient	V/V
v_{inj}	Injection verocity	m/s
R_s/R_d	Source/drain resistance	Ω
N_{tun}	Substrate concentration of the tunnel junction	cm^{-3}
μ_{tun}	Effective mobility of the tunnel junction	m^2/Vs
μ_{th}	Effective mobility of gate-to-source overlap region	m^2/Vs
V_{th0}	Threshold voltage	V
d_{tran}	Transition length of *p-n* junction[1)]	m

1) d_{tran} means the tunneling length.

III. MODEL EVALUATION

Our proposed model was implemented in SmartSpice [21] using Verilog-A description. In order to extract the model parameter for TFET with typical device characteristics, we compared with in-house 2D TCAD simulation results. Fig. 6 shows the 2D dopanat profile for TCAD simulation. The device structure was formed to demonstrate the steep *S.S.* of 50mV/decade and the ideal I_{on} required for the low-power operation. The channel length is 120nm, T_{ox} is 2nm and the substrate concentration is 1e16 cm^{-3}.

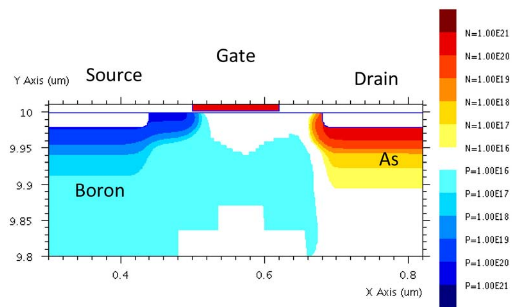

FIGURE 6. 2D dopant profile for our in-house TCAD simulation. The device structure was formed to demonstrate the steep *S.S.* of 50mV/decade and the ideal I_{on} required for the low-power operation. The channel length is 120nm, T_{ox} is 2nm and the substrate concentration is 1e16 cm^{-3}.

Fig. 7 shows the simulated I_d-V_g and I_d-V_d results. Our proposed model shows a good agreement with TCAD simulations in the targeted operating voltage range. Similarly, leakage current was also extracted. Fig. 8 shows the simulated current voltage results for various voltage regimes. After the transistor-level verification for model parameter which was verified through the convergent of the SPICE simulation, it has been found that our proposed

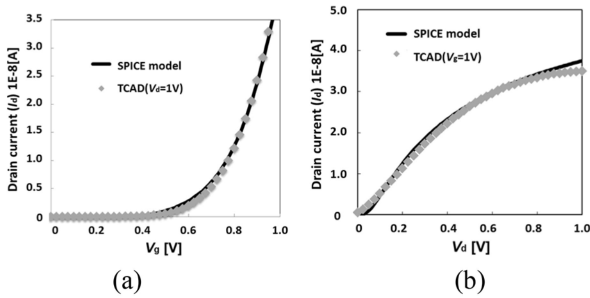

FIGURE 7. The simulated (a) I_d-V_g and (b) I_d-V_d results. Lines indicate the results obtained from our analytical model and symbols indicate the results obtained from 2D TCAD simulator.

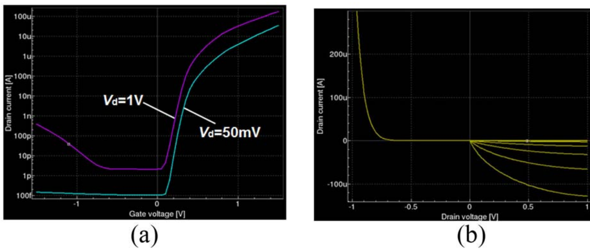

FIGURE 8. The simulated (a) I_d-V_g and (b) I_d-V_d result for the typical TFET characteristics. Our proposed model was implemented in SmartSpice [22] using Verilog-A description.

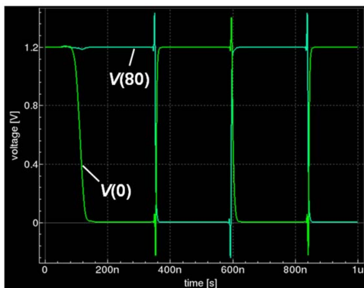

FIGURE 9. The simulated waveform for 81-stage ring oscillator.

model is useful tool for the circuit-level analysis from the simulation of 81-stage ring oscillator, as shown in Fig. 9.

IV. CONCLUSION

In this study, the compact model of TFETs, which combines BSIM4, has been proposed. In order to obtain TFETs compact model for circuit simulation that operates in every voltage region, the operating current under the various V_{gs} and V_{ds} conditions are considered. Model parameters for BTB tunneling current, leakage current were extracted for the conventional TFETs structure by comparing with 2D TCAD simulation results. In our formation, the steep *S.S.* less than 60mV/decade and the continuity of transition region from weak inversion to strong inversion have been expressed. The circuit-level simulation of 81-stage ring-oscillator using our proposed model was performed. Therefore, our proposed model will be a useful tool for characterizing an ultra-low circuit performance of TFETs.

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