Design and Development of Single Switch High Step-Up DC-DC Converter

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***Abstract*— In this paper, a new single switch high step-up dc-dc converter with high voltage gain is proposed. The proposed topology is developed by combining boost and SEPIC converter with diode - capacitor circuit to reduce the stress across the semiconductor devices. The proposed converter produces low switching voltage and hence it improves its efficiency. The operating principle and the steady state performance analysis are discussed. The performance of the converter is validated by developing a prototype circuit with input voltage of 30 V, output voltage of 300 V and output power rating of 250 W. The theoretical analysis and experimental results concludes the proposed converter is suitable for high voltage applications.**

***Index Terms*— DC-DC power conversion, high voltage gain, low voltage stress, single switch**

I. Introduction

THIS non isolated dc-dc converter with high static gain has gained focus in research as there is a requirement of this technology for many applications which generates low dc voltage sources. The non conventional energy resources like Photovoltaic (PV) modules, small wind turbines and fuel cells [1],[2] generates low dc voltage and needs to be stepped up. Normally, low voltages are ranging from 12 V to 125 V and it must be boosted up to ac grid requirement voltage [3].

Renewable energy based distributed generation of power production got tremendous development as a most essential power producing sector due to its clean and environment friendly nature. And these power production results in low voltage profiles where there is a need for different converter topologies. High step-up converter design needs some key requirements such as high power density, reduced switching voltage stress, low weight, and low cost.

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Digital Object Identifier

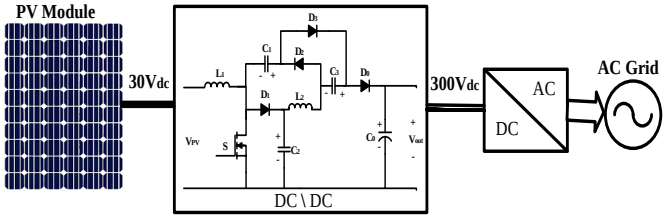


Fig. 1. Grid integrated PV based power generation system.

In transformer based converters high voltage conversion can be achieved by adjusting the turn's ratio which creates large leakage inductor problem. Also, it utilizes high frequency which impacts on high switching voltage stress, increase of range weight, volume and size, as well as the efficiency gets reduced [4]. The non-isolated high step-up converters generate the high voltage gain with reduced switching frequency for boosting up the voltage. Conventional boost converter is used in general, for stepping up the voltage for the non-isolated dc-dc converter family. Normally, it needs high duty cycle to generate the high output voltage [5]. The switching voltage stress is equal to the output voltage in boost converter and introduces large inductor current ripple. Hence it creates the large conduction loss and reverse recovery issues which affects the conversion efficiency and high voltage gain.

To achieve high step-up voltage gain and to improve conversion efficiency, many step-up dc-dc converters are proposed in [6]-[17]. The step-up converter is upgraded by using switched capacitor and coupled inductor [6], voltage doubler [7], diode-capacitor [8] and voltage lift [9] techniques. Some researchers proposed topologies that combines converters like classical boost converter with Single Ended Primary Inductor Converter (SEPIC) [10]-[12], integrate double boost with SEPIC [13], integrate boost with flyback converter [14], [15], and interleaved boost converters [16], [17].

In [18], coupled inductor based converter is used to achieve the high voltage gain, where the main switch is affected by leakage inductance and degrades the conversion effectiveness. To rectify the above issue, the active clamp circuit based coupled inductor topology has been proposed in [19]. The switched capacitors are used in converters to achieve high static gain in [20], but this will increase the cost of converter. Converters using voltage multiplier cell techniques have reduced the voltage stress with increase in high voltage gain. The overall system size and cost are increased with several multiplier cell stages [21]. The converter topologies proposed in [14]-[18], introduces the effect of Electro Magnetic Interference (EMI) because of high input current ripple.

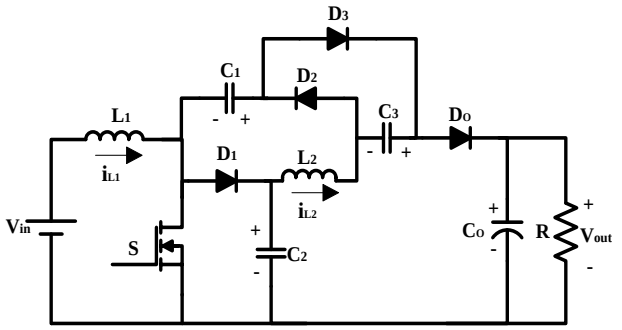


Fig. 2. Proposed non isolated high step-up converter.

To overcome the disadvantages listed in the previous discussions, a non-isolated dc-dc converter with single switch is proposed in this paper. The proposed converter introduces a diode-capacitor circuit in series and also uses low voltage rating of MOSFET, low resistance (R_{DS-ON}) due to which the voltage stress across MOSFET and diodes gets reduced. This increases the conversion efficiency of the proposed model.

The proposed converter is most suitable for the photovoltaic based power generation integrated with grid systems using inverter or ac module as shown in Fig. 1. The ratings of PV system with maximum output power (P_{MPP}= 250 W) and maximum output voltage (V_{MPP}= 30 V) has been considered for this study.

The further discussion of this paper is organized as follows: Section II presents the operational principles of the proposed converter. The performance analysis of the circuit is given in Section III. The design procedure of converter parameters is discussed in Section IV. The experimental results of 250 W prototype at full load condition are shown in Section V. Section VI, shows the conclusion of this study.

II. Operational Principle of Proposed Converter

The circuit topology of proposed converter is shown in Fig. 2. It consists of dc voltage source V_{in}, main switch S, three diodes D_1, D_2, and D_3, three capacitors C_1, C_2, and C_3, two inductors $L_1$and L_2, output diode D_O, and capacitor output C_O. To increase the static voltage gain, diode-capacitor based SEPIC converter is proposed with the combination of boost converter. The diode-capacitor elements reduce stress on the switch. The capacitor C_2 is charged with the output voltage of conventional boost converter. The voltage from capacitor C_2 is applied to the inductor L_2 during conduction period of power switch S which increases the voltage static gain, when compare to conventional SEPIC. In order to simplify the circuit analysis, following assumptions were considered;

1) Semiconductor switch and diodes are ideal;
2) Switching frequency is constant;
3) All capacitors are designed for less voltage ripple at the switching frequency;

A. Continuous Conduction Mode Operation

The continuous conduction mode (CCM) operation is discussed for the proposed converter with its operating modes as shown in Fig. 3.

1) Mode I [t_0-t_1]: In this mode, the switch S and diode D_3 is turned ON and diodes D_1, D_2, and D_O are in reverse biased condition as in Fig. 3(a). The energy is being stored in both inductors $L_1$and L_2. The generation of charging current from the input voltage, V_{in} makes capacitor C_1 to charge the capacitor C_3 through diode D_3 current (i_{C1}-i_{L2}). The output load gets energy from the discharge of output capacitor C_O. This operation ends, when diode D_3 current becomes zero at t=t_1.

2) Mode II [t_1-t_2]: In this mode, the switch S is turned ON and diodes D_1, D_2, D_3, and D_O are in reverse biased as shown in Fig. 3(b). The current from input supply V_{in} is used to charge the inductor L_1. As D_O is reverse biased, the output load R gets current flow due to capacitor current i_{C0}. This mode ends, when the diode D_2 starts conducting mode at t=t_2.

3) Mode III [t_2-t_3]: In this mode, the switch S and diode D_2 is turned ON and diodes D_1, D_3, and D_O are in reverse biased condition as shown in Fig. 3(c). The charge is stored in both inductors $L_1$and L_2. The capacitor C_1 is being charged by i_{C3} of capacitor C_3 through diode D_2. The output capacitor C_O starts discharging and provides the energy to load R. This mode of operation terminates, when the main switch S is turned OFF and diode D_2 current become zero at t=t_3.

4) Mode IV [t_3-t_4]: In this mode, the switch S and diode D_2 is turned OFF and diodes D_1, D_3, and D_O are in forward bias condition as shown in Fig. 3(d). This mode starts discharging the energy from both the inductors $L_1$and L_2 with reverse polarity. ThecapacitorC_2 is getting charged by the current (i_{L1}-i_{C1}-i_{L2}) which flows from the inductor L_1 and capacitor C_1.The output capacitor C_O and load R are getting charged from the capacitor C_3 through diode D_O. This mode of operation is ended, when the main switch S is turned ON at the next period.

The main theoretical waveforms of proposed converter are shown in Fig. 4. The switching voltage and voltage across all the diodes are less than the output voltage. The voltage in power switch S and the diodes D_1 and D_O are equal to the capacitor C_2 voltage. The voltage in diodes D_2 and D_3 is equal to the capacitor C_3 voltage. The output voltage is equal to the sum of the capacitors C_1 and C_2 voltage, when the switch is turned off and expressed as:

$$V_{out} = V_{C1} + V_{C2} \tag{1}$$

B. Discontinuous Conduction Mode Operation

The discontinuous conduction mode of the proposed converter is operated in three modes of operation, is shown in Fig. 5 and described as follows:

1) Mode I [t_0-t_1]: During this mode, the switch S and diode D_2 is turned ON and diodes D_1, D_3, and D_O are in reverse biased condition as shown in Fig. 5(a). The input current is stored in inductors L_1 and L_2. The current through the inductor L_2 is less than the L_1, but the voltage applied for both inductors are equal to input voltage V_{in} as in (2).

The output capacitor C_O discharges and transforms the energy to load R. This mode of operation ends, when the main switch S is turned OFF and diode D_2 current becomes zero at t=t_1.

$$V_{in} = V_{L1} = V_{L2} \tag{2}$$

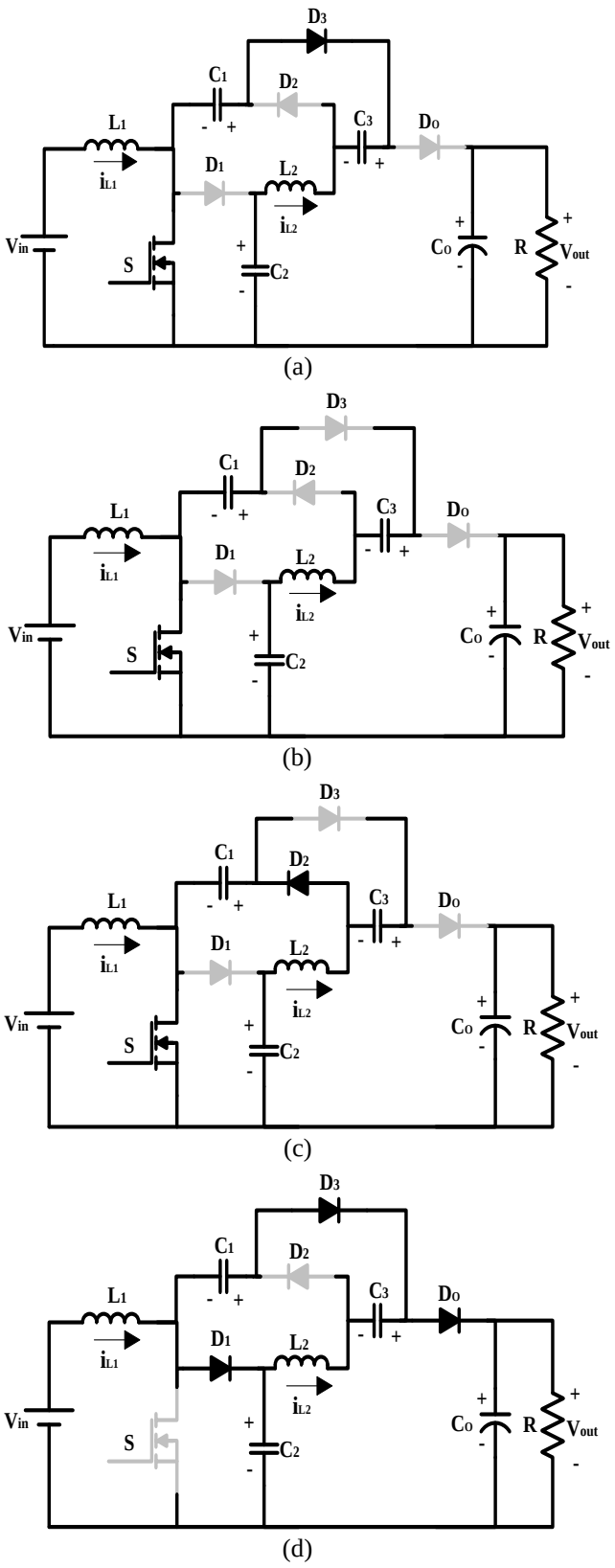


Fig. 3. Operational modes of the proposed converter during one switching period at CCM operation. (a) Mode I. (b) Mode II. (c) Mode III. (d) Mode IV.

2) Mode II [t_2-t_3]: During this mode, the switch *S* and diode D_2 is turned OFF and diodes D_1, D_3, and D_O are in forward bias condition as in Fig. 5(b). The current from input supply V_{in} is used to charge the inductor $L_1$and capacitor C_2 in turn the current i_{C2} is used to charge the inductor L_2. The capacitor C_2 is charged by the current flowing through the diode D_1 and the switching voltage is equal to capacitor C_2 voltage. In this mode, t_d is the conduction time of diodes during which the inductors L_1 and L_2 energy is transferred to C_1 and C_2 respectively. The output capacitor C_O and load *R* are getting charged from the capacitor C_3 through diode D_O.

3) Mode III [t_2-t_3]: During this mode, the switch *S* is turned OFF and diodes D_1, D_2, D_3, and D_O are in reverse bias condition as shown in Fig. 5(c). The voltage across the inductors L_1 and L_2 become zero and current through the inductors remains same as given in (3), where the mode acts in freewheeling stage. The charge stored in capacitor C_O is discharged to load *R*. When switch S is turned ON condition, this mode ends at $t=t_3$.

$$V_{L1} = V_{L2} = \Delta i_{L1} = \Delta i_{L2} = 0 \tag{3}$$

The main theoretical DCM waveforms of proposed converter are presented in Fig. 6. The average current inductor L_1 is equal to the input current ripple and average current of the inductor L_2 is same as the output current of the converter.

III. Performance Analysis of the Proposed Converter

Steady state analysis and their design equations of the proposed converter are presented in this section.

The static gain of the proposed converter is obtained by assuming average inductors voltage as zero at steady state condition. During CCM operation, the following relation (4) is formulated for the inductor L_1.

$$V_{in} D = (V_{C2} - V_{in})(1 - D) \tag{4}$$

where, V_{in} is the input voltage of proposed converter, *D* is the duty cycle, and V_{C2} is the capacitor voltage. The capacitor C_2 and C_3 voltages are obtained similar to conventional boost converter static gain as given below,

$$\frac{V_{C2}}{V_{in}} = \frac{1}{1-D} \tag{5}$$

$$\frac{V_{C3}}{V_{in}} = \frac{1}{2(1-D)} \tag{6}$$

The relation considered for the average inductor L_2 voltage at steady state condition is given in (7),

$$(V_{C2} - V_{C1})D = (V_{out} - V_{C2} - V_{C3})(1 - D) \tag{7}$$

From equation (1),

$$V_{C1} = V_{out} - V_{C2} \tag{8}$$

By substituting (5), (6) and (8) in (7), the voltage gain is computed as,

$$\frac{V_{out}}{V_{in}} = \frac{3+D}{2(1-D)} \tag{9}$$

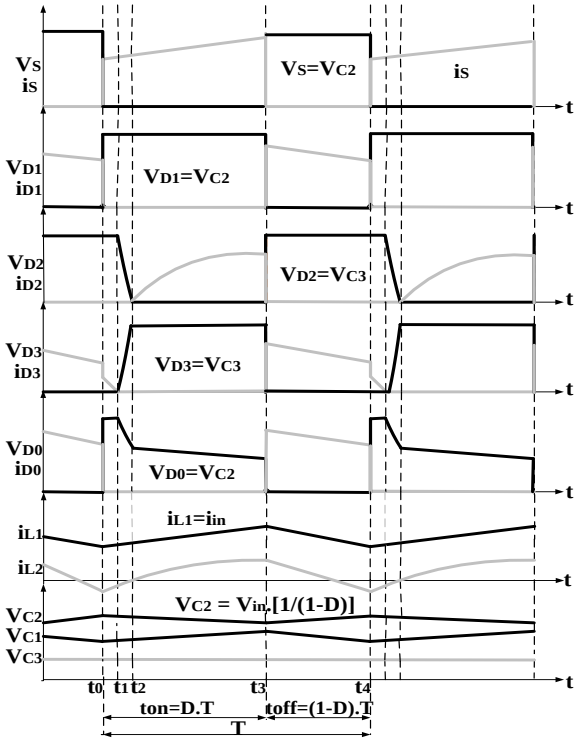


Fig. 4. Main theoretical CCM operation waveforms of the proposed converter.

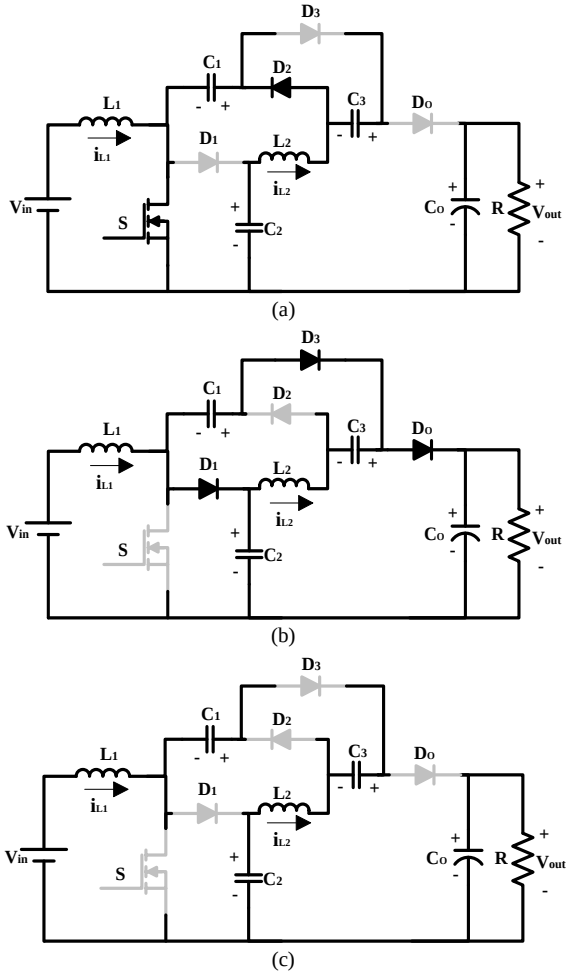


Fig. 5. Operational modes of the proposed converter during one switching period at DCM operation. (a) Mode I. (b) Mode II. (c) Mode III.

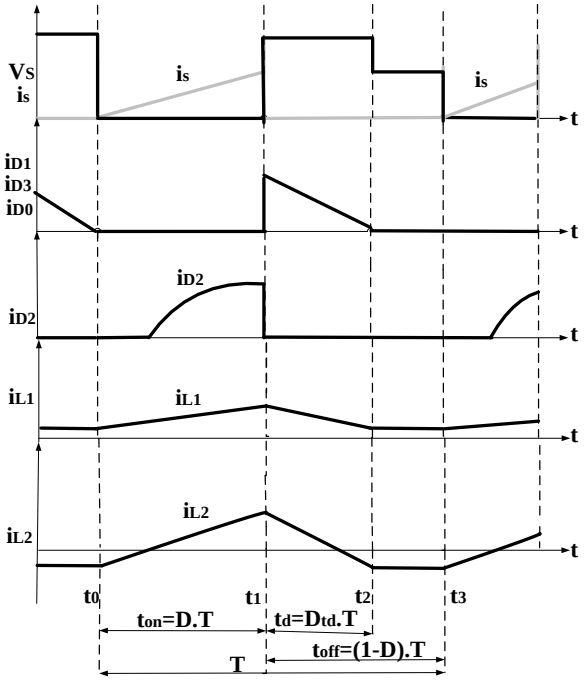


Fig. 6. Main theoretical DCM operation waveforms of the proposed converter.

Equation (9), is rearranged to find duty cycle as (10),

$$D = \frac{2V_{out} - 3V_{in}}{2V_{out} + V_{in}} \tag{10}$$

The capacitor C_1 voltage is formulated by substituting (5) and (9) in (8),

$$\frac{V_{C1}}{V_{in}} = \frac{1+D}{2(1-D)} \tag{11}$$

The static gains of the classical boost, SEPIC, modified SEPIC [10], high step [23] along with proposed converter are illustrated in Fig. 7. From Fig. 7, it is observed that the voltage gain of the proposed converter reaches maximum of 10 with duty cycle of D = 0.81. Also, it is observed that the proposed converter gain is higher than other compared converters at any particular duty cycle. During the DCM operation, the proposed converter at steady state condition with voltage across the both inductors to be assumed as zero and the capacitor C_2 voltage is equal to sum of the input voltage V_{in} and capacitor C_1 voltage in equation (12). The operation mode in DCM of proposed converter is illustrated as follows:

$$V_{C2} = V_{in} + V_{C1} \tag{12}$$

The average voltage across both the inductors $L_1$and L_2 are equal to null, during the steady state operation of the converter as given in (13), D_{td} is duty cycle during $t_{d,}$ and t_d is the conduction period of diodes D_1, D_3, and D_O.

$$V_{in} D = (V_{C2} - V_{in}) D_{td} \tag{13}$$

$$\frac{V_{C2}}{V_{in}} = \frac{D_{td} + D}{D_{td}} \tag{14}$$

From the (1), the capacitor C_2 voltage is considered as,

$$V_{C2} = V_{out} - V_{C1} \tag{15}$$

Substituting (12) in (15), the capacitor C_1 voltage is obtained as follows:

$$V_{C1} = \frac{V_{out} - V_{in}}{2} \tag{16}$$

Substituting (16) in (15), the capacitor C_2 voltage is obtained as follows:

$$V_{C2} = \frac{V_{out} + V_{in}}{2} \tag{17}$$

The static gain of proposed converter is obtained for DCM operation by substituting (17) in (14),

$$\frac{V_{out}}{V_{in}} = \frac{D_{td} + 2D}{D_{td}} \tag{18}$$

$$D_{td} = \frac{2V_{in}D}{V_{out} - V_{in}} \tag{19}$$

The average current through the diode D_O is equal to the output current I_{out},

$$\frac{1}{2} D_{td} i_{Do} = I_{out} \tag{20}$$

where,

$$i_{Do} = \frac{V_{in}}{L_{eq} f_S} D \tag{21}$$

$$L_{eq} = \frac{L_1 L_2}{L_1 + L_2} \tag{22}$$

Combining (19), (20) and (21), the output voltage can be obtained and the voltage gain in DCM operation with inductor time constant, τ is,

$$\frac{V_{out}}{V_{in}} = \left(\sqrt{1 + \frac{2D^2}{\tau}} \right) \tag{23}$$

The capacitor C_1 voltage is derived by substituting (16) in (18),

$$\frac{V_{C1}}{V_{in}} = \frac{D}{D_{td}} \tag{24}$$

The theoretical analysis, modes of operation and waveforms of proposed converter for both CCM and DCM operation is presented in this paper. The static gain, capacitors C_1 and C_2 voltages are derived for both CCM and DCM operations in proposed converter.

During boundary conduction mode, the voltage gain of CCM is equal to DCM. Combining (9) and (23), the normalized boundary inductor time constant can be calculated as follows,

$$\tau_B = \frac{2D(1-D)^2}{1+3D} \tag{25}$$

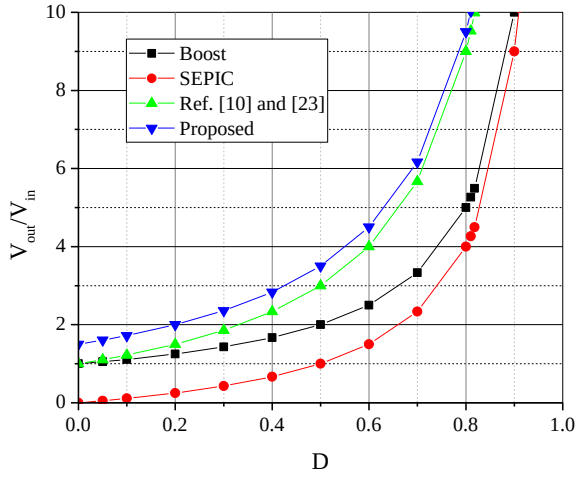


Fig. 7. Converters static gain waveforms.

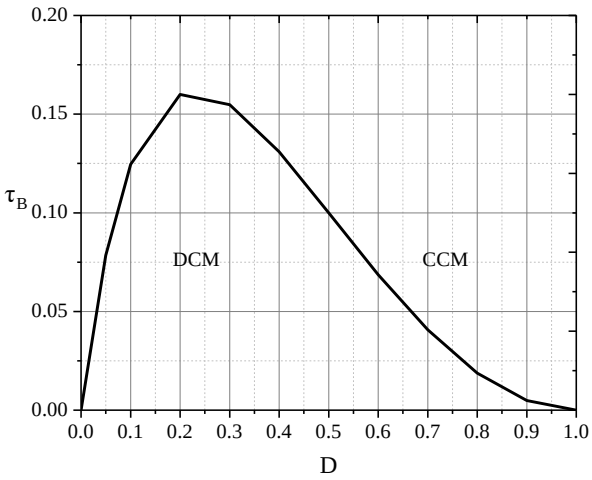


Fig. 8. Boundary condition of the proposed converter.

Fig. 8, plots the relation between τ_B and D. If, $\tau > \tau_B$ the converter operates in CCM, else it will operate in DCM. Table I shows the comparison of components used in proposed converter with other converters. From [22], four types of converters are chosen for comparison which is designed with 50 kHz switching frequency. The SH-SLC (Symmetrical Hybrid – Switched Inductor Converters) and SC-boost (Switched capacitor - boost) has the average sum of input and output voltage as switching voltage. The AH-SLC (Asymmetrical Hybrid – Switched Inductor Converters) has the drawback of high switching voltage. The SL-boost (Switched Inductor - boost) and [23] has the similar static gain with switching voltage equal to the output voltage of the converter. The proposed converter operates with less switching frequency and reduced switching voltage for high voltage gain, when compared with other converters. The efficiency of the proposed converter is 92.2% which is better than the other converter topologies for full load condition and operates with low switching voltage.

TABLE I
COMPARISON OF CONVERTERS PARAMETERS

Topology	[22]				[23]	Proposed Converter
	SH-SLC	AH-SLC	SC-Boost	SL-Boost		
Output Power, P	200 W	200 W	200 W	200 W	100 W	250 W
Input Voltage, V_{in}	20-40 V	20-40 V	20-40 V	20-40 V	25-45 V	30 V
Output Voltage, V_{out}	200 V	200 V	200 V	200 V	380 V	300 V
Switching Frequency, F_s	50 KHz	50 KHz	50 KHz	50 KHz	100 KHz	24 KHz
(No. Of Switch, Diode, Inductor, Capacitor)	(2, 7, 4, 1)	(2, 4, 3, 1)	(1, 3, 2, 3)	(1, 4, 2, 1)	(1, 3, 1, 3)	(1, 4, 2, 4)
Voltage Gain	$\frac{1+3D}{1-D}$	$\frac{1+2D}{1-D}$	$\frac{4}{2(1-D)}$	$\frac{1+D}{1-D}$	$\frac{1+D}{1-D}$	$\frac{3+D}{2(1-D)}$
Switching Voltage Stress	$\frac{V_{out}+V_{in}}{2}$	$\frac{1+2V_{out}}{3}$	$\frac{V_{out}+V_{in}}{2}$	V_{out}	V_{out}	$\frac{V_{in}}{1-D}$
Efficiency, η (Full load condition)	91.5%	90.3%	90.1%	89%	90.6%	92.2 %

IV. DESIGN STEPS OF THE PROPOSED CONVERTER

The equations used to design the proposed non-isolated dc-dc converter operating in continuous conduction mode (CCM), are presented in following specifications:

A. L_1 and L_2 Inductances

The value of input inductance is designed by using the equation (26) and (27).

$$L_1 = \frac{V_{in}D}{\Delta i_L f_S} \tag{26}$$

$$L_2 = \frac{V_{C2}.(1-D)}{f_S.\Delta i_{L2}} \tag{27}$$

where, f_S is the switching frequency, Δi_L is ripple current V_{C2} is the capacitor voltage and V_{in} is the input voltage.

B. C_1, C_2 and C_3 Capacitors

The capacitors C_1, C_2 and C_3 are designed for proposed converter by assuming same voltage ripple. Usually, the small capacitance value is obtained with low series equivalent resistance. The value of capacitor is designed by using the capacitor voltage ripple ΔV_C in the equation (30). A capacitor voltage ripple as 10% (0.1) of the nominal voltage of the capacitor C_2 is assumed. The capacitor charge variation ΔQ is given as,

$$\Delta Q = \frac{I_{out}D}{f_S} \tag{28}$$

$$\Delta V_C = \frac{\Delta Q}{C} \tag{29}$$

$$C = C_1 = C_2 = C_3 = \frac{I_{out}D}{\Delta V_C f_S} \tag{30}$$

where,

$$\Delta V_C = \left(\frac{V_{in}}{1-D}\right)(0.1) \tag{31}$$

C. Power Switch Voltage

The switching voltage is an important parameter of a circuit in high voltage application which increases the converter cost and efficiency. The proposed converter in this paper drastically reduces the high switching voltage compared with conventional boost and SEPIC converter. The switching voltage of proposed converter is equal to the capacitor C_2 voltage and is given in (32). From the analysis, the switching voltage of the proposed converter is less than the output voltage for all different input voltage.

$$V_S = \frac{V_{in}}{1-D} \tag{32}$$

where, V_s is the switch voltage of the proposed converter.

D. Output capacitor C_O

The output capacitor is represented as the function of duty cycle D, output current I_{out}, switching frequency and output voltage ripple ΔV_O. The output capacitor is calculated using (33), by considering peak-peak output voltage ripple equal to 1% of the output voltage,

$$C_O = \frac{I_{out}D}{f_S \Delta V_O} \tag{33}$$

where, $$I_{out} = \frac{V_{out}}{R} \tag{34}$$

where, R is the load and V_{out} is the output voltage of proposed converter.

The proposed converter can be utilized for various applications and it has been designed for 250 W which is more suitable for photovoltaic system.

V. EXPERIMENTAL RESULTS

To express the usefulness of the notional analysis in the proposed converter, a prototype circuit model is implemented and tested in the laboratory as shown in Fig. 9. The components used in the prototype model along with its ratings are tabulated in Table II.

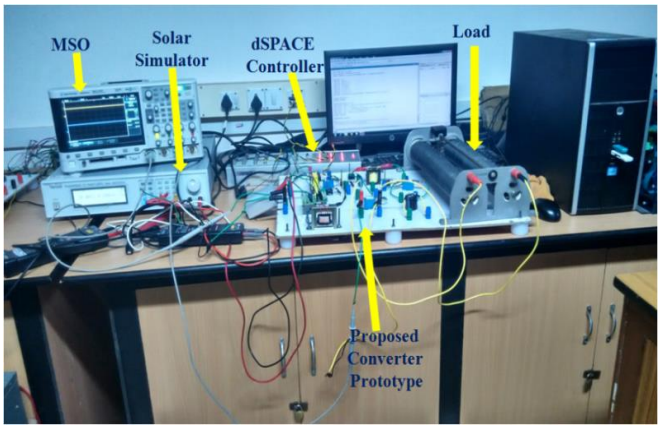
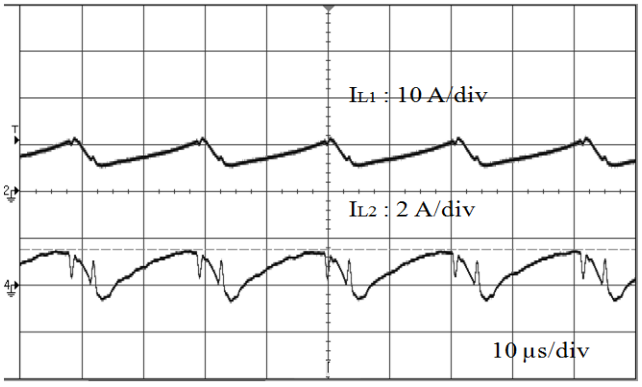


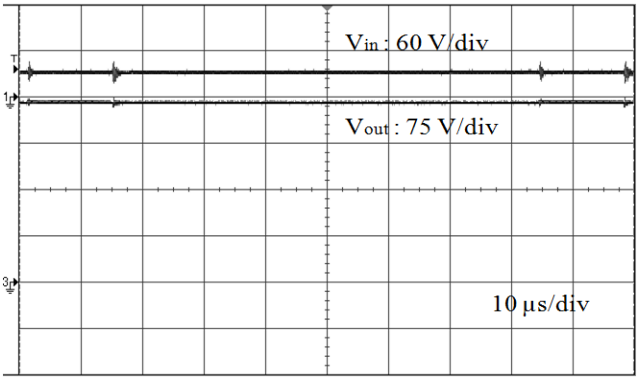
Fig. 9. Experimental prototype of proposed converter.

TABLE II
COMPONENTS AND PARAMETERS OF PROPOSED CONVERTER

Components	Parameters
Maximum Output Power, P	250 W
Input Voltage, V_{in}	30 V
Output Voltage, V_{out}	300 V
Switching frequency, f_s	24 kHz
Power MOSFET, S	IXFB110N60P3
Diodes, D_1, D_2, D_3, and D_O	VS-15EWX06FN-M3
Inductance, L_1 and L_2	205 µH and 180 µH
Capacitors, C_1, $C_2$and C_3	2.08 µF/250 V
Output Capacitor, C_O	140 µF/600 V



(a)



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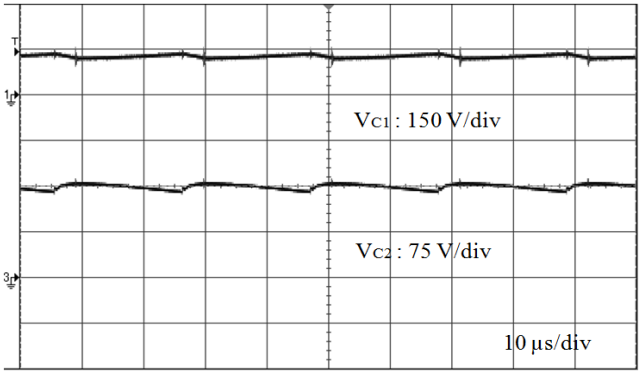

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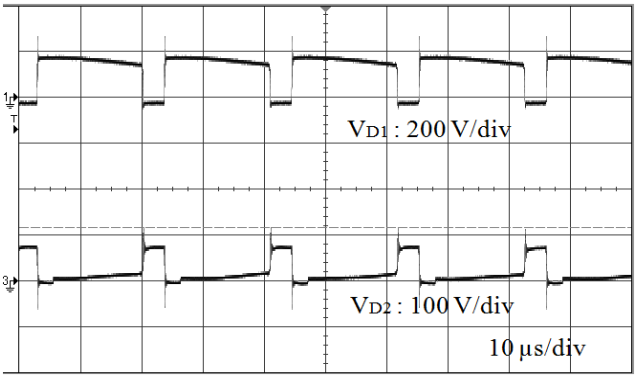

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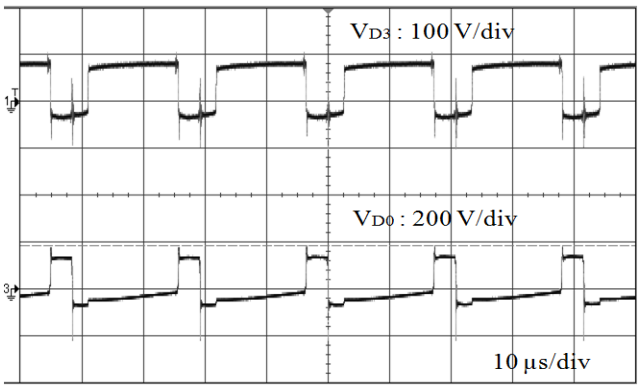

(e)

Fig. 10. Experimental results of proposed converter. (a) I_{L1} and I_{L2} (b) V_{C1} and V_{C2} (c) V_{in} and V_{out} (d) V_{D1} and V_{D2} (e) V_{D3} and V_{DO}.

TABLE III
COSTS ANALYSIS OF PROPOSED CONVERTER

Components	No. of items	Parameters (250 kW)	USD (250 kW)	Parameters (250W)	USD (250 W)
Switch, S	1	FZ1500R33HE3BPSA1	$ 2343.42 (including gate driver)	IXFB110N60P3	$ 21.52(including gate driver)
Diodes, {D_1, D_2, D_3, and D_O}	4	D291S45T	$ 386.06 x 4 = $ 1544.24	VS-15EWX06FN-M3	$ 1.43 x 4 = $ 5.72
Inductance, {L_1 and L_2}	2	14.85 mH and 13.57 µH	$ 311.19 x 2 = $ 622.38	205 µH and 180 µH	$ 13.23 x 2= $ 26.46
Capacitors, {C_1, $C_2$and C_3}	3	24.29 µF/ 18 kV	$ 19.26 x 3 = $ 57.78	2.08 µF/ 250 V	$ 3.73 x 3 = $ 11.19
Output Capacitor, {C_O}	1	1.917 mF/ 25 kV	$ 757.44	140 µF/ 600 V	$ 33.21

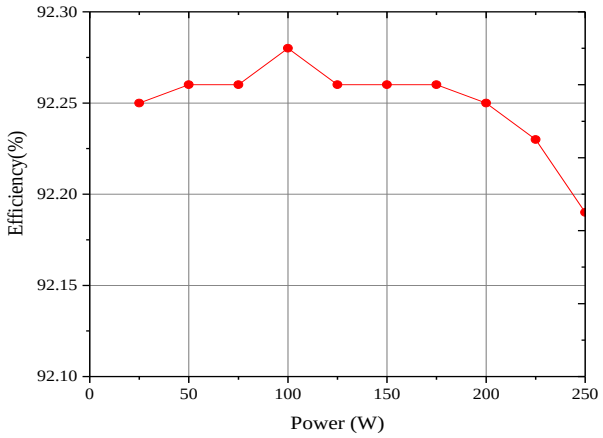

Fig. 11. Efficiency curve of the proposed converter under various power.

All the results obtained from the proposed converter are measured using Mixed Signal Oscilloscope (MSO). The switching pulse required for MOSFET is generated using dSPACE 1104 controller. The results taken from the proposed high step-up dc-dc converter operated under CCM at full load (250 W) is shown in Fig. 10. Fig. 10(a) shows the L_1 and L_2 inductor current waveforms. The input current is equal to the average of L_1 current and the output current is equal to the average of L_2 current.

In Fig. 10(b) capacitors C_1 and C_2 voltage waveforms are shown. From the Fig. 10(b) it is observed that, the value of capacitor is 161 V and the C_1 voltage is around to 142 V. The sum of capacitors C_1 and C_2 voltages is equal to the output voltage of the proposed converter. The input and output voltage waveforms for the proposed converter clearly shows that the voltage is stepped up ten times than the input voltage given to the converter and they are shown in Fig. 10(c). The input voltage given to the converter is 30 V and it provides output voltage of 297 V which is approximately near to the designed voltage level.

The switching voltage of power MOSFET is verified and found that in proposed converter it is 162 V. Fig. 10(d) and (e), shows the diodes D_1, D_2, D_3, and D_O voltage waveforms. The voltage waveforms of diodes D_1 and D_O is 163 V and 158 V which is close to the capacitor C_2 voltage (~161 V) and diodes D_2 and D_3 is 78 V and 82 V which is nearly the capacitor C_3 voltage (~78.5V). Fig. 11 shows the experimental results of the converter efficiency under various loading conditions. The proposed converter efficiency is equal to 92.2 % at the full load power. Table III shows the cost analysis of the proposed converter for two different rating like 250 W and 250 kW. It clearly shows that the proposed converter is more cost effective when the power rating increased. The proposed converter for 250 W power rating is designed and tested in laboratory setup and validated the results.

VI. CONCLUSION

A new single switch high static gain non-isolated dc-dc converter is presented in this paper. The proposed converter topology is suitable for renewable energy based applications having low input dc voltage. The proposed converter provides high voltage conversion without using transformer and coupled inductor. The semiconductor power devices used in this topology having reduced voltage stress with low ON-resistance in switch. The steady state analysis based CCM and DCM operations are performed with static gain and presented in this paper. The experimental prototype of the proposed converter is implemented and verified its operation in laboratory. The prototype results ensure high efficiency and high voltage gain with low conduction loss can be achieved. The efficiency of proposed converter achieves 92.2% operating with input voltage equal to 30 V and output voltage around 300 V.

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