A High-Speed, Low-Offset and Low-Power Differential Comparator for Analog to Digital Converters

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***Abstract*—Analysis and design of a high-speed comparator with improved input referred offset is presented in this paper. The proposed comparator is designed in TSMC low power CMOS technology under 1.2 V power supply. The new presented comparator has a low power consumption and utilizes dual offset cancellation technique. The minimum convertible input voltage is calculated to be 52 µV and the propagation delay at this worst case is equal to 219 ps. The power consumption at 1 GHz clock frequency is 755 µW. Monte Carlo simulation with 500 points iteration shows that the standard deviation of the input referred offset is about 723 µV.**

Keywords—High speed comparator; low offset; low power; low kickback noise

I. INTRODUCTION

Comparators play the most important role in voltage based analog to digital converters (ADCs) such as successive approximation register (SAR), Pipeline, and specifically in Flash ADCs [1-3]. Designing the comparators in the lower power supply with higher speed and lower power has its own challenges. Besides, realizing circuits in sub-nano CMOS technologies need digitally assisted circuits and complex techniques to overcome the kickback noise and offset voltage [4-6]. The kickback noise and offset variation due to the capacitive path to the input can degrade the overall performance of the system, e.g., it can shift the different reference voltage levels in Flash ADC. This degradation will result in the erroneous conversion process.

The design and analysis of the proposed comparator is discussed and presented in this paper. The paper is organized as follows; the proposed comparator idea and circuit implementation explained and discussed in Section II, and the simulation results are covered in Section III. Finally, the comparator performance is concluded in Section IV.

II. PROPOSED COMPARATOR CIRCUIT IMPLEMENTATION

Clocked regenerative comparators are suitable for high-speed Flash and SAR analog to digital converters. Proposed implemented comparator is shown in Fig. 1. Input voltage appears on the left plate of C_s and the common mode voltage will be applied to another plate when the clock is low. Consequently, V_{ref} and $V_{cm}\neg V_{in}+V_{ref}$ are applied to the left and right plates when the clock is high, respectively. It is worth mentioning that the comparator is chosen to be differential due to the robustness against the process, voltage, and temperature (PVT) variation.

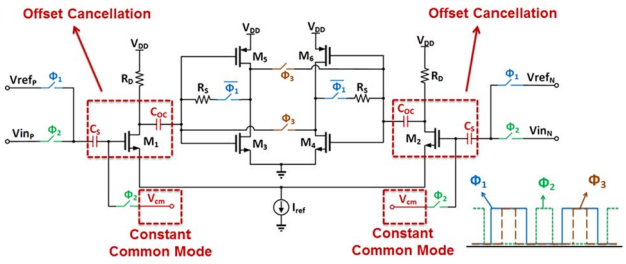

Fig. 1. Proposed comparator circuitry

The proposed comparator delay consists of the preamplifier and latch delays. Latch delay can be written as [7]:

$$t_{Latch} = \frac{C_L}{g_{m,eff}} \ln\left(\frac{\Delta Vout}{\Delta Vin}\right) \quad (1)$$

Where $g_{m,eff}$, ΔV_{out}, C_L, and ΔV_{in} are defined as back to back effective transconductance, output differential voltage, load capacitor, and differential input voltage, respectively. The differential preamplifier output voltage can be calculated as:

$$A_{pre} = \frac{g_m \times R_D}{1+\frac{j\omega}{\omega_0}} \quad (2)$$

$$\Delta V_{o,pre} = 2R_D \omega_o \left(\frac{I_{D,1}}{V_{OD,1}} + \frac{I_{D,2}}{V_{OD,2}}\right) e^{-\omega_0 t_{pre}} \quad (3)$$

Where R_D is the differential pair output resistor, ω_0 is the 3dB-bandwidth of the preamplifier, $I_{D,i}$ and $V_{OD,i}$ are the i-th transistor biasing current and overdrive voltage. Based on the (3) and (1), the total propagation delay for the two-stage comparator is:

$$t_p = t_{latch} + t_{pre} \quad (4)$$

$$t_p = \frac{C_L}{g_{m,eff}} \ln\left(\frac{\Delta Vout}{\Delta Vo,diff}\left(\frac{\Delta Vo,diff}{2\,R_D\,\omega_0} \cdot \frac{V_{OD,1}\,I_{D,2}+V_{OD,2}\,I_{D,1}}{V_{OD,2}\,V_{OD,1}}\right)^{\frac{1}{\omega_0}}\right) \quad (5)$$

Equation (5) shows the impact of different parameters on the propagation delay. The propagation delay of the comparator is inversely proportional to the input common mode voltage. By decreasing the common-mode voltage, the propagation delay

will increase. Therefore, keeping the common mode voltage constant, is the main challenge which is considered into the proposed comparator design through the ϕ_2 switch when the clock is in reset mode. This is the principal benefit of the proposed comparator since a big issue of the comparators used in Flash ADCs can be resolved and the maximum input dynamic range of the ladder can be utilized. The comparator works based on the input voltage storage on the capacitor, it takes a time to charge and discharge the capacitor with respect to the input voltages. Therefore, the sample and set signals should be non-overlapping clocks.

Dual offset cancellation is embedded into the circuit through capacitors, C_S and C_{OC}. C_S samples the input signal and stores the input offset voltage and output offset voltage will be stored on C_{OC}. C_S should be chosen larger than C_{OC} since it is used for the input offset storage.

III. Simulation Results

The comparator delay with 52 µV voltage difference with respect to the reference voltage is simulated and measured to be 219 ps. This delay can be controlled by the other clocks used in the comparator. Comparator average power consumption at the worst case is 755 µW. The worst comparator delay happens when the input voltage difference is minimum.

An error will occur in the output if the comparator is not able to resolve the next input due to the recovery time needed to discharge the previous state. Overdrive recovery test has been done and the results are shown in Fig. 2. It is obvious from the overdrive recovery test that the comparator can compare two different inputs right after each other without any error.

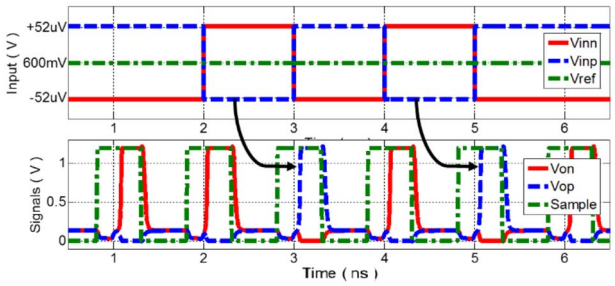

Fig. 2. Comparator overdrive recovery test

The comparator offset rejection performance is assessed by running the Monte Carlo simulation with 500 points iterations. Monte Carlo simulation confirms that the input referred offset voltage is limited to σ_{OS} = 723 µV. Simulated Monte Carlo histogram is demonstrated in Fig. 3.

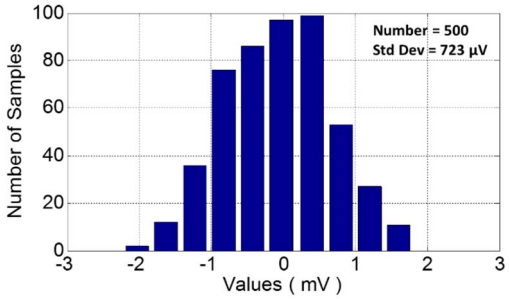

Fig. 3. Monte Carlo simulation

The proposed comparator performance summary is summarized in Table I. Layout of the proposed comparator is shown in Fig. 4.

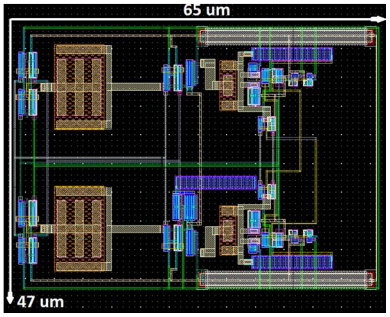

Fig. 4. Proposed comparator layout

TABLE I. Performance Summary

Parameter	Value
Technology	65 nm
Supply Voltage	1.2 V
Average Power @ 1GHz	755 µW
Worst Case Delay (V_{cm}=0.6V, ΔV_{in}=52µV)	219 ps
Offset (σ_{OS})	723 µV
Delay/log(ΔV_{in})	51 ps/dec
Energy Efficiency	0.76 J

IV. Summary

The proposed high-speed, low-offset, low-power comparator has a resolution of 52 µV and a power consumption of 755 µW which make this comparator suitable for high resolution and fast applications. The presented comparator works with a 1 GHz sampling frequency where a dual offset cancellation technique is applied to reduce the offset voltage and kickback noise voltage to the input.

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