Analog Integr Circ Sig Process (2016) 88:43–56
DOI 10.1007/s10470-016-0739-8

A new gain-enhanced and slew-rate-enhanced folded-cascode op amp

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Received: 4 May 2015 / Revised: 1 April 2016 / Accepted: 4 April 2016 / Published online: 10 May 2016

Abstract This paper describes a gain enhancement method and also a slew-rate enhancement scheme for folded-cascode amplifiers which uses positive feedback + transconductance increaser method for the sake of gain increment that gives rise to approximately 21 db of increment in the amount of the gain. An approach for increasing the slew-rate has also been employed which has increased the slew-rate of the amplifier approximately 5 times the conventional folded-cascode one as well as the triple folded-cascode one. Also the settling time and consequently the speed of the circuit is improved remarkably i.e. over 6 times the conventional folded-cascode and triple folded cascode ones. The amplifier has been designed in TSMC RF 0.18 μm and consumes 920 μw of power meanwhile provides 67 db for gain, 581 MHz for UGBW, 69° for phase margin, 793 V/μS for slew-rate and 3.2 nS for large-signal settling time as well as the gain-error of the amplifier for large-signal is approximately 0.5 %. The layout of the circuit has also been carried out in Cadence and demonstrates that the op amp occupies 41 μm × 61 μm (0.002 mil^2) of the die area. The post-layout-simulation of the op amp was also fulfilled and the results are displayed.

Keywords Folded-cascode · Accuracy · Slew-rate · Gain · Compensation · High-speed · CMFB · Layout

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1 Introduction

The operational amplifiers play a crucial role in most of the analog and mixed-signal systems. Depending on the application in which the op amp is employed, the demanding performance for it will be different. For example if the speed is critical while the gain error is not, a topology is chosen that favors the former, possibly sacrifices the latter. Also by scaling the cmos process technology down which consequently lowers the supply voltage, besides the low power demanding and the issues of short channel effects, providing a high gain, high speed, high output swing, etc. despite all of the above-mentioned limitations, asks for new circuit design techniques. Despite its rather medium performance, the folded-cascode topology, is used copiously in a wide range of applications such as those in analog to digital converter, filters, etc. The large signal settling time is the resultant of the UGBW of the amplifier besides the slew-rate of the amplifier and the input capacitances of the op amp also the overdrive recovery (slew-back) time which altogether determine the speed of an amplifier. In high-speed circuits such as ones used in data communication systems or converters, one of the most important features which dominates the function of a data converter circuit is the speed of either of those subcircuits with which the converter is constructed. Moreover the gain of the amplifier is another significant aspect which has to be considered carefully since it has a large impact upon the accuracy and other parameters of the amplifier. Hereat two methods for increasing both the gain and the speed of a conventional folded-cascode (CFC) opamp are demonstrated in this paper [1–4]. There are various schemes in order to enhance the gain of an op amp, however, they are all based on either transconductance or output impedance increment. For the former a technique so-called recycling folded-cascode has been used in [5]. In this method they

reused the existing devices in order to provide higher gain which is similar to the feed-forward technique in a way. For the latter case, we can mention regulated cascode, triple folded-cascode and so forth. For example the repetitive regulated cascode (gain-boosted) technique used in [6] is one of those. Positive feedback can also be used so as to increase the gain of the circuit in either way. i.e. it can increase either the transconductance or the output impedance of the amplifier. Each of the above-mentioned methods has its disadvantageous and advantageous for example in the regulated cascode (gain-boosted) method the power consumption is increased and the output voltage swing is decreased by stacking six transistors atop each other in triple folded-cascode and also in terms of other considerations such as speed, noise, input common mode range and so on. There are some idle transistors in the signal path of which we can take advantage in order to provide additional current signal paths and accordingly larger transconductance. This is the way via which the enhancement of the gain of the amplifier has been accomplished in this paper. Having class AB input stage, a CMOS op amp can provide higher slew-rate values which no longer are limited by the dc bias current of the input stage as are the conventional CMOS op amps [2]. The adaptive-biasing can also be used in order to increase the slew-rate of the op amp [4, 7]. Counteracting the input capacitances by means of neutralization capacitors which are implemented by MOS transistors can be used in order to increase the speed and improve the settling behavior of the circuit as well [2].

The organization of the paper is as follows: In Sect. 2 CFC is described briefly. Section 3 presents the proposed circuit for gain enhancement. Section 4 demonstrates the proposed circuit for slew-rate enhancement. In Sect. 5 the Layout of the op amp is shown. The results of the simulation and PLS are presented in Sect. 6. The paper is concluded in Sect. 7.

2 Folded cascode amplifier

The circuit diagram of a CFC amplifier is shown in Fig. 1. We just describe it briefly, the detailed analysis has been demonstrated in [1]. The overall gain of the amplifier can be calculated as follows:

$$A_V = -G_m \times R_{out} \tag{1}$$

$$G_m = g_{m_{1,2}} \tag{2}$$

$$R_{out} = g_{m_{5,6}} r_{o_{5,6}} \left(r_{o_{3,4}} \parallel r_{o_{1,2}} \right) \parallel g_{m_{7,8}} r_{o_{7,8}} r_{o_{9,10}} \tag{3}$$

The dominant pole and the second dominant pole of the amplifier occur at output node, which is marked with $V_{\text{out}}\pm$ and at folding node i.e. the sources of M5 and M6

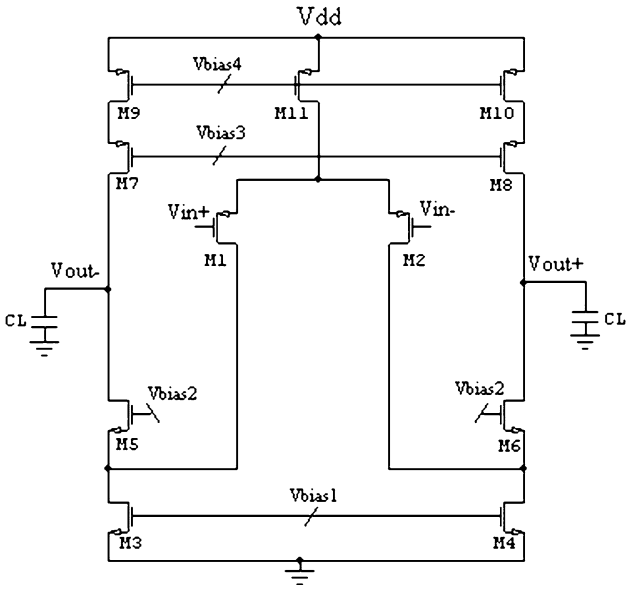

Fig. 1 Coventional folded cascode

transistors respectively. These two poles are calculated as the following equations:

$$P_1 = \frac{1}{C_{out} R_{out}} \tag{4}$$

where the C_{out}, is the total capacitance at the output node and is equal to:

$$C_{out} = C_L + C_{gd5,6} + C_{gd7,8} + C_{db5,6} + C_{db7,8} \tag{5}$$

The second pole takes place at the folding node.

$$P_2 = \frac{1}{R_{fold} C_{fold}} \tag{6}$$

where the R_{fold} and C_{fold} imply the resistance and capacitance seen looking into the folding node respectively and can be written as the following equations:

$$R_{fold} = \frac{1}{g_{m_{5,6}}} \parallel r_{o_{5,6}} \parallel r_{o_{3,4}} \parallel r_{o_{1,2}} \cong \frac{1}{g_{m_{5,6}}} \tag{7}$$

$$C_{fold} = 2C_{gd1,2} + C_{gs5,6} + C_{gd3,4} + +C_{sb5,6} + C_{db1,2} \tag{8}$$

whereas the two coefficient in $C_{gd1,2}$ represents the miller multiplication effect between input and folding nodes. We choose the PMOS input structure for the sake of the lower flicker noise and higher second pole. One can use NMOS input, suffering from higher flicker noise and lower second pole magnitude, obtains more gain because of the higher mobility of electrons. Also it has to be mentioned that the fully differential mode is employed in lieu of the single-ended one because of its well-known features which does not need to be mentioned here again. In order to compensate the op amp one can use the load capacitance as the compensation capacitor that ultimately gives rise to a unity gain frequency which can be calculated as the following:

$$A_v \times p_1 = 1 \times \omega_u \tag{9}$$

$$\text{and then } \omega_u = \frac{g_{m_{1,2}}}{c_{out}} \tag{10}$$

The CFC was designed standalone (without those gain and slew-rate enhancement circuits) and the simulation results of this design are presented in Sect. 5.

3 Proposed gain-enhancement circuit

The proposed gain-enhancement circuit is shown in Fig. 2. As can be seen the two of four added transistors (M_{11}, M_{12}) were connected in cross-coupled positive feedback fashion thereby creating inphase extra current signal paths at the output that results in overall transconductance increment of the amplifier. The current signal at those superimposed transistors (M_{13}, M_{14}) are mirrored by a factor which depends on the W/L ratio of these two transistors to those of the M_9, M_{10} of the op amp itself. The gain analysis of the op amp is described at the following subsection.

3.1 DC gain analysis

Formulating the frequency-contained transfer function may be somehow arduous and time-consuming, hereat in this subsection we introduce the capacitances in neither formulas nor figures and will do the frequency analysis at the subsequent subsection instead. Considering the small signal half-circuit of the circuit and its equivalent model in Fig. 3, the DC gain can be formulated as the following:

$$\frac{v_{out-} - V_1}{r_{o_{5,6}}} + g_{m_{5,6}}(-V_1) = \frac{V_1}{r_{oA}} + g_{m_{1,2}}(v_{in+}) \tag{11}$$

$$\frac{v_{out-} - V_2}{r_{o_{7,8}}} + g_{m_{7,8}}(-V_2) = \frac{V_2}{r_{o_9}} + g_{m_{9,10}}(V_3) \tag{12}$$

$$V_3 \cong \frac{g_{m_{11,12}}}{g_{m_{13,14}}}(-V_1 - V_3) \tag{13}$$

wherein the r_{oA} is rewritten as follows:

$$r_{oA} = r_{o_{1,2}} \parallel r_{o_{3,4}}$$

$$V_1 = \frac{v_{out} g_{ds_{5,6}}}{g_{m_{5,6}}} - \frac{g_{m_{1,2}}}{g_{m_{5,6}}} v_{in+} \tag{14}$$

$$V_2 = \frac{v_{out} g_{ds_{7,8}}}{g_{m_{7,8}}} - \frac{g_{m_{1,2}} g_{m_{9,10}}}{g_{m_{5,6}} g_{m_{7,8}}} \beta v_{in+} \tag{15}$$

$$V_3 = -\beta V_1 \tag{16}$$

whereas g_{ds} is representative for the output transconductance of transistors and the β is given by the following equation: $\beta = \frac{g_{m_{11,12}}}{g_{m_{11,12}} + g_{m_{13,14}}}$. By writing another KCL we can solve the equations:

$$V_2 g_{ds_{9,10}} - g_{m_{9,10}} V_1 \beta = -V_1 g_{dsA} - g_{m_{1,2}} v_{in+} \tag{17}$$

For the sake of brevity, we abridge the results, thereby Simplifying the above equations and keeping in mind that $g_m r_o \gg 1$ yield:

$$A_V = \frac{v_{out\mp}}{v_{in\pm}} = \frac{v_{out+} - v_{out-}}{v_{in+} - v_{in-}} \tag{18}$$

$$\frac{-g_{m_{1,2}}\left[g_{m_{9,10}} g_{ds_{9,10}} \beta + g_{m_{7,8}} g_{dsA} + g_{m_{7,8}} g_{m_{9,10}} \beta\right]}{g_{m_{5,6}} g_{ds_{7,8}} g_{ds_{9,10}} + g_{m_{7,8}} g_{ds_{5,6}} g_{dsA} - g_{m_{7,8}} g_{m_{9,10}} g_{ds_{5,6}} \beta}$$

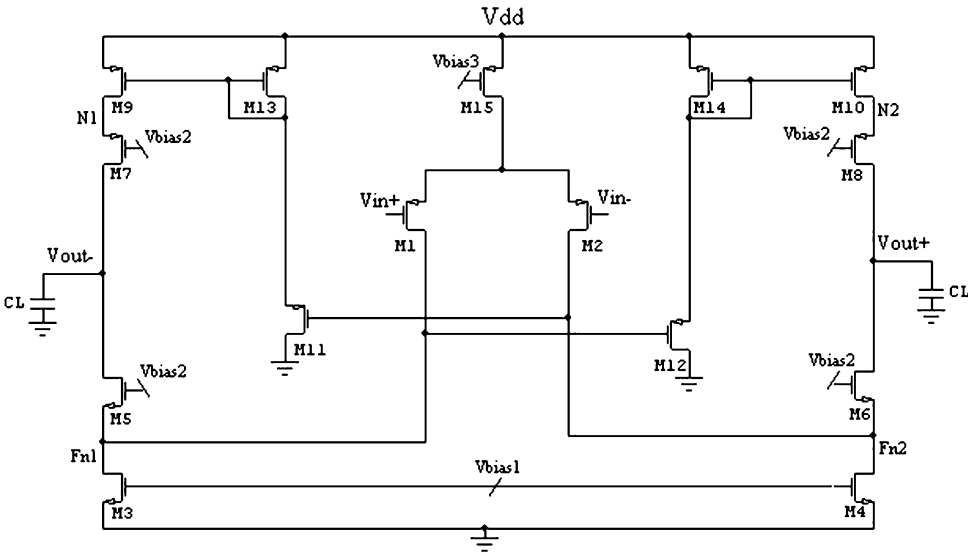

Fig. 2 Proposed gain-enhancement circuit

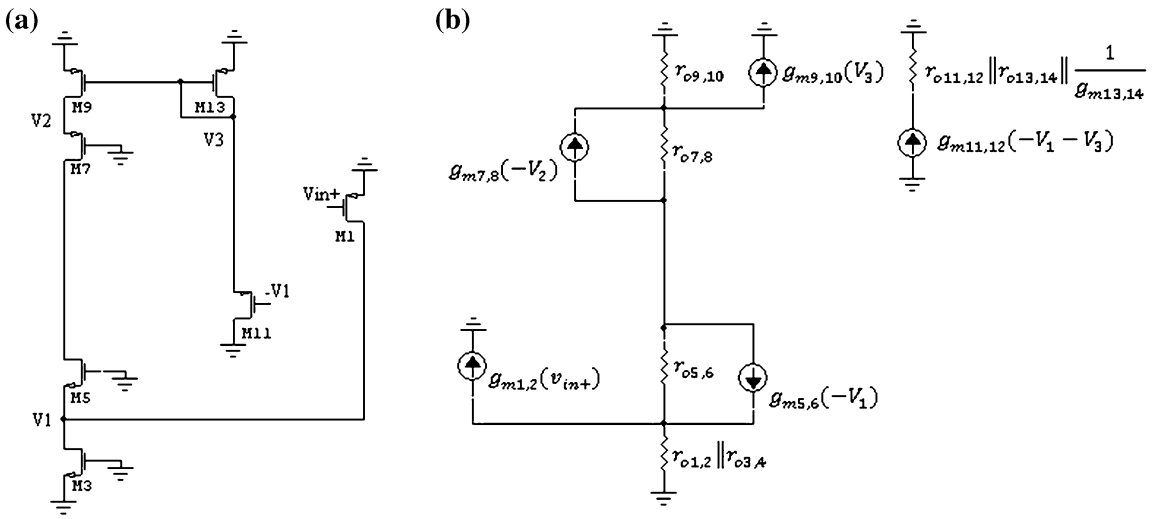

Fig. 3 **a** Small signal half-circuit. **b** Equivalent model of **a**

Since the denominator consists of output transconductances squared whereas the nominator is a multinomial containing transconductances squared and as we know the latter is approximately too many fold greater than the former in a typical design, and having a subtraction term at the denominator, we can manage the design i.e. the aspect ratio of transistors, in a way to achieve very high values for the gain but the caution should be taken into account so as to prevent negative gain values from being taken at the corners of the process or temperature, supply and other process variations.

3.2 Frequency response

As those excess transistors only add one low impedance node i.e. the $\pm V_3$ node in Fig. 3(a), and the capacitance at this node is much less than the output capacitor hereby contributing a pole beyond the unity-gain frequency, have no significant impact on the frequency response by comparing it with CFC. The two most dominant poles occur at the same nodes as do the CFC ones. The third one takes place at the node named V_2 and the fourth at node designated as V_3. We can write down those resistances and capacitances seen looking across those afore-mentioned nodes respectively in such a manner:

$$R_{out} = R_{up} || R_{down}$$

$$R_{up} = \frac{g_{m_{5,6}} g_{m_{7,8}}}{g_{m_{5,6}} g_{ds_{7,8}} g_{ds_{9,10}} - g_{m_{7,8}} g_{m_{9,10}} g_{ds_{5,6}} \beta} \tag{19}$$

$$R_{down} = g_{m_{5,6}} r_{o_{5,6}} \left(r_{o_{3,4}} \parallel r_{o_{1,2}} \right)$$

$$R_{V_2} \cong \frac{1}{g_{m_{7,8}}} \tag{20}$$

$$C_{V_2} = C_{gs_{7,8}} + C_{sb_{7,8}} + C_{gd_{9,10}} \left(1 + \frac{g_{m_{7,8}}}{g_{m_{9,10}}} \right) + C_{db_{9,10}}$$

$$R_{V_3} \cong \frac{1}{g_{m_{11,12}}} \parallel \frac{1}{g_{m_{13,14}}} \tag{21}$$

$$C_{V_3} = C_{gs_{9,10}} + C_{gs_{13,14}} + C_{sb_{11,12}} + C_{db_{13,14}} + C_{gs_{11,12}} \left(1 - \frac{1}{\beta} \right) + C_{gd_{9,10}} \left(1 + \frac{g_{m_{9,10}}}{g_{m_{7,8}}} \right)$$

The output capacitances, folding node resistance and capacitances are given by (5), (7) and (8) respectively, except that two capacitances $C_{gd_{11,12}}$ and $C_{gs_{11,12}}(1-\beta)$ have to be added to the folding node capacitances. The first dominant pole and the second one are given by (4) and (6) of course by replacing the output resistance and folding node capacitances by the new ones i.e. (19) and adding the two extra capacitances to the folding node ones. The third and fourth poles are yielded as follows:

$$P_3 = \frac{1}{C_{V_2} R_{V_2}}, \quad P_4 = \frac{1}{C_{V_3} R_{V_3}} \tag{22}$$

The C_L has been added in order to compensate the frequency response for reasonable phase margin to prevent the circuit from instability and oscillation. The amount of 250 fF has been chosen in this design. Again we have to be careful in allocating the device dimensions, because it may result in negative R_{up} (19) either in corners or by process and temperature and supply variations and stability issues thereof incur. Abstaining lengthiness and complexity, the g_{mb} of all transistors have been neglected in all formulas and calculations.

4 Proposed slew-rate enhancement circuit

As already mentioned there are some techniques in order to cope with dc bias limitations for the slew-rate of an op amp. The method which has been proposed in this paper

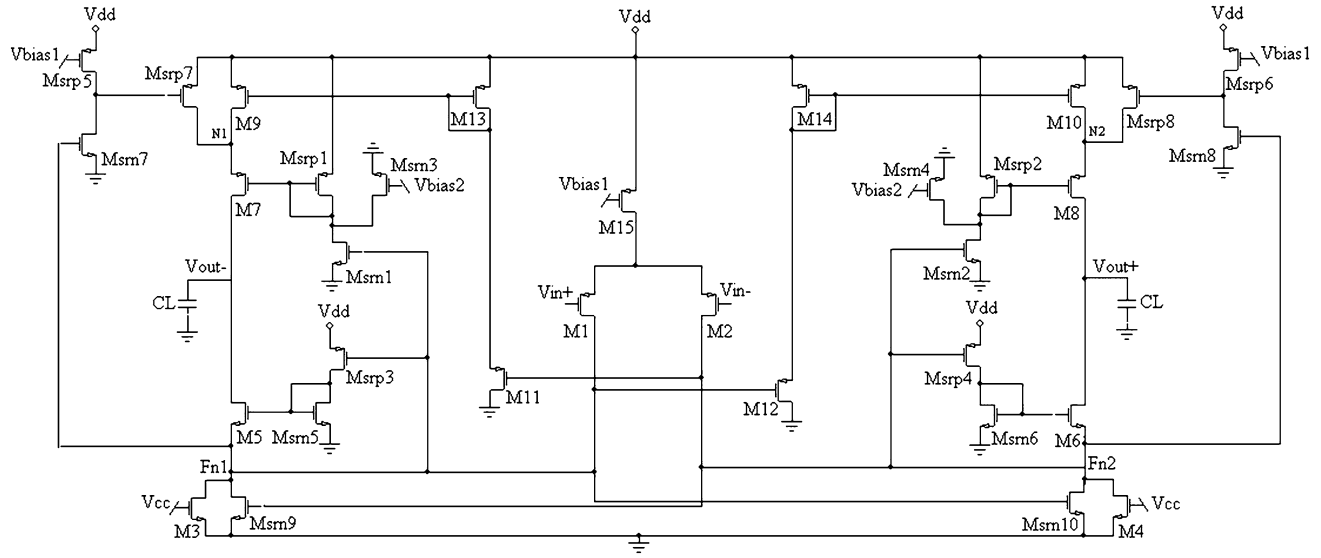

Fig. 4 Proposed gain-enhanced and slew-rate-enhanced circuit

provides dynamic biasing for the cascode transistors in slewing duration of the opamp which increases the slew-rate drastically. The proposed circuit is shown in Fig. 4. Among these extra transistors the $M_{srp_{7,8}}$ and $M_{srn_{1,2,7,8,9,10}}$ will be off at the normal i.e. small signal or linear operation of the circuit, thus contribute neither noise to the overall noise of the op amp nor excessive capacitances to the interconnected relevant node, but will be on at the slewing interval hereby providing extra large currents for the output capacitance, increase the slew-rate considerably. The operation of the circuit, in slewing cycle is as follows: by decreasing the input (v_{in+}) voltage level to very large negative value (or by applying a step with a very large negative amplitude) the folding node voltage (F_{n_1}) is increased dramatically and turns the $M_{srn_{1,7,10}}, M_{srp_7}$ transistors on. By turning the M_{srn_1} on, drain voltage of this transistor drops effectively and this action, in turn, gives rise to considerable decrement at the gate voltage of the M_7. On the other hand the M_{srn_7} is located at the same circumstances as the M_{srn_1} thereby dropping its drain voltage turns the M_{srp_7} on and pulls the drain voltage of M_{srp_7} up. All the above procedure results in drastically reduction in the gate voltage of M_7 and increment in the source voltage of this transistor, which means the M_7 carries a very large amount of current. This current flows through the output capacitance thereby increasing the positive slew-rate of the circuit drastically. The size of M_{srp_5} has been chosen in a manner that provides a voltage with a very high level, i.e. so close to supply voltage, for the gate of the M_{srp_7} when the M_{srn_7} is off, hereat this transistor will be completely off at the normal operation of the circuit. At the same time the other folding node (F_{n_2}) voltage is decreased which leads to increment of the drain voltage of M_{srn_6} transistor (gate voltage of M_6). Since the F_{n_1} voltage is increased the $M_{srn_{10}}$ turns on and pulls the F_{n_2} voltage down even more. By dramatically increment in its gate voltage and decrement in its source voltage, the M_6 transistor will carry a huge amount of current hereby provides a large current for the output capacitor to be discharged through. This gives rise to drastically increment in the negative slew-rate of the op amp. The aspect ratio of $M_{srn_{2,4}}$ and M_{srp_2} are chosen in a way that cater a signal-independent bias voltage for the M_8 in the normal operation of the circuit, but the bias voltage of the M_5 will be varied a little bit in normal operation, but this variation is negligible and has no impact on the normal operation of the circuit, As well as it has a little impact on the gain and output impedance of the circuit and this can be included by substituting the $\gamma g_{m_{5,6}}$ for $g_{m_{5,6}}$ in (18) and (19) wherein $1<\gamma<2$. Also because of applying this scheme to the circuit, in output capacitance and folding node capacitance calculation at the previous section, the $C_{gs_{5,6}}$ and $C_{gd_{5,6}}$ get a miller coefficient and other equations and discussions for gain and frequency response will be the same as were for the circuit without slew-rate-enhancement technique. The same discussion can be applied for the counterpart transistors of the above-mentioned ones at the next excursion of the input signal. Incidentally it has to be mentioned that the gain-enhancement scheme also increases the slew-rate somewhat but not as much as the slew-rate-enhancement circuit does. In fact this increment with respect to the slew-rate-enhancement approach increment is minuscule. Also the V_{cc} is the controlling voltage which comes from the CMFB circuit and will be explained at the next subsection.

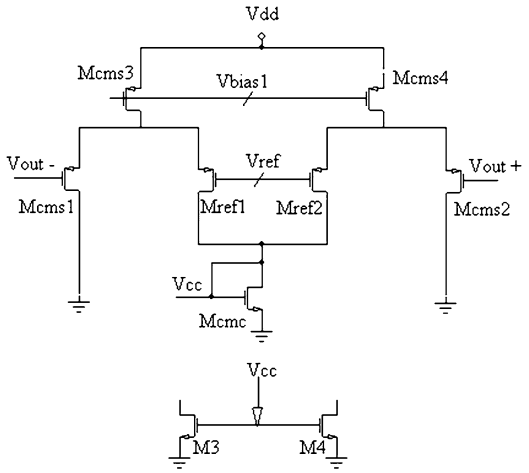

Fig. 5 CMFB circuit

4.1 CMFB circuit

The CMFB circuit which has been used for this op amp is the traditional DDA (differential difference amplifier) which is shown in Fig. 5 and can be found in [2, 3].

The stability of the CMFB circuit is one of the most important issues which has to be considered carefully. Turns out, the load capacitor used for differential-mode compensation, is able to provide enough phase margin for CMFB circuit as well.

4.2 Output voltage swing and ICMR

The extra added circuits do not engender any restriction on the swing of the output voltage, and the output voltage swing of the proposed op amp is the same as the CFC one i.e. $V_{dd} - 4V_{dsat}$. The input common mode range (ICMR) is also the same as the CFC one.

4.3 Noise analysis

The PMOS input structure has been chosen in order to reduce the flicker noise of the circuit. Comparing the proposed circuit with CFC, the noise of the proposed circuit is more than the noise of the CFC but it's not the case to be concerned about because the gain of the proposed circuit is large enough to counteract all the detriments stemmed from those augmented transistors thereby reducing the input-referred noise to a very small value in comparison with the CFC one.

4.4 CMRR

In common-mode operation the folding nodes will be inphase, therefore the CM gain of the proposed circuit will become less than the CM gain of the CFC, on the other hand the DM gain of the former is much more than the latter, then the CMRR of the proposed circuit can be construed to be much more than the CMRR of CFC.

4.5 Speed and gain error considerations

By comparison the proposed circuit with the CFC, it has some additional nodes that have some impact on the frequency response of the circuit. But as already mentioned, having low impedance and low capacitance, these nodes add poles far beyond the UGBW, since the slew-rate of the proposed one is approximately 5 times more than the CFC one, then improves the speed performance of the circuit to superior levels than the CFC does. The gain-error of the circuit is also improved because of the gain increment which in turn improves the accuracy of the circuit. The settling time formulization can be done as follows:

$$T_{s_{total}} = T_{ss} + \frac{\Delta V}{SR} + T_{init} + T_{ov} \tag{23}$$

wherein the $T_{s_{total}}$ is the total settling time for a large signal applied to the input and in this case is a pulse with 1.4Vp-p of amplitude which ΔV is indicator of that, the SR is the slew-rate, T_{ov} is the time it takes for the amplifier to recover from the slewing regime and finally the T_{init} implies the time squandered on behalf of the op amp nonidealities, such as input capacitances of the op amp and all other parasitic capacitances at the input of the op amp or propagation delay arising from digital signals switching interval in data converters in which there is no or very small variation at the output signal in spite of the input large variation. Having ambiguous turn on and turn off point for the input transistors [1] and other slew-involved transistors, finding the latter two are somewhat arbitrary and can't be that straightforward or accurate to be calculated by hand-calculation. The former two can be calculated roughly as the following manner:

$$\tau = \frac{1}{\beta \times \omega_u} = \frac{1}{2 \times \pi \times 1 \times 581\ \text{MHz}} = 0.27\ \text{nS}$$

$$T_{ss} = \tau \ln \frac{1}{e_{ss}} = 0.27\ \text{nS} \times \ln \frac{1}{0.01} = 1.24\ \text{nS}$$

$$\frac{\Delta V}{SR} = \frac{1.4\ V}{793 \frac{V}{\mu S}} = 1.77\ \text{nS}$$

Wherein τ is the time-constant of the folded-cascode amplifier, β is representative for the feedback factor of the unity-gain closed-loop configuration [3] and regarding Fig. 7 it is unity and e_{ss} implies the settling-error or accuracy of the amplifier and in this case is supposed to be 1 %. Of course the evaluated time for slewing is smaller in practice, the reason why, is that the output does not go the total amplitude range through the slewing duration which

means the ΔV becomes smaller and so does the slewing time. The overall settling time obtained from the simulation is 3.2 nS.

5 Layout

Layout of the op amp was performed in Cadence and is presented in Fig. 6. As can be seen the area which is taken up by the op amp is 41 μm × 61 μm (0.002 mil^2). It is worth mentioning that since the transistors are laid out in multi-finger manner even the results of the pre-layout-simulation (PreLS) and the Hspice simulation of the circuit show a little bit discrepancy with respect to each other. A comparison was made and results are demonstrated in Table 1.

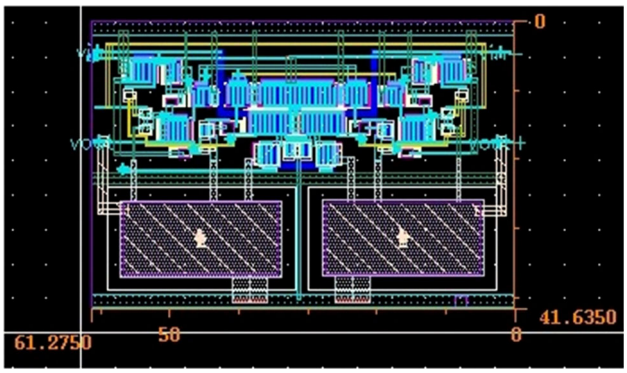

Fig. 6 Layout of the proposed op amp

6 Simpulation results

The proposed circuit and also the CFC, triple folded cascode (TFC) and the op amp demonstrated in [5] have been designed in TSMCRF 0.18 μm, and simulated with HSPICE, Model BSIM (V3.24), Level 49. The simulation results confirm all the analysis based on inspection and theory that already mentioned. The supply voltage is 1.8v and the total power consumption of the whole circuit is 920 μwatt (Fig. 7). The load capacitors and their counterparts have been chosen exactly alike in the proposed circuit and the CFC and also the TFC but the op amp depicted in [5] needed larger load capacitance to be compensated. Also the post-layout-simulation of the proposed op amp has been

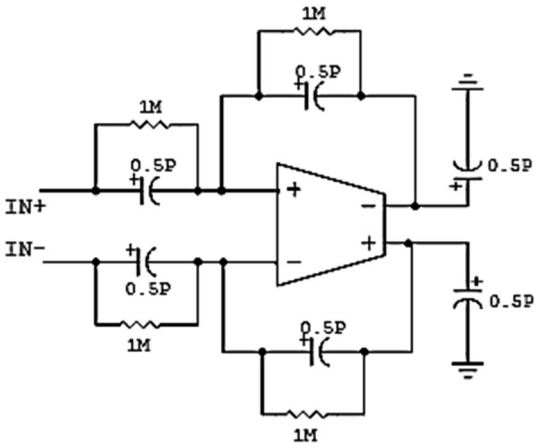

Fig. 7 Closed-loop unity-gain configuration used for setting time and linearity simulation

Table 1 Performance specification comparison of the proposed op amp at different circumstances

Parameter	HSPICE	PreLS (multifinger)	PLS
DC gain (db)	67	66.6	67.7
UGBW (MHz)	581	550	482
Phase margin (°)	69	72	65
CL (fF)	250	250	250
Slew rate (V/μs) (V_{outp-p} = 1.4 V) (CI = 0.5 PF, CL = 250 fF)	793	731	691
Settling time (ns) (V_{outp-p} = 1.4 V) (l %) (CL = 0.5 PF, CI = 250 fF)	3.2	3.2	3.6
Thd (f = 1 MHz, V_{outp-p} = 1 V) (db) (CL = 0.5 PF, Cl = 250 fF)	−83	−84	−82
Thd (f = 4 MHz, V_{outp-p} = 1 V) (db) (CL = 0.5 PF, Cl = 250 fF)	−79	−72	−71
Thd (f = 1 MHz, V_{outp-p} = 1.6 V) (db) (CL = 0.5 PF, Cl = 250 fF)	−61	−57	−54
Thd (f = 1 MHz, V_{outp-p} = 0.2 V) (db) (CL = 0.5 PF, Cl = 250 fF)	−105	−111	−105
Input offset voltage (mV)	–	–	0.032
Power supply (V)	1.8	1.8	1.8
Power consumption (μwatt)	920	896	872
Process technology (μm)	0.18	0.18	0.18
Output voltage swing (V_{outp-p}) (V)	2 (Vdd-4Vdsat)	2 (Vdd-4Vdsat)	2 (Vdd-4Vdsat)
Gain error (%) (V_{outp-p} = 1.4 V)	0.5	0.4	0.4

done. The frequency response simulation of the proposed op amp as well as the CFC, TFC and also the RFC (the op amp in [5]) is shown in Fig. 8(a). As seen the gain of the proposed circuit is 67 db, the UGBW is 581 MHz and the phase margin is 69°, these results have been achieved for a load capacitor of 0.25 PF. The frequency response of the proposed op amp for both PLS and PreLS is shown in Fig. 8(b). As can be seen, in PLS the gain of the op amp is

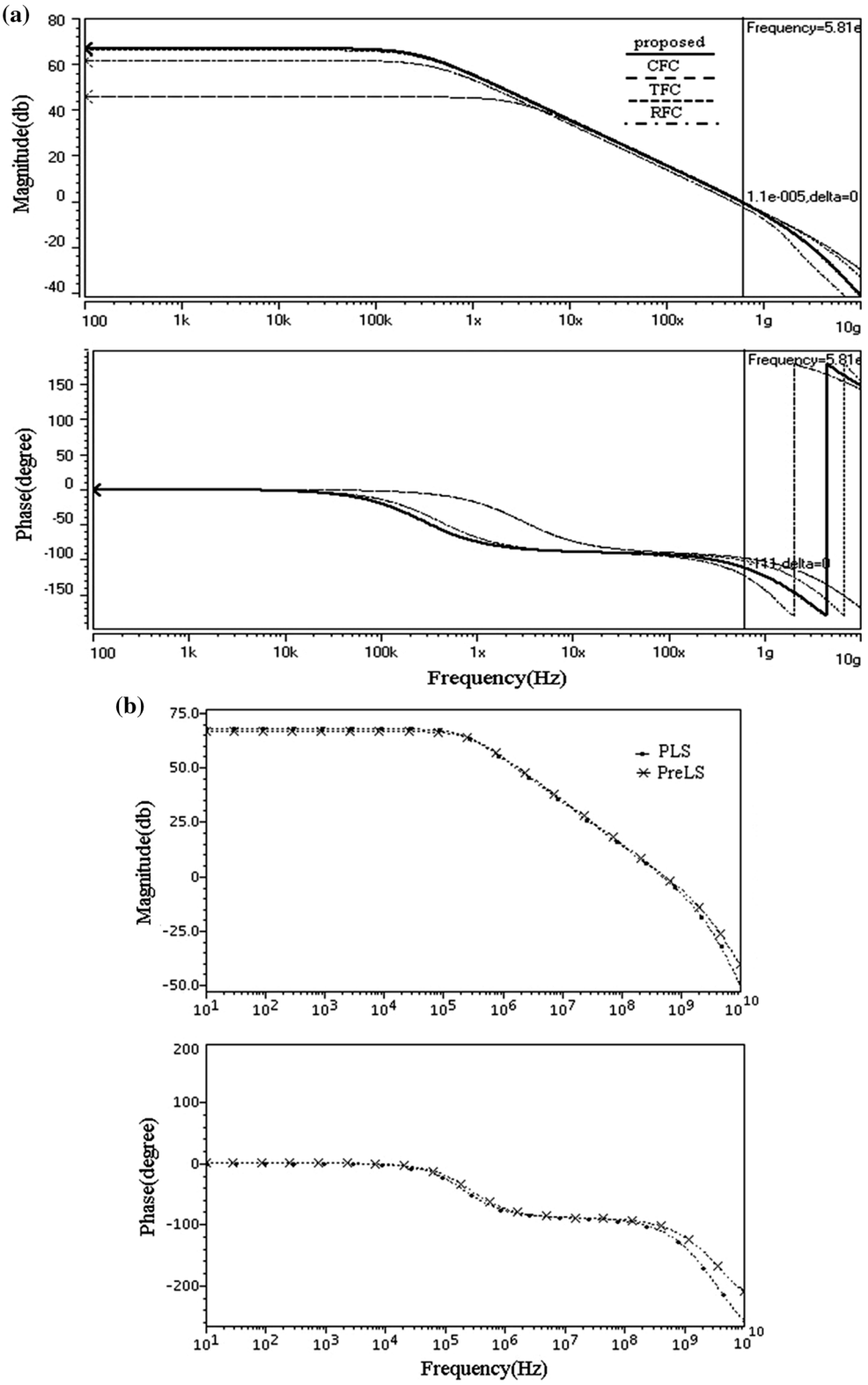

Fig. 8 **a** Frequency response of the proposed op amp and CFC, TFC and RFC. **b** Frequency response of the proposed op amp

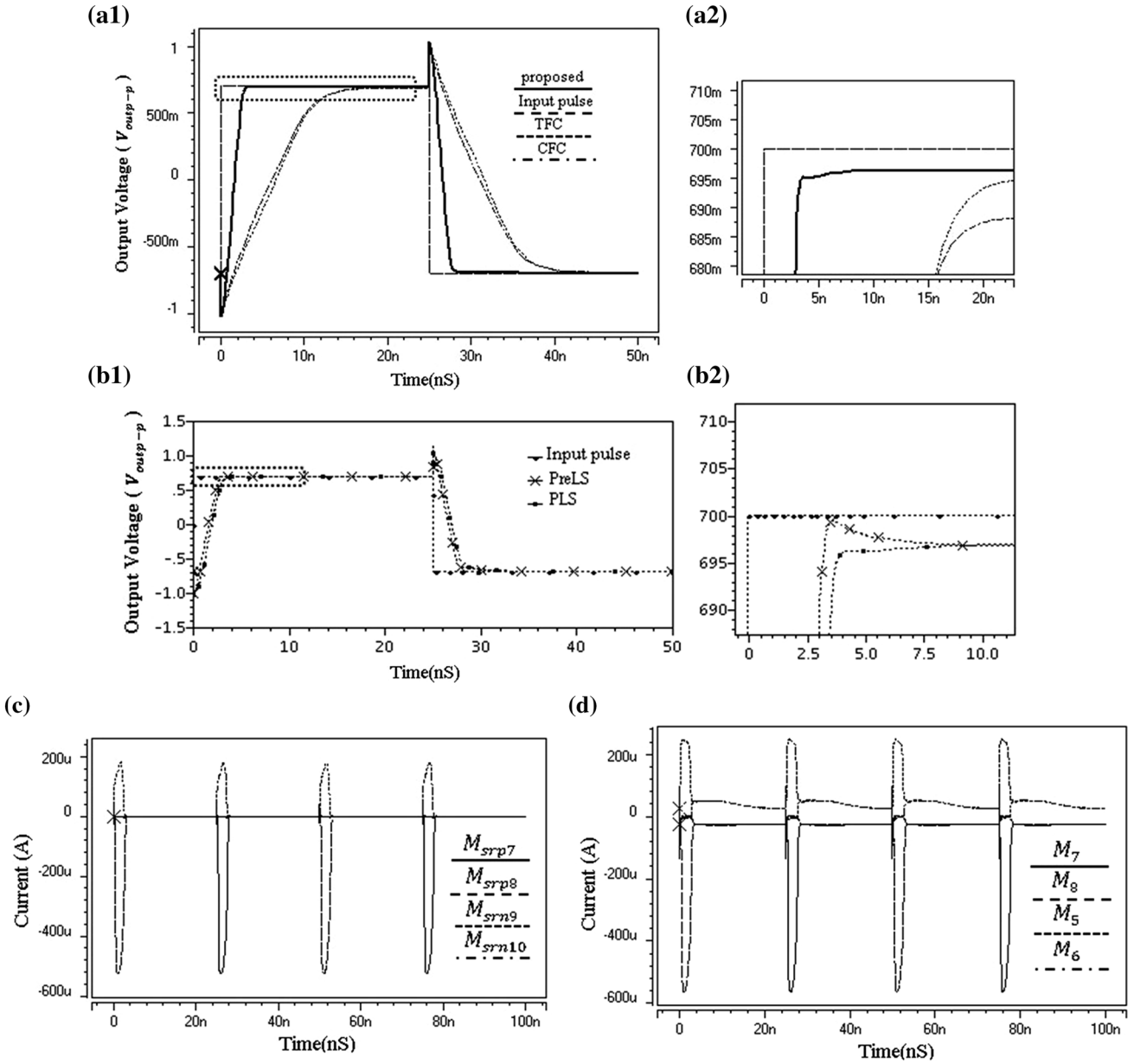

Fig. 9 **a1** Time response of the proposed op amp, CFC and TFC to 1.4 V input pulse. **a2** Magnified version of dashed region of (**a1**). **b1** Time response of the proposed op amp to a 1.4 V input pulse. **b2** Magnified version of dashed region of (**b1**). **c** Transient currents in slewing duration. **d** Transient currents in slewing duration

increased by 1.1 db, the UGBW is decreased by 12 % and the PM is decreased by 0.7° therefore the resulting gain, UGBW and PM after PLS are 67.7 db, 482 MHz and 65° respectively and this comparison is between the PreLS and PLS and in cadence for multi-finger devices. A comparison among the Hspice and Cadence simulation results for both PreLS and PLS has been made for all performance characteristics of the op amp and the results are presented in Table 1. The unity-gain closed-loop configuration depicted in Fig. 7. is used for transient response and linearity simulations. The time response simulation results for an input pulse signal with an amplitude of 1.4Vp-p are illustrated in Fig. 9(a). As it is clear the slew-rate is increased up to 793 V/μS for the proposed op amp. This is expressive of five-fold increment over the CFC and TFC ones. The magnified version of the required region for settling time measurement is demonstrated as well which implies that the 1 % settling time for the proposed op amp is 3.2 nS and this time is one-sixth the CFC and TFC ones. Having single-ended structure, the settling behavior of the RFC is simulated for an amplitude of 1.1 V (250 mv–1350 mv) which displays 15 ns for settling-time and 136 V/μS for slew-rate. The PLS time response results in Fig. 9(b) display that the settling time is increased by 0.4 nS and the SR

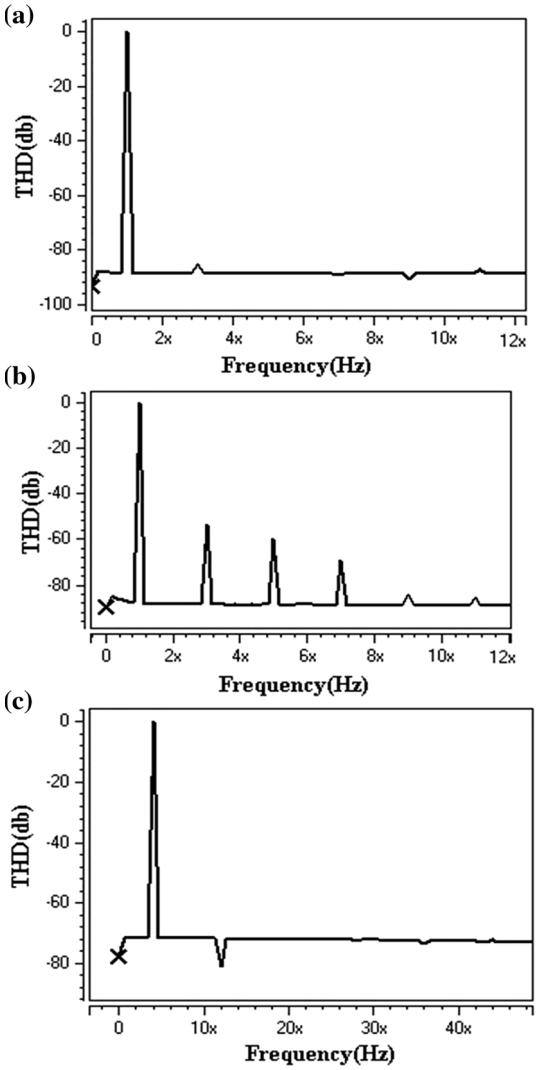

Fig. 10 **a** Thd of the proposed op amp for an input signal with F = 1 MHz and $V_{outp-p} = 1\ V$. **b** Thd of the proposed op amp for an Input signal with F = 1 MHz and $V_{outp-p} = 1.6\ V$. **c** Thd of the proposed op amp for an input signal with F = 4 MHz and $V_{outp-p} = 1\ V$

in decreased by 5 % which results in 3.6 nS for settling time and 691 V/μS for SR (again, the comparison is between PreLS and PLS in cadence and for multi-finger devices). The transient currents for the proposed circuit in slewing period are also shown in Fig. 9(c, d). The THD of the proposed op amp for 1Vp-p of output amplitude and also for 1 MHz and 4 MHz frequencies are displayed in Fig. 10. A comparison among the THD of the proposed op amp and the other three at 1 MHz and for various input

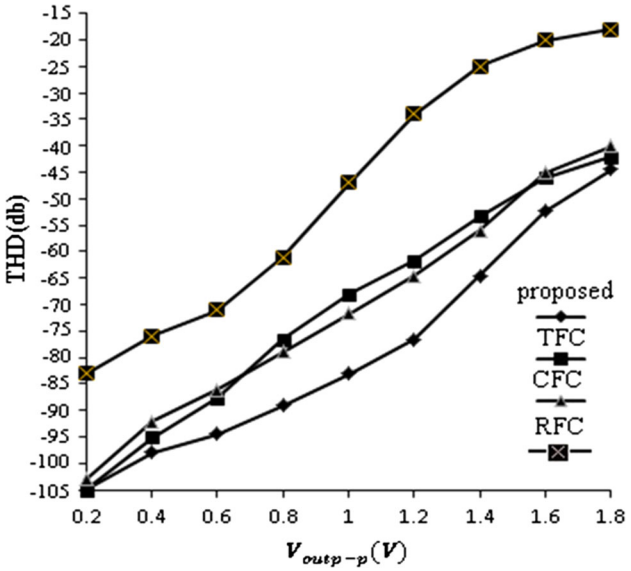

Fig. 11 Thd comparison of four op amps for F = 1 MHz in different input signal amplitudes

signal amplitudes was also made and the graphical delineation is depicted in Fig. 11 and as already mentioned the circuit shown in Fig. 7 is utilized for THD simulations. The frequency response of the proposed op amp for different supply voltages and also different temperatures were also done and the results are shown in Fig. 12. Maximum variation range for vdd is 300 mv and for temperature from −60° to 140°. The first two have been done in Hspice and the second two are the PLS results which have been done in Cadence. The time-response was also simulated for vdd variations and the results are depicted in Fig. 13. The Thd of the proposed op amp was also simulated for both the supply and temperature variation and the range of the variation for both is again 300 mv for vdd and from −60 to 140 for temperature. All the results are for PLS. A comparison between the Thd of the proposed op amp for PLS and PreLS was made and all the results are delineated in Fig. 14. The Input offset of the proposed op amp after layout is measured and the value for that is 32 μV. The CM response of the proposed op amp for full range variation in the input CM voltage i.e. from zero to vdd were also performed. This simulation is for both the input CM pulse and input CM DC voltage. Also similar simulation was carried out in PLS and the results are the same as the Hspice one.

The results are presented in Fig. 15. As it is clear from this figure for full range variation of input C-M voltage the

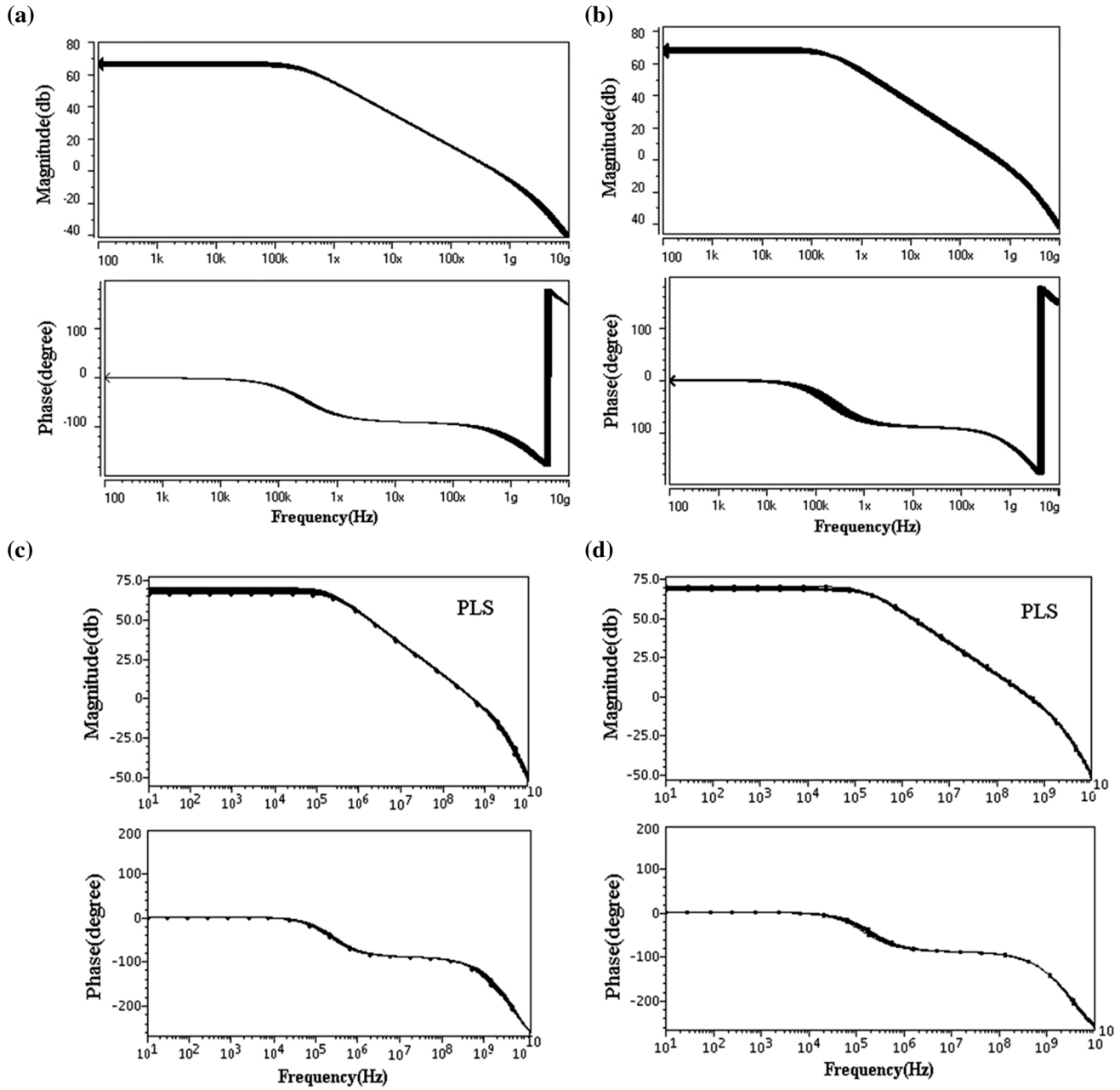

Fig. 12 **a** Frequency response of the proposed op amp for vdd variation (maximum variation is 300 mv). **b** Frequency response of the proposed op amp for temperature variation from −60° to 140°. **c** Frequency response of the proposed op amp for vdd variation (maximum variation is 300 mv). **d** Frequency response of the proposed op amp for temperature variation from −60° to 140°

variation at the output CM range is 8 %. The proposed circuit was simulated at worst-case corners and the results are as follows, in SS corner (140°) the gain and THD are increased 1 and 5 db, the UGBW, PM and SR are decreased 21 %, 3° and 26 % respectively and the large-signal settling time is increased to 8.2 nS. In FF corner (−40°) the gain is decreased 13 db, the UGBW, PM are increased 16 % and 4°, the SR and THD are decreased 27 % and 1 db respectively. The gain-error at all corners is 0.6 %, by the way by increment in THD we mean

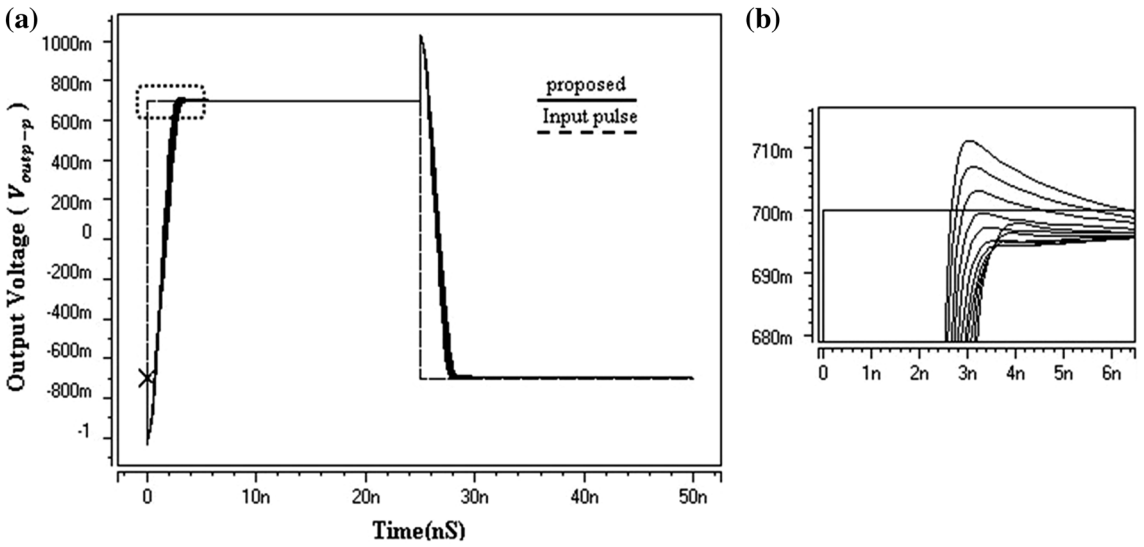

Fig. 13 **a** Time response of the proposed op amp to 1.4 V input pulse for vdd variation (maximum variation is 200 mv). **b** Magnified version of dashed region of (**a**)

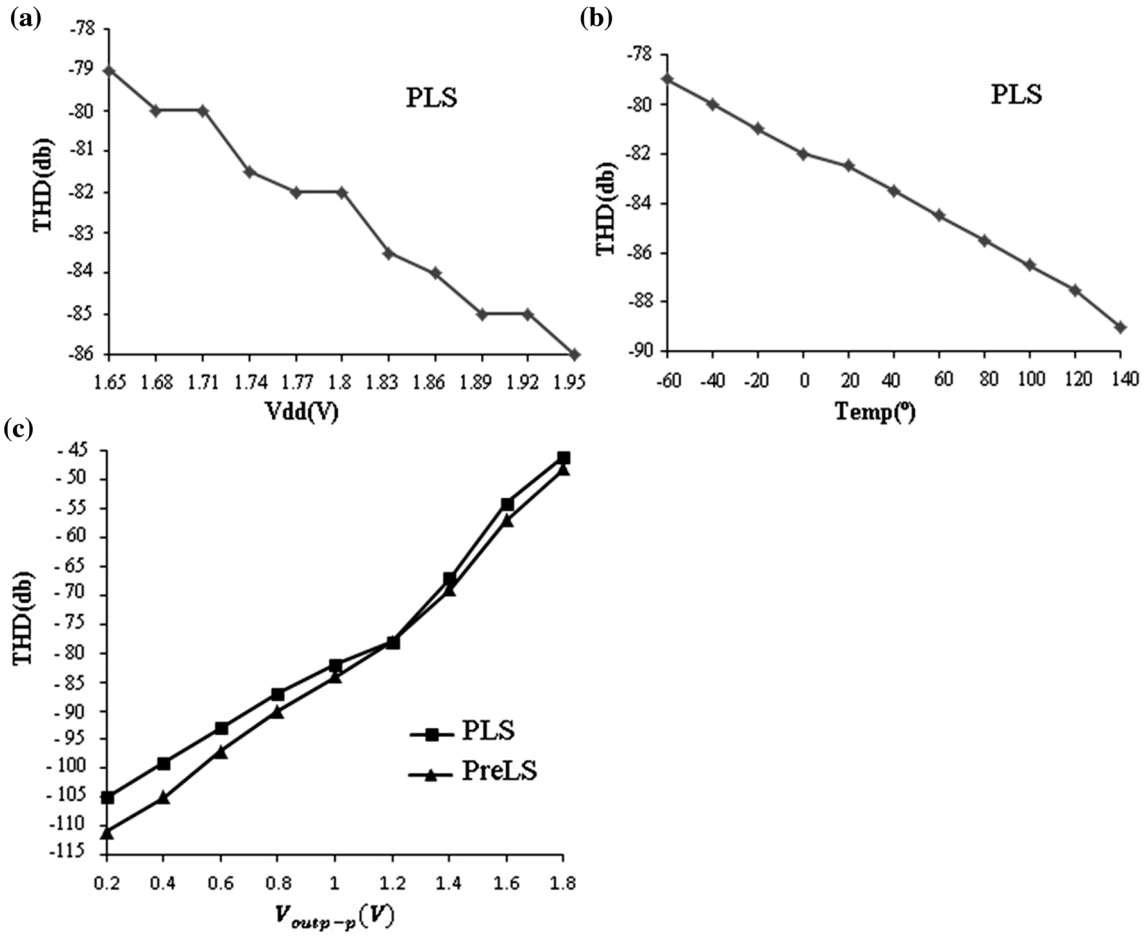

Fig. 14 **a** Thd variation of the proposed op amp for F = 1 MHz and $V_{outp-p} = 1$ V at different supply voltages. **b** Thd variation of the proposed op amp for F = 1 MHz and $V_{outp-p} = 1$ V for temperature variation from −60° to 140°. **c** Thd comparison of the proposed op amp for F = 1 MHz in different input signal amplitudes

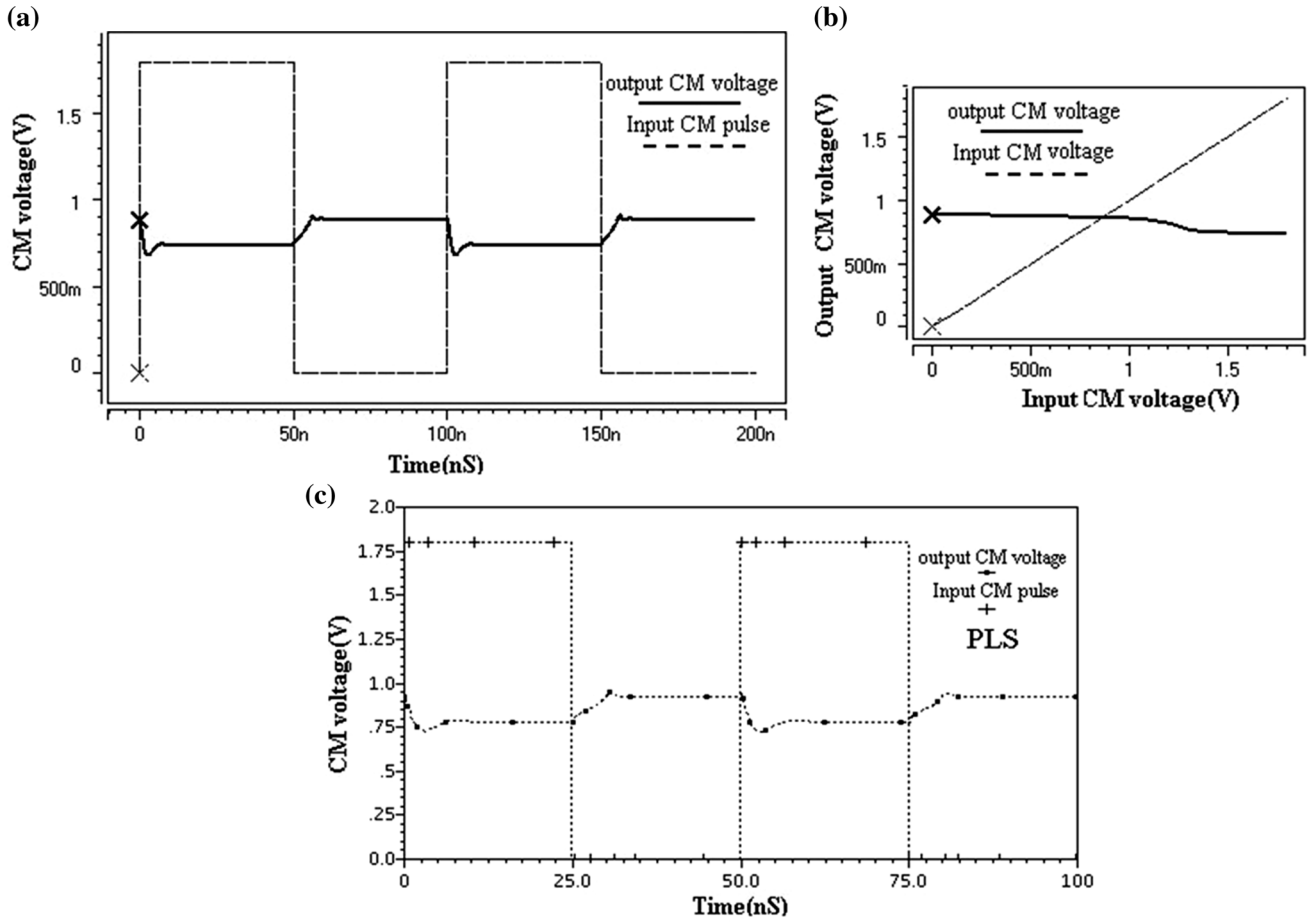

Fig. 15 **a** Output CM variation for a 0–1.8 V input pulse. **b** Output CM variation for a 0–1.8 V DC input signal. **c** Output CM variation for a 0–1.8 V input pulse

Table 2 Performance specification comparison of the proposed op amp and comparison with other op amps

Parameter	Proposed	TFC	CFC	RFC [5]	[8]
DC Gain (db)	67	66.3	46	61.7	00
UGBW (MHz)	581	581	581	475	11.8
Phase margin (°)	69	80	83	65	55
CL (fF)	250	250	250	2300	30,000
Slew rate (V/μs) ($V_{outp-\ p} = 1.4$ V) (CI = 0.5 PF, CL = 250 fF)	793	147	135	142**	35/26***
Settling time (ns) ($V_{outp-\ p} = 1.4$ V) (1 %) (CI = 0.5 PF, CL = 250 fF)	3.2	19.7	21.3*	15**	–
Thd (f = 1 MHz, $V_{outp-\ p} = 1$ V) (db) (C1 = 0.5 PF, CL = 250 fF)	−71	−69	−71	−47	–
Thd (f = 4 MHz, $V_{outp-\ p} = 1$ V) (db) (C1 = 0.5 PF, CL = 250 fF)	−79	−69	−75	−37	–
Power supply (V)	1.8	1.8	1.8	1.8	±5
Power consumption (μwatt)	920	920	920	920	12,500
Process technology (μm)	0.18	0.18	0.18	0.18	2
Output voltage swing (V_{out-p}) (V)	2(Vdd-4Vdsat)	2(Vdd-6Vdsat)	2(Vdd-4Vdsat)	Vdd-3Vdsat-|VTH|	–
Gain error (%) ($V_{out-p} = 1.4$ V)	0.5	0.7	1.7	0.55**	–

* For 1.7 % settling-error; ** For an input pulse with 1.1 V amplitude; *** They mentioned up and down values for slew-rate

improvement and vice versa, i.e. by considering the absolute value of THD. At last the performance specification of the proposed op amp and also the other three are summarized in Table 2.

7 Conclusion

A gain-enhanced and slew-rate-enhanced folded-cascode amplifier was presented in which the cascode devices are used in order to provide additional signal currents at the output thereby increasing the gain of the amplifier, and the idea of dynamic-biasing has been used so as to increase the currents in slewing regime that increases the slew-rate of the amplifier to superior levels than the CFC and TFC do which in turn decreases the settling time hereby improving the speed of the op amp. The proposed scheme decrease the slew-back (over drive recovery) time as well. The total gain of the op amp is 67 db, the unity-gain-bandwidth is 581 MHz and the phase margin is 69° meantime it provides 793 V/μS for slew-rate and 3.2 nS for large-signal settling time. The layout of the whole circuit was also done and the above-mentioned parameters in PLS are 67.7 db, 482 MHz, 65°, 691 V/μS and 3.6 nS respectively which implies that first of all we have to compare the results for PreLS and PLS because of utilizing multifinger devices for the sake of gate electrode resistance decrement on behalf of lowering the noise and also having more efficient area saving than it would be with single-finger devices which gives rise to a little discrepancy even between the Hspice results and PreLS results with multifinger devices in Cadence. Second of all if we consider the performance of the op amp in terms of gain, after layout it is improved by 1.1 db, however in terms of the speed it is decreased only by 0.4 nS, which is expected to. The linearity variation after layout is so small that can be ignored. The overall power consumption of the op amp is 872 μW in PLS and 912 μW in Hspice which indicates of 4 % decrement in power dissipation. The input offset of the proposed op amp is 32 μV.

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