A Single Switch High Step up DC-DC Converter Based on Quadratic Boost

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***Abstract*—This paper proposes a novel high step-up non-isolated single switch DC-DC converter suitable for regulating DC bus in various micro sources especially for PV sources. Quadratic boost and switched-capacitor technique are used as primary and secondary circuit, respectively. The coupled inductor is applied to connection between them, so high DC voltage gain is achieved. High efficiency is yield where voltage stress on active switch is alleviated by clamped capacitor, consequently, smaller $R_{DS(ON)}$ for power switch is required. On the other hand, input current of proposed converter is continued, hence stress on the input source is reduced. The operating principles and steady-state analyses are discussed in detail for both continues and discontinuous conduction mode. Also, the boundary condition is computed. To verify the performance of the proposed converter and theoretical calculations, a 250W prototype converter is implemented with an input voltage 24V and output voltage 400V designed especially for PV sources in CCM operation. Finally simulation results are confirmed by experimental results; maximum efficiency is occurred in 150 W and full-load efficiency is 92.96%.**

***Index Terms*—Coupled inductor, high gain, DC-DC converter, renewable energy.**

I. Introduction

NOWADAYS, using renewable sources of energy is more and more expanded all over the world. Some of these sources include solar cell, fuel cell, and wind turbine [1]-[4]. In using the power of mentioned renewable sources by AC load or network, the voltage level value should be increased enough to be inverted to desired AC value [5]. PV-panel modules can be used in series connection to obtain higher dc voltage [6], [7], but shading problem and decreasing reliability are prohibitive in this method [8]-[12]. Therefore, DC-DC boost converter is better way instead of numerical series PV-panel modules. Conventional DC-DC boost converter is one of the common ways for increasing voltage gain. However, high extra duty cycle is required and this results in reduction of efficiency. In addition, voltage stress on the switch is equivalent to output voltage [13]-[16]. Coupled inductor technique is subsequently introduced, which allows applying turn ratio beside the duty cycle to increase voltage gain [17], [18]. Hence, duty cycle is ranged in suitable value and efficiency is improved. Flyback converter is a typical sample of these converters; although voltage gain is increased by turn ratio of coupled inductor, spike voltage on active switch is appeared due to discharging energy of leakage inductance, so increasing dissipations is the inevitable result of discharging energy of leakage inductance on the active switch [19]. Therefore snubber circuit of the switch is applied. Although the spike voltage is becoming better, dissipations still remain due to leakage inductance [20]. Active clamp circuit can be employed, but the cost and complexity is increased due to extra power switch [19], [22], so passive clamp replaced [30].

To achieve a high step up voltage gain and reduction of leakage inductance dissipations, some new methods such as switched-capacitors [23], [24], switched-inductor [25], voltage lift [26], voltage doubler [27], capacitor-diode voltage multiplier [28] and transformer less switched-capacitor type [13], [29] have been presented. To combine conventional DC-DC boost converters with above mentioned methods, some of topologies like integrated boost and flyback converter [31] , [32], compound of boost and switch-capacitor [33]-[36], and compound of zeta converter and capacitor multiplier [5] have been presented. High voltage gain conversion ratio and recycling leakage inductance energy are merits of these topologies. Moreover, the voltage stress on the active switch and dissipations are decreased. Although the voltage gain conversion ratio is high, more turn ratio is required, so cost and leakage inductance are increased. A safety enhanced high step up DC-DC converter is proposed in [37]. It has safety, but the input current is not continuous. In [21], [38] and [39], three winding coupled inductor are applied. Multiplicity of devices and number of winding are drawbacks.

Quadratic boost is an interesting topology that its voltage gain is the function of quadratic of duty cycle, however the voltage stress on the active switch is equal to output [40]; this topology is made of two cascade boost converter [41]. In [42] and [43], a quadratic boost converter using coupled inductor and voltage multiplier technique, and in [44], a quadratic boost converter using coupled inductor and diode-capacitor technique are presented. These topologies reach the object of extreme high voltage gain without larger turn ratio and duty cycle.

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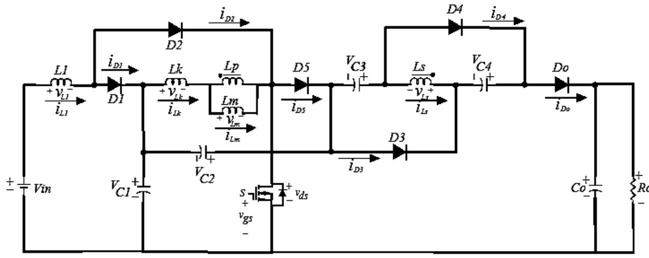

Fig. 1. Equivalent circuit configuration of the proposed converter

In this paper, a novel single switch converter based on quadratic boost is presented. The proposed converter uses coupled inductor and switched-capacitor techniques. The proposed converter has higher output voltage gain in comparison of the other converters based on quadratic boost. Some properties of proposed converter are: 1) The voltage conversion ratio is efficiently increased by a compound of coupled inductor and switched-capacitor techniques. 2) A clamped capacitor is embedded in the path of switch to clamp the voltage across the active switch. So $R_{DS(on)}$ of active switch is alleviated. Furthermore, increasing output voltage is another advantage of the clamped capacitor existence. 3) Efficiency is increased because of reviving the leakage inductance energy of coupled inductor.

The steady state principles of proposed converter in both CCM and DCM operation are given in section II and III, the boundary condition is studied in section IV, a 250W prototype converter in CCM under full load is presented in section V and finally an appropriate conclusion can be driven.

II. Operating Principles Of Proposed Converter

Equivalent circuit of proposed converter is shown in Fig. 1. This converter consists of quadratic boost as primary and switched-capacitor as secondary part of converter. Quadratic boost includes an inductor L_1, two diodes D_1 and D_2, a capacitor C_1, and primary side of coupled inductor L_p with N_p turn. Also switched-capacitor includes diodes D_3 and D_4, and capacitors C_3 and C_4. These capacitors are charged in parallel and discharged in series; when the secondary side of coupled inductor current is changed to positive, they are charging in parallel, conversely, when the secondary side of coupled inductor current is changed to negative they are discharging in series. Finally, the proposed clamped circuit includes diode D_5 and capacitor C_2, capacitor C_1 of quadratic boost also helps C_2 to fix voltage on the active switch. It should be mention that coupled inductor is replaced by leakage inductor L_k, magnetizing inductor L_m, and ideal transformer N_p turn as primary and N_s turn as secondary.

Some assumptions are considered for simplifying analysis of proposed converter:

1) Capacitors C_1, C_2, C_3, C_4, and C_o are large enough. Thus the voltages across them are considered to be constant in one period of switching. The input inductance L_1 isassumed to be large enough so that i_{L1} is continuous.
2) The switch is considered to be ideal and dissipations of the power devices are neglected.
3) The coupling coefficient of the coupled inductor k is equal to $L_m/(L_m + L_k)$, and the turn ratio n is equal to N_s/N_p. The ESR of capacitors and parasitic resistance of coupled inductor are neglect.

A. CCM Operation

The waveforms of proposed converter are shown in details in Fig. 2, and the paths of currents are illustrated in Fig. 3, so the proposed converter is analyzed in CCM mode as follow:

1) *Mode I [t_0,t_1]:* In this transition mode switch S is conducted, also diodes D_2, D_3, and D_4 are biased. Magnetism inductor L_m is releasing its energy to the C_3 and C_4 by secondary side of coupled inductor. The current flow path is shown in Fig.3 (a); as shown, I_{Lk} is increasing, because of C_1 releases its energy to the primary. Diode D_1 is reversed-biased by V_{C1}. Meanwhile, V_{in} is releasing its energy to the L_1 through D_2 and S. The diode current i_{D3} and i_{D4} are decreasing. C_o is discharging its energy to the load. This mode is finished when decreasing i_{Lm} equals increasing i_{Lk} at t_1 [5].

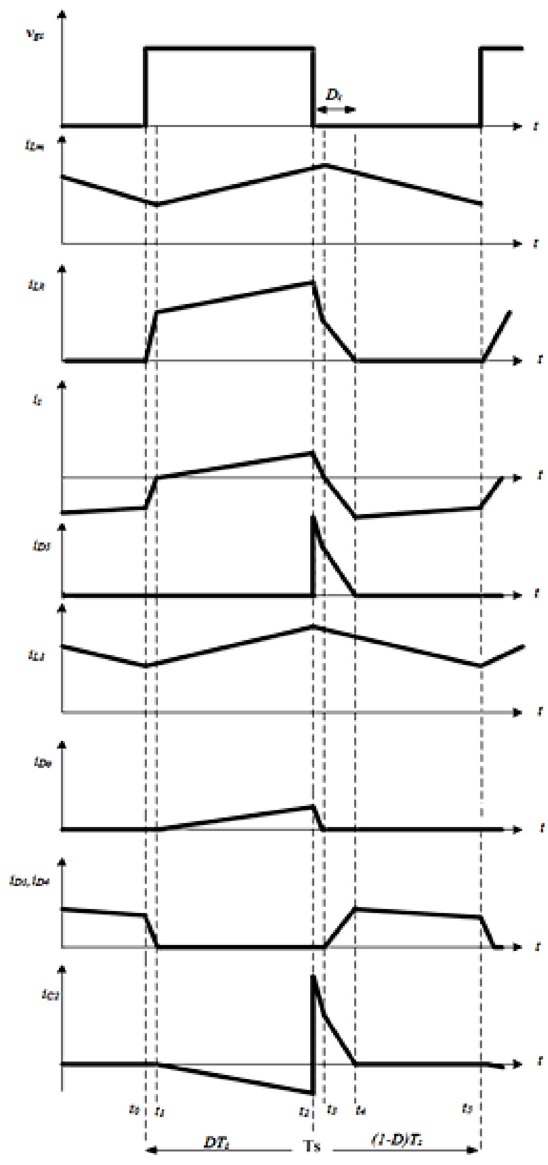

Fig. 2. Some typical waveforms of proposed converter at CCM operation

2) *Mode II* [t_1,t_2]*:* In this interval, switch S is still on, diodes D_2 and D_o are biased. The current flow path is shown in Fig. 3(b); capacitors C_1, C_2, C_3, and C_4 are connected in series with secondary side of winding N_S and release their energies to R_o and C_o. In this section, clamped capacitor C_2 is discharged to output load and capacitor. Diodes D_3 and D_5 are reversed-biased by $V_{Ls}+V_{C3}$ and $V_{C1}+V_{C2}$, respectively. Meanwhile, energy of V_{in} is stored by L_1. Capacitor C_1 is releasing part of its energy to L_m and L_k. Currents i_{Do} and i_{Ns} are increasing and i_{C1} is decreasing. At the end of this mode i_{Ns} is receiving maximum value and this mode ends when switch is turned off at t_2.
3) *Mode III* [t_2,t_3]*:* In this mode switch S is off and diode D_1 is turned on because of I_{L1} continuation constraint. The current flow path is shown in Fig. 3(c); as shown, diodes D_5 and D_o are biased. Leakage inductance L_k releases its energy to clamped capacitor C_2 through D_5. Furthermore, capacitor C_1 is charged through D_1 by V_{in} and L_1. Capacitors C_3 and C_4 transfer their energy on C_o and R_o throughout D_o. Meanwhile, currents i_{Lk} and i_{LNs} reduce instantly. However, magnetism current i_{Lm} increase. This mode is finished when i_{LNs} equals zero at t_3. The voltage across switch S is the summation of voltage of quadratic boost capacitor V_{C1} and voltage of clamped capacitor V_{C2}.
4) *Mode IV* [t_3,t_4]*:* In this mode, switch S is still off like former mode. Diode D_o is reversed-biased by V_o-V_{C1}-V_{C2}-V_{C4}. Fig. 3(d) shows the current flow path. Diodes D_1, D_5, D_3, and D_4 are conducting; as mentioned in previous section, when i_{Ns} is negative, the energy of magnetism current i_{Lm} transfer from secondary side of winding to C_3 and C_4. Energy of leakage inductance L_k is also continued to discharge to C_2 by means of D_5. In this interval, currents i_{D5} and i_{Lk} are decreased immediately. Capacitor C_1 is also charged by input source V_{in} and L_1. The voltage across switch is the same as former mode. Current i_{Lm} is decreasing while i_{D3} and i_{D4} is increasing. This mode ends when $i_{Lk}=0$.
5) *Mode V* [t_4,t_5]*:* In this mode switch S is also off. Meanwhile, diodes D_1, D_3, and D_4 are conducting. Magnetism inductor L_m is releasing completely its energy to C_3 and C_4 via the secondary side of coupled inductor. The current flow path is shown in Fig. 3(e); as shown, there is a path between V_{in}, L_1 and C_1, so C_1 is Charged by input source V_{in} and L_1. R_o is receiving its energy from C_o and the voltage stress on the switch is the same as pervious mode. This mode is ended when switch S is turned on.

B. DCM Operation

In this operation, we have five modes, to simplify the circuit operation, leakage inductor L_k is neglected, Fig. 4 shows the typical waveforms when the proposed converter works in DCM mode.

Fig. 5 shows the principles of DCM operation, as shown, we have five modes and operating are illustrated as follow:

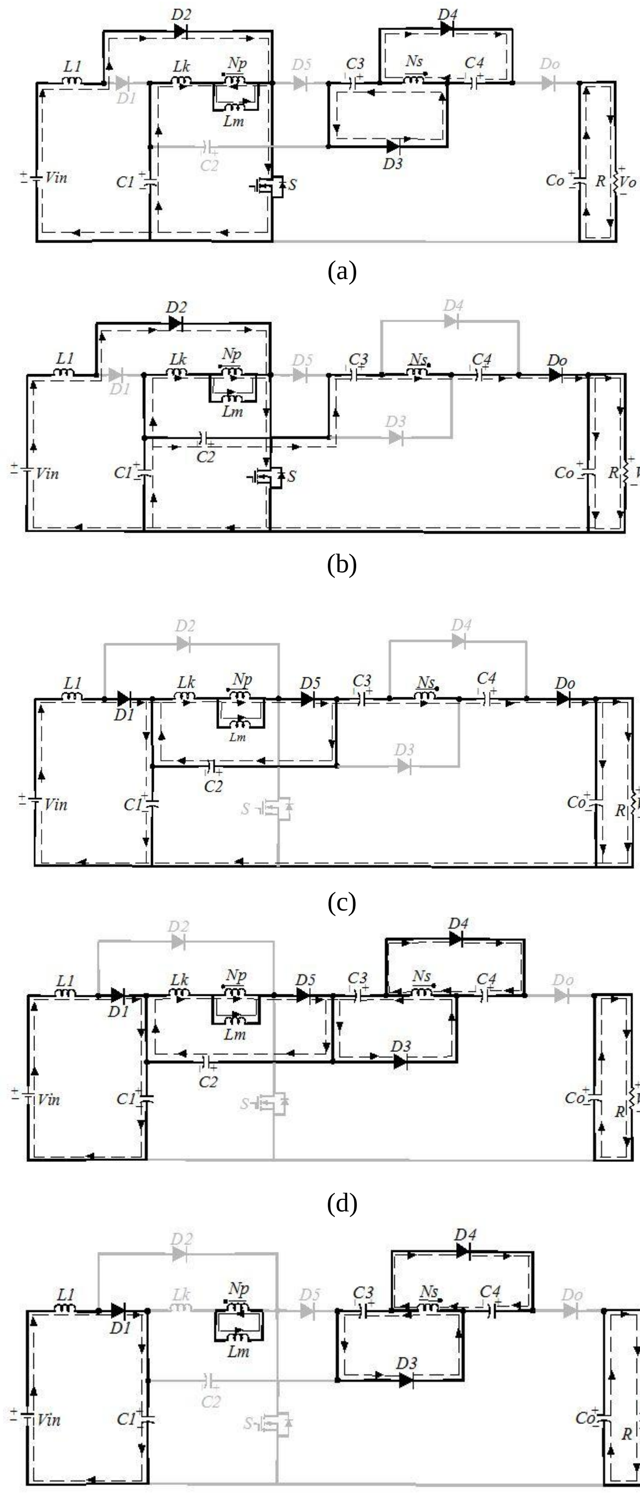

Fig. 3. Current flow paths of operating modes during on switching period at CCM operation. (a) Mode I. (b) Mode II. (c) Mode III.(d) Mode IV.(e) Mode V.

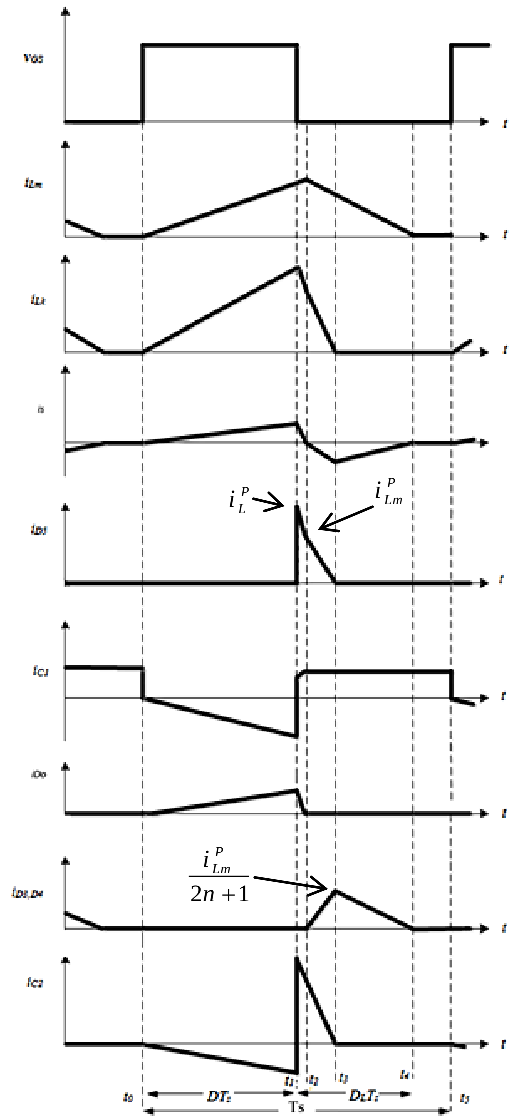

Fig. 4. Some typical waveforms of proposed converter at DCM operation

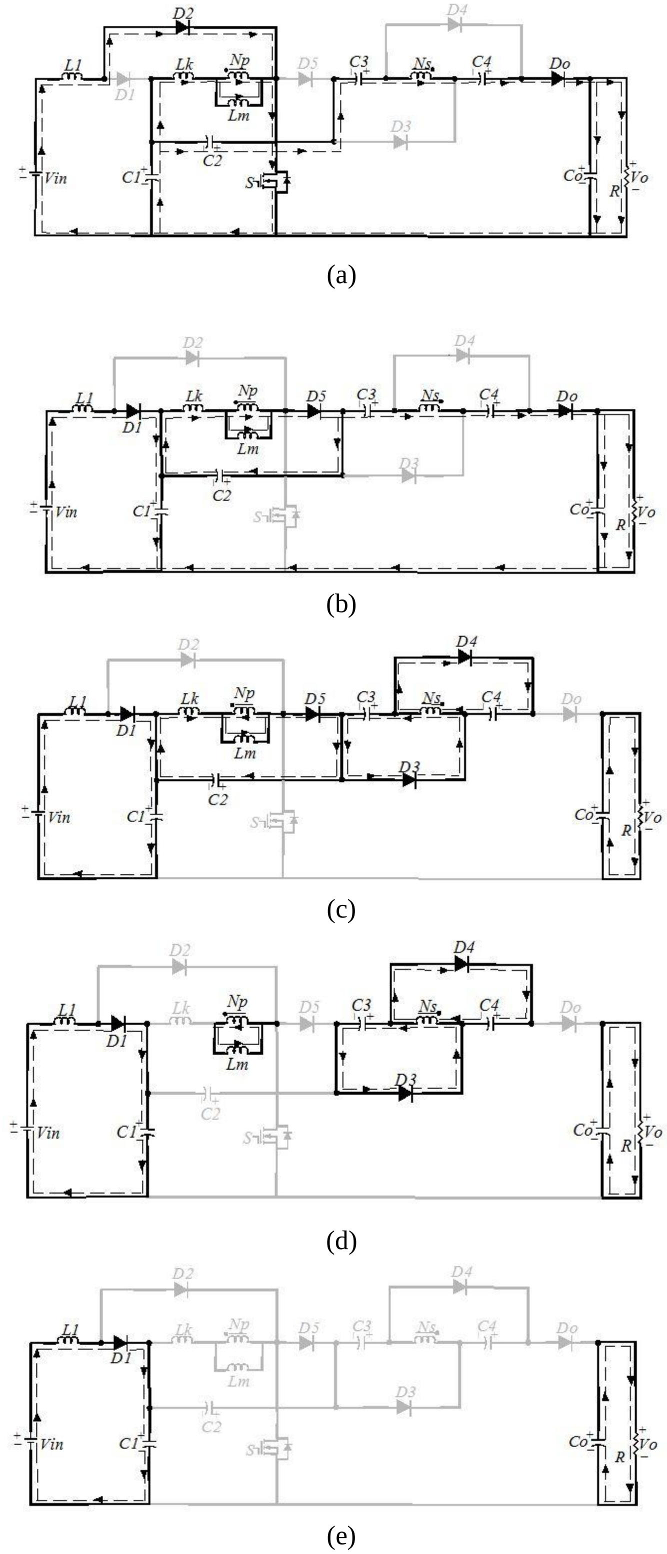

Fig. 5. Current flow paths of operating modes during on switching period at DCM operation. (a) Mode I. (b) Mode II. (c) Mode III.(d) Mode IV.(e) Mode V.

1) *Mode I [t_0,t_1]:* In this section switch S is on and diodes D_2 and D_o are biased. Therefore, energy is transferred from D_o to the output. Meanwhile, magnetism inductor L_m and leakage inductor L_k are receiving energy from C_1, so currents i_{Lm} and i_{Lk} are increasing. V_{in} is charging L_1, while capacitors C_2, C_3, and C_4 are discharging to output capacitor C_o and load R_o . So, current of these capacitors becomes negative. This mode ends when the switch is turned off at t_1.
2) *Mode II [t_1,t_2]:* In this transition mode switch S is turned off and diodes D_1, D_5, and D_o are biased. So, energy of leakage inductance L_m is transferred from D_5 to C_2. Meanwhile, C_1 is charged through D_5 by input voltage V_{in} and inductor L_1. This mode is ended when decreasing i_{Lk} equals increasing i_{Lm} at t_2.
3) *Mode III [t_2,t_3]:* In this mode switch S is still turned off and only diodes D_2 and D_o are reversed-biased. Also leakage inductance i_{Lm} is still transferring its energy from D_5 to C_2. Meanwhile, magnetism inductor L_m is releasing its energy to C_3 and C_4 via the coupled inductor, so, the current of secondary side of coupled inductor is become negative. Hence, D_o is off and R_o is fed by C_o. This mode is ended when the energy of leakage inductance is vanished at t_3.
4) *Mode IV [t_3,t_4]:* In this mode, switch S is still turned off

and diodes D_1, D_3 and D_4 are biased. Meanwhile, Energy of magnetism inductor L_m is also transferred to capacitors C_3 and C_4 and they are charging in parallel. R_o is continued to feed by C_o, capacitor C_1 is charged by L_1 and V_{in} through D_1. This mode is ended when energy of magnetism inductor L_m is completely discharged at t_4.

5) *Mode V [t_4,t_5]:* In this final mode only D_1 is on and the others are off. Current i_{Lm} is equal zero. However, R_o and C_1 are still fed by C_o and V_{in} and L_1, respectively. This mode is continued till end of the period T_s at t_5.

III. Steady State Analysis Of Proposed Converter

A. CCM Operation

To simplify the analysis of steady state of converter, two modes II and V are considered. Leakage inductor of secondary side of winding is neglected; as illustrated in Fig. 3, following equations can be written by using voltage balance on L_1,L_p and L_s:

$$V_{C1} = \frac{1}{1-D}V_{in} \tag{1}$$

$$V_{C3} = V_{C4} = \frac{nkD}{1-D}V_{C1} = \frac{nkD}{(1-D)^2}V_{in} \tag{2}$$

From obtaining V_{C2}, we use D_C from [30], D_c is the time that leakage inductor releases its energy to the C_2.

$$D_C = \frac{2(1-D)}{1+n} \tag{3}$$

$$V_{C2} = \frac{D}{D_C}V_{C1} = \frac{D(1+n)}{2(1-D)^2}V_{in} \tag{4}$$

As $V_{Ls}^{(II)}$ is calculated in mode II, therefore $V_o^{(II)}$ is obtained as follow:

$$V_o = \frac{1}{1-D}V_{in} + \frac{D(n+1)}{2(1-D)^2}V_{in} + \frac{2nkD}{(1-D)^2}V_{in} + \frac{nk}{1-D}V_{in} \tag{5}$$

So converter gain will be:

$$M_{CCM} = \frac{n(2kD+D+2k)+(2-D)}{2(1-D)^2} \tag{6}$$

The voltage gain versus the duty cycle under various coupling coefficients of the coupled inductor is shown in Fig. 6. It illustrates that the voltage gain is not very sensitive to the coupling coefficient, so, at k=1, the ideal voltage gain is written as:

$$M_{CCM} = \frac{n(3D+2)+(2-D)}{2(1-D)^2} \tag{7}$$

Voltage conversion ratio of proposed converter in CCM mode operation compare to the other papers is shown in Fig. 7, which n =2, k =1, and D = (0 ,0.7). From Fig. 8, it is obvious

that the voltage gain of proposed converter is higher than the similar topologies after D=0.4, so this converter is preferred to the other converters where high voltage gain is required.

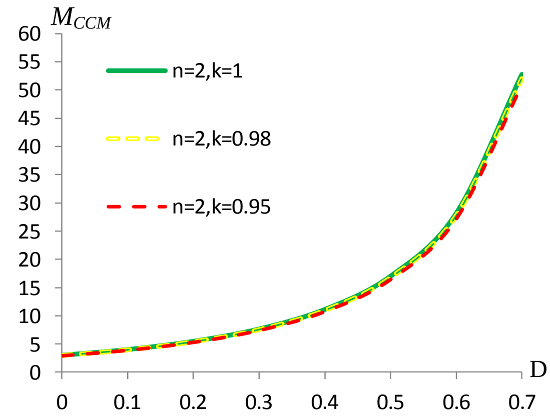

Fig. 6. Voltage gain versus duty cycle at CCM operation under n = 2 and various k.

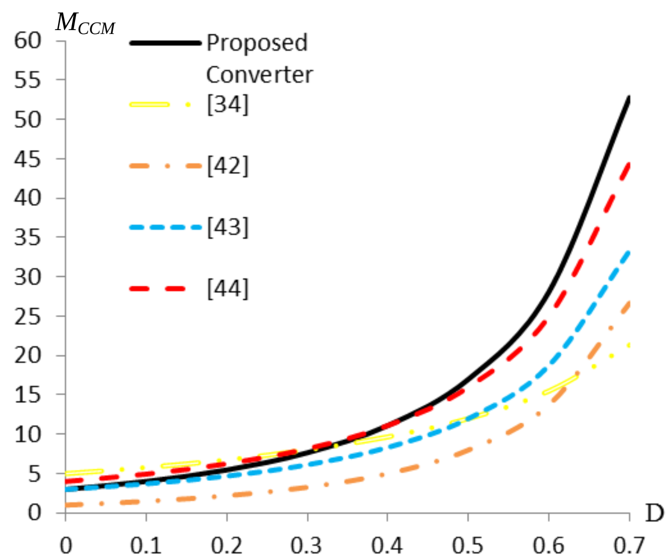

Fig. 7. Voltage gain versus duty ratio of the proposed converter and converters in [34],[42],[43] and [44] at CCM operation under n=2 and k=1

Moreover, voltage stresses on active switch S and diodes D_1, D_2, D_3, D_4, D_5, and D_O are obtained as follow:

$$V_{SW} = V_{D5} = \frac{2+D(n-1)}{2(1-D)^2}V_{in} = \frac{2+D(n-1)}{n(3D+2)+(2-D)}V_o \tag{8}$$

$$V_{Do} = \frac{n}{(1-D)^2}V_{in} = \frac{2n}{n(3D+2)+(2-D)}V_o \tag{9}$$

$$V_{D1} = \frac{1}{1-D}V_{in} = \frac{2(1-D)}{n(3D+2)+(2-D)}V_o \tag{10}$$

$$V_{D2} = \frac{D(n+1)}{2(1-D)^2}V_{in} = \frac{D(n+1)}{n(3D+2)+(2-D)} \tag{11}$$

$$V_{D3,4} = \frac{n}{(1-D)^2}V_{in} = \frac{2n}{n(3D+2)+(2-D)}V_o \tag{12}$$

B. DCM Operation

As illustrated, there are five modes in DCM. D_L is the period of time that magnetism current decrease from its maximum value to zero. By applying voltage balance on L_1,

L_{Np}, and L_{Ns} and neglecting second and fourth modes (because of the short time of second mode and getting together third and fourth mode as third mode), following equation are given:

$$V_{C1}=\frac{1}{1-D}V_{in} \tag{13}$$

$$V_{C2}=\frac{D}{D_L(1-D)}V_{in} \tag{14}$$

$$V_{C3}=V_{C4}=\frac{nD}{D_L(1-D)}V_{in} \tag{15}$$

$$V_{Ls}^{(I)}=nV_{C1}=\frac{n}{(1-D)}V_{in} \tag{16}$$

By simplifying above equations the relationship between input voltage and output voltage can be derived as follow:

$$V_o=\frac{D_L(n+1)+D+2nD}{D_L(1-D)}V_{in}=\frac{1}{1-D}(1+n+\frac{D+2nD}{D_L})V_{in} \tag{17}$$

Now the value of D_L is calculated as follow:

$$D_L=\frac{D(1+2n)V_{in}}{(1-D)V_o-(1+n)V_{in}} \tag{18}$$

By considering peak value of magnetism current is equal to Δi_{Lm} , so we have:

$$I_{Lmpeak}=\frac{V_{C1}}{L_m}DT_S=\frac{DT_S}{L_m}\frac{V_{in}}{1-D} \tag{19}$$

Because of average value of C_1, C_2, C_3, C_4 and C_o is equal to zero, so yields:

$$<i_o>=<i_{Do}>=<i_{D3}>=<i_{D4}>=<i_{D5}> \tag{20}$$

$$<I_{CO}>=<I_{Do}>-<I_O>=\frac{1}{2}D_L\frac{I_{Lmp}}{2n+1}-I_O=0 \tag{21}$$

Since I_{Co} is equal to zero in steady state, by substituting (18) and (19) into (21) yields:

$$\frac{D^2V_{in}^2T_S}{2((1-D)V_O-(1+n)V_{in})(1-D)L_m}=\frac{V_O}{R_O} \tag{22}$$

Then, the normalized magnetizing inducted time constant is defined as:

$$\tau_{Lm}=\frac{L_m}{RT_s}=\frac{L_mf_s}{R} \tag{23}$$

Substituting (23) into (22) yield:

$$M_{DCM}=\frac{V_O}{V_{in}}=\frac{1+n}{2(1-D)}+\frac{1}{1-D}\sqrt{\left(\frac{1+n}{2}\right)^2+\frac{D^2}{2\tau_{Lm}}} \tag{24}$$

Fig. 8 illustrates the voltage gain versus the duty ratio under various τ_{Lm} values.

C. Boundary Operating Condition

If the proposed converter is operated in boundary condition mode between CCM and DCM, the voltage gain of CCM operation and DCM operation are equal. From two previously obtained gains, the boundary normalized magnetizing-inducted time constant τ_{LmB} can be derived as:

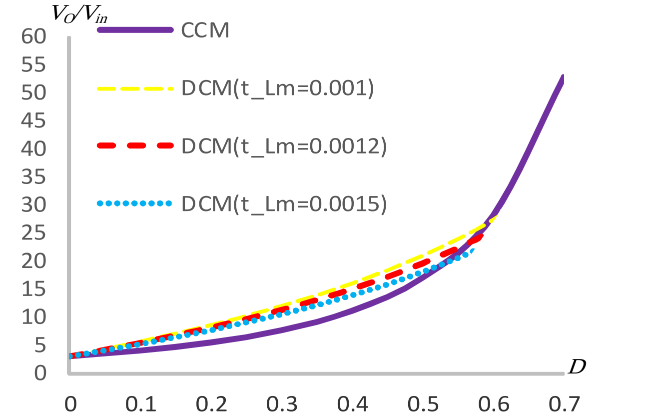

Fig. 8. Voltage gain versus duty ratio at DCM operation under various τ_{Lm} value and CCM operation under n=2 and k=1

$$\tau_{LmB}=\frac{2(1-D)^2D^2}{(4nD+n+1)^2-(1+n)^2(1-D)^2} \tag{25}$$

The curve of the τ_{LmB} versus duty ratio of the proposed converter is shown in Fig. 9. If τ_{Lm} is larger than τ_{LmB} , the proposed converter will be operated in CCM operation.

IV. Design And Experimental Result Of The Proposed Converter

To check operation of the proposed converter, a prototype circuit is made in laboratory and its characteristics are shown in table I. Experimental results show the measured waveforms of prototype converter for full-load P_o=250 W and input voltage V_{in}=24V. The prototype converter operates in CCM under the full load condition. The steady state analysis of circuit can be demonstrated in the experimental results; as shown in Fig. 10, V_{Gs} illustrate that duty cycle is 50%, voltage stress on diodes V_{D0}, V_{D1}, and V_{D2} demonstrate the consistency of (9)-(11). Moreover, complementary conduction of diodes D_1 and D_2 is obvious. The voltage across on the switch S is clamped on 120V during switch-off period, the voltage stress on the switch is nearly equivalent to summation of V_{C1} and V_{C2} (8). So, a low voltage rated switch can be considered for proposed converter to reduce conduction loss. Finally, output

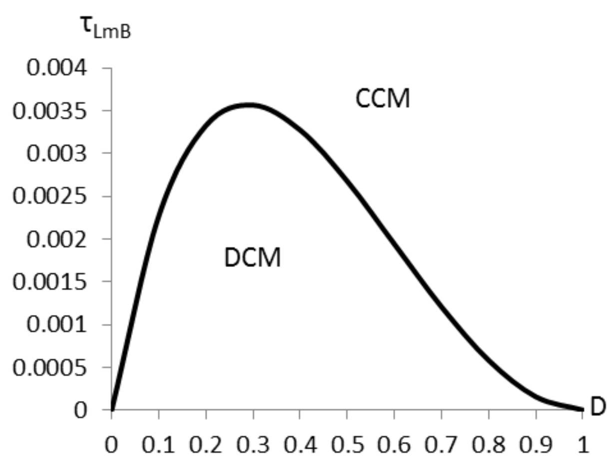

Fig. 9. Boundary condition of the proposed converter under n=2

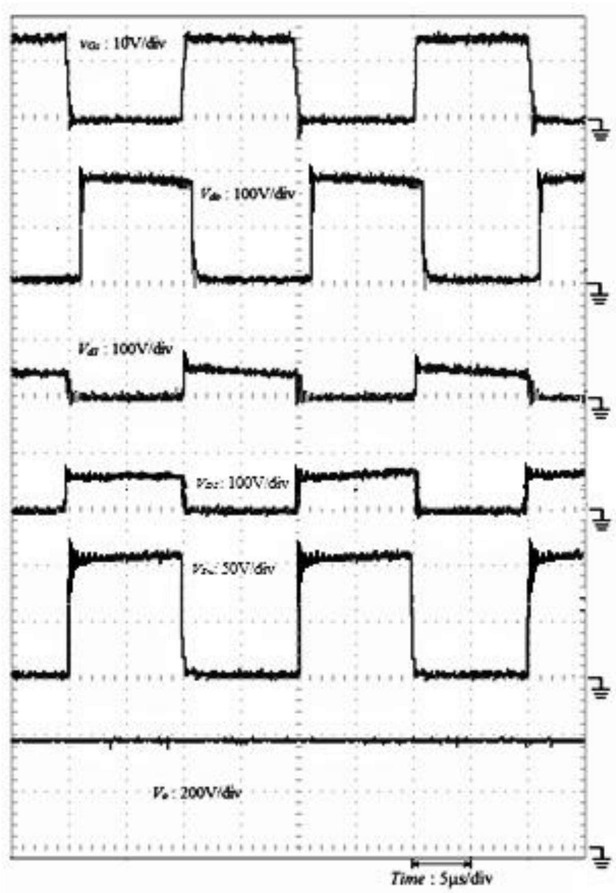

Fig. 10. Experimental result of the voltage stress on: V_{GS}, V_{do}, V_{d1}, V_{d2}, V_{sw}, and V_o, respectively.

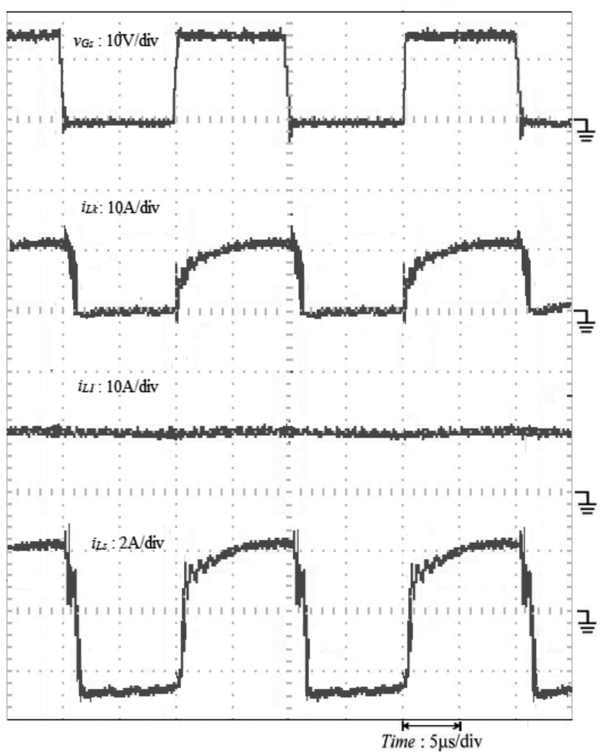

Fig. 11. Experimental result of the current waveform of i_{Lk}, i_{L1} and i_S, respectively.

voltage is shown in this figure which is approximately consistent with (7). Fig. 11 is illustrated leakage current I_{Lk}, input inductor current i_{L1} and secondary current I_{Ls}; I_{Ls} demonstrates that proposed converter is operated in CCM mode because the current is not equal to zero when the active switch is turned on [35]. I_{L1} appears obvious continuity of input current of converter because input current I_{in} equals inductor current I_{L1}, so input current ripple is cancelled. Fig. 12 shows current and voltage of diodes and capacitors. The voltage stress $V_{D3(D4)}$ confirms the equation (12). Next, the

TABLE I
UTILIZED COMPONENTS AND PARAMETERS OF PROTOTYPE

Components	**Parameters**
Input dc voltage: V_{in}	24V
Output dc voltage: V_{out}	400V
Max output power: P_{out}	250W
Switching frequency: f	50 kHz
MOSFET S	IRFP260NPBF
Diodes D_1/D_2	BYV32-200
Diodes $D_3/D_4/D_5$	MUR460
Coupled inductor:	$n : 2$
L_m	$400\mu H$
L_k	$1\mu H$
Inductor: L_1	230 µH
C_1	68µF/50V
C_2	5.6µF/100V
$C_{3,4}$	2.85µF/400V
C_O	100µF/450V

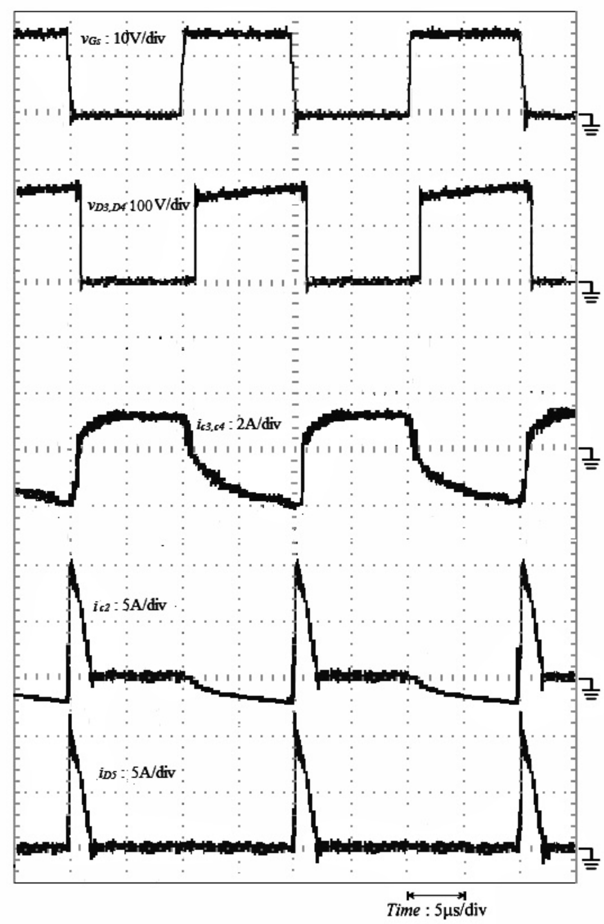

Fig. 12. Experimental result of some diodes and capacitor: V_{d3}, V_{d4}, V_{d5}, I_{C3}, I_{C4}, I_{C2}, and I_{D5}, respectively.

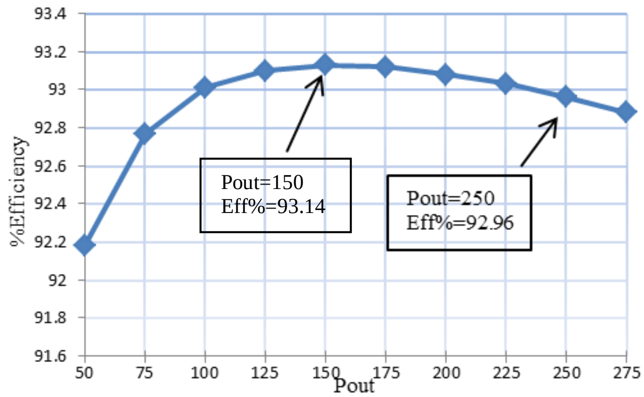

Fig. 13. Efficiency versus output power

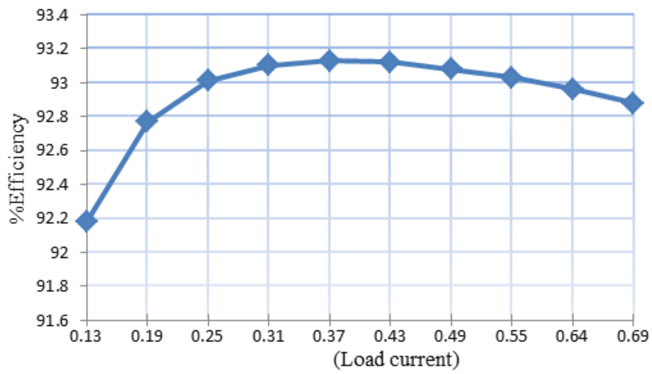

Fig. 14. Efficiency versus output current

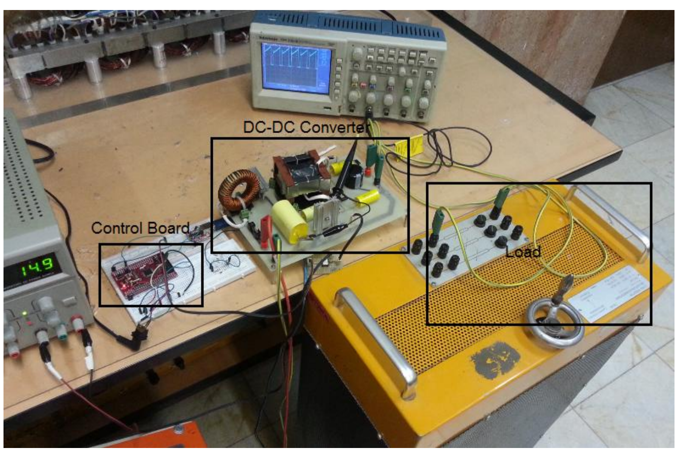

Fig. 15. Prototype of proposed converter

measured current of capacitor $C_{3(4)}$ is shown, which is agreed the theoretical analysis of converter. Moreover, the current of capacitor $C_{3(4)}$ is in harmony with the diode on-off time of $D_{3(4)}$. At the end, the current of C_2 and D_5 illustrate that energy of leakage inductance is discharge to capacitor C_2 through D_5.

Efficiency can be estimated by considering active switch, diodes and capacitors dissipations. Active switch includes two types of dissipations; conduction losses and switching losses [5]. Efficiency versus output power variations is shown in Fig. 13, which is equal to 92.96% and optimum efficiency is occurred in 150 W output power. Also, efficiency versus load current is shown in Fig. 14.

A prototype proposed converter is displayed in Fig. 15.

V. Conclusion

A novel topology of non-isolated high step up dc-dc converter has been introduced into renewable sources of energy by using quadratic boost as primary and switched-capacitor as secondary part of circuit. Input current of converter is continuous, so current stress on source is reduced. To produce higher voltage gain in this topology, only one switch is used which reduced complexity of converter control. Furthermore, the energy of leakage inductance has recycled throughout of clamped capacitor; the voltage stress on the main switch is clamped because of the existence of clamed capacitor, so low on-state resistance $R_{DS(on)}$ can be chosen. To verify the proposed converter, a prototype 250W is implemented with 24V input and 400V output voltage, output waveforms have illustrated in CCM operation, and efficiency is approximately 93% in full-load. Theoretical calculations are confirmed by experimental results to some extent.

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