# A New Nonisolated Quasi-Z-Source Inverter With High Voltage Gain

Xiaoquan Zhu, Bo Zhang, *Senior Member, IEEE* and Dongyuan Qiu, *Member, IEEE*

***Abstract*—This paper proposes a new high boost quasi-Z-source inverter (qZSI) with combined two quasi-Z-source networks, which has a common ground between the input source and the inverter bridge. Compared with other non-coupled inductor-based (q)ZSIs, by using the same total number of passive and active components, the proposed inverter provides higher boost capability, requires smaller inductance and capacitance values at the impedance network, achieves lower voltage stress across the active switching devices, and has higher modulation index for the inverter bridge to improve the output waveform quality. Although the proposed inverter has the same voltage boost factor with the enhanced boost (quasi-)Z-source inverters (EB-ZSI and EB-qZSI), the proposed scheme has lower capacitor voltage stress than EB-ZSI and has higher efficiency than EB-qZSI. The topological configuration, operating principles, power loss analysis, and performance comparison with other high boost (q)ZSIs are presented. Finally, both simulations and experimental results are given to validate the aforementioned characteristics of the proposed topology.**

***Index Terms*—DC-AC power conversion, boost factor, impedance network, high-gain voltage, quasi-Z-source inverter (qZSI).**

## I. INTRODUCTION

THE traditional three-phase voltage source inverter (VSI) and current source inverter (CSI) are the most commonly used two kinds of pulse width modulation (PWM) inverter topologies. And, they have been widely used in many industrial applications such as uninterruptible power supply, ac motor drives, and hybrid electric vehicles [1]-[2]. However, both of them still exist some major problems. For the traditional VSI, its ac output voltage is always lower than the dc input voltage; thus, the VSI only performs a buck converter for the dc-ac power conversion. Similarly, the traditional CSI only performs a boost converter due to its ac output voltage is always greater than the original dc input voltage. For some applications where both voltage buck and boost capabilities are needed, an additional dc-dc converter will be required in VSI and CSI, which induces a two-stage power conversion, to obtain the desired ac output voltage. As a result, the volume and size of the whole system will be increased, leading to high weight, high cost and low overall efficiency[3].

To overcome the aforementioned limitations in traditional VSIs, a novel, simple and efficient design of Z-source inverter (ZSI) was firstly proposed by Peng in 2003[4], as shown in Fig. 1(a). By using the Z-source network, which consists of two inductors and two capacitors connected in an X-shape, to replace the traditional dc link in VSI, the ZSI can achieve both voltage buck and boost operating capabilities with a single-stage power conversion. In addition, both the semiconductor switches of each phase leg can be turned on simultaneously, which implies that the anti-interference ability of the inverter can be further improved, especially for the switches misgating-on caused by the electromagnetic interference noise. And no dead time is needed, so the output waveform distortion can be greatly reduced. Due to these distinct advantages, the study of Z-source converter has become a hot topic, and the researches mainly focus on the modelling and control [5]-[7], the modulation strategies [8]-[10], and new Z-source converter topologies [11]-[33].

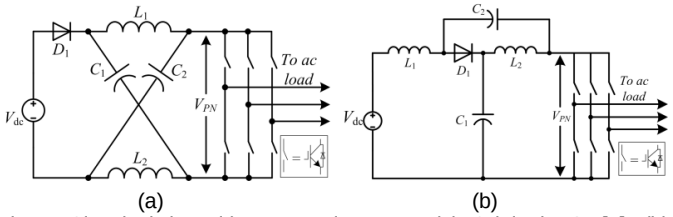



Fig. 1 Classical (quasi-)Z-source inverters: (a) Original ZSI [4], (b) quasi-ZSI [13].

Despite the aforementioned advantages, the classical ZSI also has some drawbacks, such as huge inrush current at start-up, lager voltage stress on capacitors and switches, discontinuous input current, and the dc input voltage source has no common ground with the inverter bridge [11]-[12]. To address these problems, the quasi-Z-source inverter (qZSI) was proposed in [13], as shown in Fig. 1(b), which not only retains the main characteristics of classical ZSI, but also can provide continuous input current, lower capacitor voltage stress, and common ground between the dc input source and the inverter bridge. However, the boost capability of the qZSI is still not high enough for many industrial applications.

Recently, a number of new Z-source impedance networks have been proposed for high boost ZSIs. In order to obtain high dc-link voltage with a small shoot-through duty ratio, five extended-boost qZSIs have been proposed in [14], which can be categorized as the continuous- or discontinuous-current diode-/capacitor-assisted qZSIs (DA-qZSI/CA-qZSI), and the

Manuscript received February 3, 2018; revised July 23, 2018; accepted September 18, 2018. This work was supported in part by the Team Program of Natural Science Foundation of Guangdong Province, China, under Grant No. 2017B030312001, and in part by the Key Program of National Natural Science Foundation of China, under Grant No. 51437005. (*Corresponding author: Bo Zhang*).

Xiaoquan Zhu, Bo Zhang and Dongyuan Qiu are with the School of Electric Power, South China University of Technology, Guangzhou 510640, China (e-mail: ijrue68@163.com; epbzhang@scut.edu.cn; epdyqiu@scut.edu.cn).

hybrid extended-boost qZSIs (HE-qZSI), respectively. In addition, by combining the switched-inductor (SL) cell, switched-capacitor (SC) cell, and the hybrid SL/SC cells with the classical (quasi-) Z-source network, several new (q)ZSIs have been proposed in [15]-[18]. In [15], a switched-inductor Z-source inverter (SL-ZSI) was proposed by using two SL cells to replace the two inductors in the Z-source network, as shown in Fig. 2(a). In [16] and [17], by applying one SL cell and two SL cells into the qZS network, two kinds of switched-inductor quasi-Z-source inverters (SL-qZSI) were presented, respectively. In order to produce higher boost factor for the classical ZSI, additional SL/SC cells can be cascaded at the generalized multicell SL/SC ZSIs, as presented in [18]. By combining the active SC/SL cells with the qZS network, an extended active switched-capacitor/switched-inductor-qZSI (ASC/SL-qZSI) was proposed in [19]. In addition, by using the switched Z-impedance network to replace the traditional Z-source network, two kinds of enhanced boost-(q)ZSIs were proposed in [21] and [22],as shown in Fig. 2(b) and Fig. 2(c), respectively.

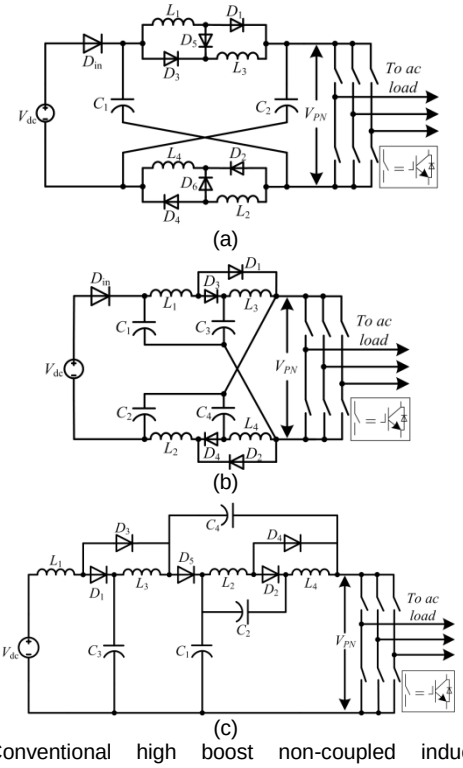



Fig. 2 Conventional high boost non-coupled inductor type (quasi-)Z-source inverters: (a) SL-ZSI [15], (b) Enhanced boost-ZSI (EB-ZSI) [21], (c) Enhanced boost-qZSI (EB-qZSI) [22].

For even higher voltage boosting, tapped- or coupled -inductors and transformers have been used to replace the traditional inductors in Z-source impedance network. Thus, the TL-ZSIs in [25], trans-ZSIs in [27], TZ-ZSIs in [28] and the other new magnetically coupled ZSIs in [29] have been proposed, respectively. However, for those coupled-inductor (or transformer) based ZSI topologies, when their winding currents are switched under the high dc-link voltage condition, the over-voltages may would be caused by their leakage inductances, which will shorten the life span of these magnetic devices and damage the active power switches. In order to reduce the voltage stress on passive/active components, an alternate-cascaded technique between impedance networks is proposed in [30], and accordingly some new cascaded high boost ZSIs have been proposed in [31]-[33]. In [31], cascaded multicell trans-ZSIs are presented, in which a single high power transformer with large turns ratio is replaced by cascaded multiple small transformers, thus, the inverter can achieve higher efficiency and lower component stresses. In [32] and [33], two kinds of alternate-cascaded high-boost ZSIs have been proposed, which combine the switched-inductor with tapped-inductor cells and transformer cells, respectively.

Based on the classical qZSI, this paper proposes a new high boost qZSI with combined two qZS networks. Compared to the existed non-coupled inductor-based (q)ZSIs, the proposed inverter can provide higher boost factor and lower voltage stresses across active switching devices with the same shoot-through duty ratio. Moreover, for obtaining the same buck-boost factor, the proposed topology can use a higher modulation index, thus, the output waveform quality can be improved with lower total harmonic distortion (THD).

The remainder of this paper is organized as follows. Section II gives a description of the proposed topology. The operating principles will be analyzed in Section III. In Section IV, the design guidelines of passive and active components are discussed. The comprehensive performance comparison with other high boost (q)ZSIs is presented in Section V. It is followed by the power loss analysis and efficiency comparison with other topologies in Section VI. In Section VII, both the simulation and the experimental results will be conducted to validate the theoretical analysis. Finally, a conclusion is drawn in Section VIII.

## II. Configuration of The Proposed Topology

The configuration of the proposed inverter is depicted in Fig. 3. It can be seen from Fig. 3 that the proposed inverter consists of four inductors, four capacitors, five diodes and a three-phase inverter bridge. Inductors $L_2$, $L_3$, capacitors $C_2$, $C_3$, and diode $D_3$ composes the first quasi-Z-source network The second quasi-Z-source network consists of inductors $L_1$, $L_4$, capacitors $C_1$, $C_4$, and diodes $D_1$, $D_4$. The other two diodes $D_2$ and $D_5$ are used to connect these two quasi-Z-source network. Therefore, by combining these two qZS network appropriately, the proposed inverter would have higher boost capability.

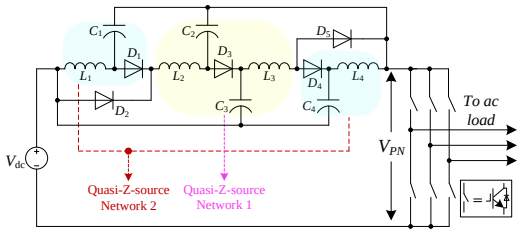



Fig. 3 Configuration of the proposed qZSI with combined two quasi-Z-source networks.

## III. Operating Principle of The Proposed Inverter

In this section, the operating principle of the proposed inverter would be analyzed in detail. To simplify the analysis,

we assume that all the components used in the topology are ideal, capacitors, inductors, and resistors are all linear, time invariant, and frequency independent.

### A. *Steady-state analysis of the proposed qZSI*

The operating principle of the proposed qZSI is similar to the classical (q)ZSIs. It has six active states, two zero states and an extra shoot-through zero state for the inverter bridge. For analysis, it can be simplified into two operating states, shoot-through and non-shoot-through states, as shown in Fig. 4. The inverter bridge's action can be replaced by a current source plus a single active switch [14]. The dc side theoretical waveforms of the proposed inverter are shown in Fig. 5.

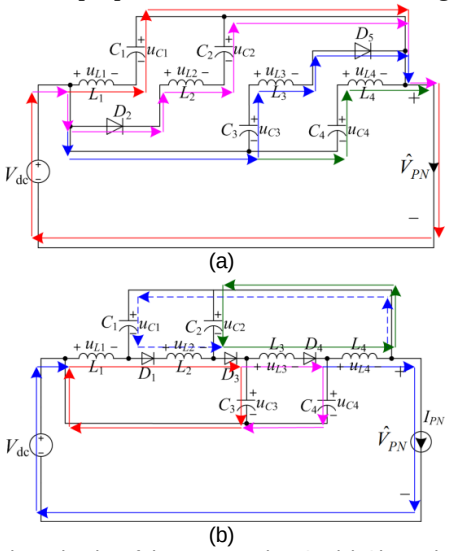



Fig. 4 Equivalent circuits of the proposed qZSI. (a) Shoot-through state, (b) Non-shoot-through state.

*1) Shoot-Through State*: The equivalent circuit of the proposed qZSI in this state, which is represented by a closed switch, is show in Fig. 4(a), and the dc-link side is short circuited. During this state, diodes $D_2$ and $D_5$ both are forward biased. While, diodes $D_1$, $D_3$ and $D_4$ are all reverse blocking due to the reverse parallel connection with capacitors. Assuming that $T_0$ is the time interval of this state, and $T_0$=$DT_s$, where $D$ is the shoot-through duty ratio of the inverter bridge, $T_s$ is the switching period. There are four loops during this state: 1) loop 1 is composed of $V_{dc}$, $L_1$, $C_1$. The input voltage source $V_{dc}$ is in series with capacitor $C_1$ to charge inductor $L_1$; 2) loop 2 is consisted of $V_{dc}$, $D_2$, $L_2$, $C_2$. $V_{dc}$ and $C_2$ discharge the energy to $L_2$; 3) loop 3 is composed of $V_{dc}$, $C_3$, $L_3$, $D_5$. $V_{dc}$ and $C_3$ charge inductor $L_3$ in series; 4) loop 4 is consisted of $V_{dc}$, $C_4$, $L_4$. $V_{dc}$ and $C_4$ discharge the energy to $L_4$. Thus, inductors are all charged by the dc input voltage source and capacitors in series. Assuming that all the capacitor voltages are kept constant during this operating state, then the inductor currents increase linearly. Therefore, from Fig. 4(a), by applying KVL, the following equations can be obtained

$$u_{L1\_on}=V_{dc}+V_{C_1} \quad u_{L2\_on}=V_{dc}+V_{C_2} \tag{1}$$

$$u_{L3\_on}=V_{dc}+V_{C_3} \quad u_{L4\_on}=V_{dc}+V_{C_4} \quad \hat{V}_{PN}=0 \tag{2}$$

where $u_{L\_on}$ is the corresponding inductor voltage during this shoot-through state, and $V_{PN}$ is the dc link voltage across the inverter bridge.

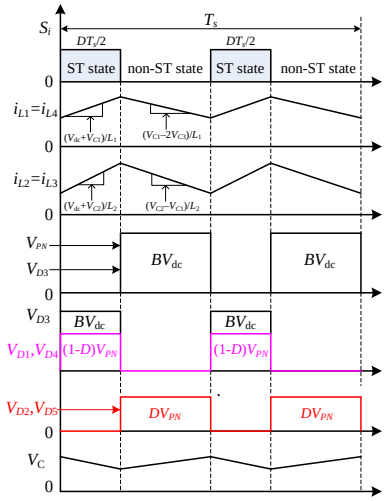



Fig. 5 The dc side theoretical waveforms of the proposed qZSI.

*2) Non-shoot-through state*: The equivalent circuit of this operating state, which is represented by an open switch, is shown in Fig. 4(b), and the inverter bridge has six active states and two zero states. During this state, diodes $D_1$, $D_3$ and $D_4$ will turn on, while diodes $D_2$ and $D_5$ are turned off due to the reverse voltage of inductors $L_1$ and $L_4$. And there are five loops in this operating state: 1) loop 1 is consisted of $L_1$, $D_1$, $L_2$, $D_3$ and $C_3$. Inductors $L_1$ and $L_2$ discharge the energy to $C_3$; 2) loop 2 is composed of $L_1$, $D_1$, $L_2$, $D_3$, $L_3$, $D_4$ and $C_4$. Inductors $L_1$, $L_2$ and $L_3$ discharge the energy to $C_4$; 3) loop 3 is consisted of $D_3$, $L_3$, $D_4$, $L_4$ and $C_2$. Inductors $L_3$ and $L_4$ charge capacitor $C_2$ in series; 4) loop 4 is composed of $D_1$, $L_2$, $D_3$, $L_3$, $D_4$, $L_4$ and $C_1$. Inductors $L_2$, $L_3$ and $L_4$ discharge the energy to $C_1$; 5) loop 5 is consisted of $V_{dc}$, $L_1$, $D_1$, $L_2$, $D_3$, $L_3$, $D_4$, $L_4$ and the inverter bridge. Inductors $L_1$, $L_2$, $L_3$, $L_4$ and the dc input voltage source $V_{dc}$ discharge the energy to the main inverter. From Fig. 4(b), by applying KVL, we have

$$u_{L1\_off}+u_{L2\_off}=-V_{C_3} \tag{3}$$

$$u_{L1\_off}+u_{L2\_off}+u_{L3\_off}=-V_{C_4} \tag{4}$$

$$u_{L3\_off}+u_{L4\_off}=-V_{C_2} \tag{5}$$

$$u_{L2\_off}+u_{L3\_off}+u_{L4\_off}=-V_{C_1} \tag{6}$$

$$\hat{V}_{PN}=V_{dc}-u_{L1\_off}-u_{L2\_off}-u_{L3\_off}-u_{L4\_off} \tag{7}$$

where $u_{L\_off}$ is the corresponding inductor voltage during the non-shoot-through state.

### B. *Boost factor derivation of the proposed inverter*

In steady state, according to the volt-second balance principle of inductor $L$, the average voltage of the inductor in a switching period is zero. Assuming that all the capacitors have the same capacitance, i.e., $C_1$=$C_2$=$C_3$=$C_4$, and the capacitor voltages can be assumed to be constant due to the large capacitance and high switching frequency. Thus, by applying the volt-second property of inductor $L$, from (1)-(2) and (3)-(6), the capacitor voltages, $V_{C1}$, $V_{C2}$, $V_{C3}$ and $V_{C4}$ can be obtained as

$$V_{C_1}=V_{C_4}=\frac{D(3-2D)}{1-4D+2D^2}V_{dc} \tag{8}$$

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2018.2873805, IEEE Journal of Emerging and Selected Topics in Power Electronics



$$V_{C_2} = V_{C_3} = \frac{D(2-D)}{1-4D+2D^2} V_{dc} \tag{9}$$

Substituting (8) and (9) into (3)-(6), we have

$$\begin{cases} u_{L1\_off} = u_{L4\_off} = \dfrac{-D}{1-4D+2D^2} V_{dc} \\ u_{L2\_off} = u_{L3\_off} = \dfrac{D(D-1)}{1-4D+2D^2} V_{dc} \end{cases} \tag{10}$$

Then, the peak dc-link voltage $V_{PN}$ during the non-shoot-through state can be derived as

$$\hat{V}_{PN} = \frac{1}{1-4D+2D^2} V_{dc} \tag{11}$$

Therefore, the boost factor $B$ of the proposed inverter is

$$B = \frac{\hat{V}_{PN}}{V_{dc}} = \frac{1}{1-4D+2D^2} \tag{12}$$

And the peak ac output phase voltage $V_{ac}$ from the inverter can be derived as

$$\hat{V}_{ac} = M \frac{\hat{V}_{PN}}{2} = M \cdot B \cdot \frac{V_{dc}}{2} = G \cdot \frac{V_{dc}}{2} \tag{13}$$

where $M$ is the modulation index. The buck-boost factor $G=M \cdot B$, is the ac output voltage gain. From (13), it can be seen that the ac output voltage gain can be controlled by changing the shoot-through duty ratio $D$ and the modulation index $M$.

Fig. 6 shows a plot of the boost factor $B$ versus the shoot-through duty ratio $D$ for the classical qZSI [13], hybrid extended-qZSI [14], SL-ZSI [15], DA-qZSI [14], rSL-qZSI/cSL-qZSI [17], EB-ZSI [21], EB-qZSI [22] and the proposed scheme. As can be seen from Fig. 6, the proposed inverter produce the same boost factor with EB-ZSI and EB-qZSI, but higher than those of the other six non-coupled inductor-based (q)ZSIs with the same shoot-through duty ratio.

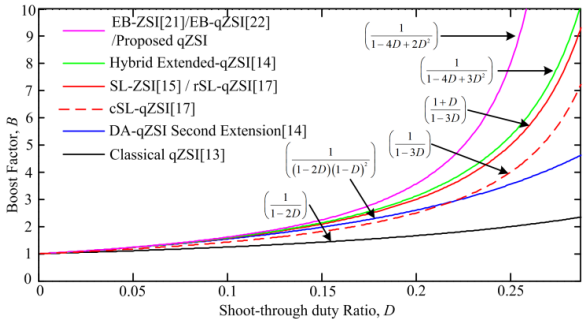



Fig. 6 Comparison of the boost factor $B$ for these high boost (q)ZSIs.

## IV. Parameter Design of Passive and Active Components

Normally, the parameters design of the passive/active components in a converter mainly depends on their rated voltages and rated currents. Hence, the voltage and current stresses of each component will be deduced at first.

### A. Voltage Stress of Each Component

According to the operating principle analysis in Section III. During the shoot-through state, diodes $D_1$, $D_3$ and $D_4$ are turned off. From Fig. 4(a), the voltage stress of $D_1$ , $D_3$ and $D_4$ can be obtained as

$$V_{D_1} = V_{D_4} = \frac{1-D}{1-4D+2D^2} V_{dc} \quad V_{D_3} = \frac{1}{1-4D+2D^2} V_{dc} \tag{14}$$

During the non-shoot-through state, diodes $D_1$, $D_3$ and $D_4$ are on, while diodes $D_2$ and $D_5$ are off, from Fig. 4(b), the voltage stress of diodes $D_2$ and $D_5$ are

$$V_{D_2} = V_{D_5} = \frac{D}{1-4D+2D^2} V_{dc} \tag{15}$$

While, the corresponding capacitor voltage stresses have derived in Section III.

### B. Current Stress of Each Component

Based on the ampere-second balance property of the capacitor $C$, the average current through the capacitor in a switch period is zero. Applying KCL to capacitors $C_1$, $C_2$, $C_3$ and $C_4$ in Fig. 4(a) and 4(b), respectively. Thus, we have

$$\begin{cases} \int_0^{DT_s} \left(-i_{L1\_on}\right) dt + \int_{DT_s}^{T_s} \left(i_{L2\_off} - i_{L1\_off}\right) dt = 0 \\ \int_0^{DT_s} \left(-i_{L2\_on}\right) dt + \int_{DT_s}^{T_s} \left(i_{L1\_off} + i_{L4\_off} - i_{L2\_off} - I_i\right) dt = 0 \\ \int_0^{DT_s} \left(-i_{L3\_on}\right) dt + \int_{DT_s}^{T_s} \left(i_{L1\_off} + i_{L4\_off} - i_{L3\_off} - I_i\right) dt = 0 \\ \int_0^{DT_s} \left(-i_{L4\_on}\right) dt + \int_{DT_s}^{T_s} \left(i_{L3\_off} - i_{L4\_off}\right) dt = 0 \end{cases} \tag{16}$$

where $i_{L\_on}$, $i_{L\_off}$ are the inductor currents during shoot-through state and non-shoot-through state, respectively. Assuming that the inductors are large enough, and the inductor currents in each operating state changed linearly. Therefore, the average inductor current can be expressed as

$$I_L = \frac{1}{DT_s} \int_0^{DT_s} i_{L\_on} dt = \frac{1}{(1-D)T_s} \int_{DT_s}^{T_s} i_{L\_off} dt \tag{17}$$

Combining (17) with (16) and solving (16),we have

$$I_{L_1} = I_{L_4} = \frac{(1-D)^2}{1-4D+2D^2} I_{PN} \quad I_{L_2} = I_{L_3} = \frac{1-D}{1-4D+2D^2} I_{PN} \tag{18}$$

Then, from Fig. 4(a), the current flow through diodes $D_2$ and $D_5$ are

$$I_{D_2} = I_{D_5} = I_{L_3} = \frac{1-D}{1-4D+2D^2} I_{PN} \tag{19}$$

From Fig. 4(b), the current flow through diodes $D_1$, $D_3$ and $D_4$ are

$$I_{D_1} = I_{D_4} = \frac{1-D}{1-4D+2D^2} I_{PN} \quad I_{D_3} = \frac{1}{1-4D+2D^2} I_{PN} \tag{20}$$

### C. Parameter Design of Inductors

By neglecting the power losses of active/passive components and the effects of ac side harmonics, the average power transferred from the dc link will be equal to the power delivered to the three phase ac load over one ac cycle, that is

$$\hat{V}_{PN}(1-D) I_{PN} = \frac{3}{2} \hat{V}_{ac} \hat{I}_{ac} \cos\phi \tag{21}$$

where $\hat{I}_{ac}$ is the peak phase current of ac side, $\cos\phi$ is the power factor on the ac side of the inverter. Based on the constant boost control method in [8], $M=2(1-D)/\sqrt{3}$. Substituting $M$ into (21), one can obtain $I_{PN}$ and the required shoot-through duty ratio $D$,

$$I_{PN} = \frac{\sqrt{3}}{2} \hat{I}_{ac} \cos\phi \quad D = \frac{4\sqrt{3}\hat{V}_{ac} - V_{dc} - \sqrt{V_{dc}^2 + 24\hat{V}_{ac}^2}}{4\sqrt{3}\hat{V}_{ac}} \tag{22}$$

During the shoot-through state, the capacitors and dc input voltage source discharge the energy to inductors. From (1)-(2),

we have

$$u_{L1\_on} = u_{L4\_on} = L_1 \frac{di_{L_1}}{dt} = V_{dc} + V_{C_1} \tag{23}$$

$$u_{L2\_on} = u_{L3\_on} = L_2 \frac{di_{L_2}}{dt} = V_{dc} + V_{C_2} \tag{24}$$

where $dt=DT_s/K_{sh}$, and $K_{sh}$ is the number of the shoot-through states in a switching period. $di_L=x_L\%I_L$, and $x_L\%$ is the given permitted fluctuation range of the inductor current. Substituting (8), (9) into (23) and (24),respectively. Then, the inductors can be designed by

$$L_1 = L_4 = \frac{V_{dc}T_s}{x_L\%I_{L_1}K_{sh}} \frac{D(1-D)}{1-4D+2D^2} \tag{25}$$

$$L_1 = L_4 = \frac{V_{dc}T_s}{x_L\%I_{L_1}K_{sh}} \frac{D(1-D)}{1-4D+2D^2} \tag{26}$$

For a practical three phase inverter application system, $\hat{V}_{ac}$, $\hat{I}_{ac}$, cos$\phi$ and $V_{dc}$ are usually fixed. Therefore, substituting (22) into (25) and (26), the inductances of $L_1$, $L_2$, $L_3$ and $L_4$ can be designed by

$$L_1 = L_4 = \frac{2V_{dc}T_s\left(4\sqrt{3}\hat{V}_{ac} - V_{dc} - \sqrt{V_{dc}^2 + 24\hat{V}_{ac}^2}\right)}{\sqrt{3}x_L\%K_{sh}\hat{I}_{ac}\cos\phi\left(V_{dc} + \sqrt{V_{dc}^2 + 24\hat{V}_{ac}^2}\right)} \tag{27}$$

$$L_{2,3} = \frac{V_{dc}T_s\left(4\sqrt{3}\hat{V}_{ac} - V_{dc} - \sqrt{V_{dc}^2 + 24\hat{V}_{ac}^2}\right)\left(V_{dc} + \sqrt{V_{dc}^2 + 24\hat{V}_{ac}^2}\right)}{24\sqrt{3}x_L\%K_{sh}\hat{I}_{ac}\cos\phi\hat{V}_{ac}^2} \tag{28}$$

**Table I**

Voltage and current stresses of the proposed inverter

| Proposed qZSI | | | |
|---|---|---|---|
| Parameter | Voltage Stress | Parameter | Current Stress |
| $C_1$, $C_4$ | $\frac{D(3-2D)}{1-4D+2D^2}V_{dc}$ | $L_1$, $L_4$ | $\frac{(1-D)^2}{1-4D+2D^2}I_{PN}$ |
| $C_2$, $C_3$ | $\frac{D(2-D)}{1-4D+2D^2}V_{dc}$ | $L_2$, $L_3$ | $\frac{(1-D)}{1-4D+2D^2}I_{PN}$ |
| $D_1$, $D_4$ | $\frac{(1-D)}{1-4D+2D^2}V_{dc}$ | $D_1$, $D_4$ | $\frac{(1-D)}{1-4D+2D^2}I_{PN}$ |
| $D_2$, $D_5$ | $\frac{D}{1-4D+2D^2}V_{dc}$ | $D_2$, $D_5$ | $\frac{(1-D)}{1-4D+2D^2}I_{PN}$ |
| $D_3$ | $\frac{1}{1-4D+2D^2}V_{dc}$ | $D_3$ | $\frac{1}{1-4D+2D^2}I_{PN}$ |

### D. Parameter Design of Capacitors

Similarly, during the shoot-through state, the capacitors are connected with the inductors in series. From Fig. 4(a), the capacitor currents are equal to the inductor currents. Hence,

$$C_1 = C_4 = \frac{DT_s}{x_C\%V_{C1}K_{sh}} \frac{(1-D)^2}{1-4D+2D^2} I_{PN} \tag{29}$$

$$C_2 = C_3 = \frac{DT_s}{x_C\%V_{C2}K_{sh}} \frac{1-D}{1-4D+2D^2} I_{PN} \tag{30}$$

where $x_C\%$ is the given permitted fluctuation range of the capacitor voltage. Substituting (22) into (29) and (30), the capacitances of $C_1$, $C_2$, $C_3$ and $C_4$ can be designed by

$$C_1 = C_4 = \frac{T_s\hat{I}_{ac}\cos\phi\left(V_{dc} + \sqrt{V_{dc}^2 + 24\hat{V}_{ac}^2}\right)^2}{16x_C\%K_{sh}V_{dc}\hat{V}_{ac}\left(2\sqrt{3}\hat{V}_{ac} + V_{dc} + \sqrt{V_{dc}^2 + 24\hat{V}_{ac}^2}\right)} \tag{31}$$

$$C_2 = C_3 = \frac{\sqrt{3}T_s\hat{I}_{ac}\cos\phi\left(V_{dc} + \sqrt{V_{dc}^2 + 24\hat{V}_{ac}^2}\right)}{2x_C\%K_{sh}V_{dc}\left(4\sqrt{3}\hat{V}_{ac} + V_{dc} + \sqrt{V_{dc}^2 + 24\hat{V}_{ac}^2}\right)} \tag{32}$$

Therefore, for a given particular three-phase inverter application system, based on (27), (28), (31) and (32), the inductors and capacitors can be determined directly.

### E. Parameter Design of Diodes

Generally, the parameter of diodes can be selected according to their voltage and current stresses, as summarized in Table I, to keep them operating in their safe operating area.

## V. Performance Comparison With Other High Boost ZSI Topologies

The performance of the proposed inverter is compared with those of the conventional non-isolated high boost (q)ZSIs. The comparison analysis of the boost abilities, the number of the components used at the impedance network, the voltage and current stresses will be presented in a detailed way.

### A. Comparison of the Boost Abilities

The relationship between the boost factor $B$ and the shoot-through duty ratio $D$ for these eight (q)ZSIs has been plotted and compared in Fig. 6. When the constant boost control method in [8] is applied to the proposed topology, the shoot-through duty ratio $D$ will be limited by the modulation index $M$, that is, $D$=1-$\sqrt{3}M/2$. Thus, the corresponding buck-boost factor $G$ can be expressed as

$$G = MB = \frac{2M}{3M^2 - 2} \tag{33}$$

Fig. 7 shows a plot of the buck-boost factor $G$ versus the modulation index $M$ for these nine topologies. As shown in Fig. 7, for obtaining the same buck-boost factor, the proposed qZSI can use higher modulation index for the inverter bridge. Therefore, this inverter can output higher quality voltage waveforms with lower total harmonic distortion (THD).

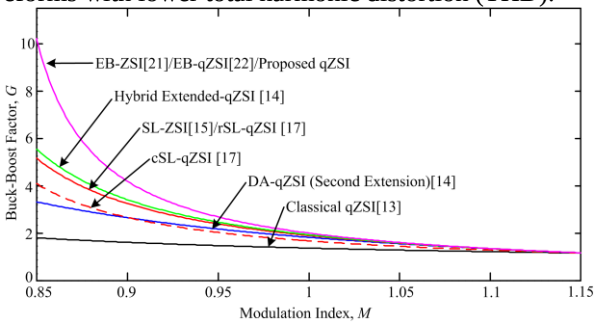



Fig. 7 Buck-boost factor $G$ versus the modulation index $M$.

### B. Comparison of the Number of Components

Table II shows the comparison of the number of components used at the impedance network for these high boost (q)ZSIs. From this table, it can be seen that the proposed topology has the same number of passive and active components with DA-qZSI, EB-ZSI and the EB-qZSI, and has the similar number of passive/active components with the other four topologies. In addition, for these eight high boost (q)ZSIs, the total number of the components used at the impedance network is same, which is 13. Therefore, the number of the components

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2018.2873805, IEEE Journal of Emerging and Selected Topics in Power Electronics



used at the proposed topology is no more than the other high boost (q)ZSIs.

**Table II**

Comparison of the number of components used at the impedance network

| | DA-qZSI [14] | SL-ZSI[15] | rSL-qZSI /cSL-qZSI[17] | Hybrid [14] Extended-qZSI | Enhanced Boost ZSI[21] | Enhanced Boost-qZSI[22] | Proposed qZSI |
|---|---|---|---|---|---|---|---|
| Inductors | 4 | 4 | 4 | 4 | 4 | 4 | 4 |
| Capacitors | 4 | 2 | 2 | 5 | 4 | 4 | 4 |
| Diodes | 5 | 7 | 7 | 4 | 5 | 5 | 5 |

### C. Comparison of Inductance and Capacitance Values

In order to make the comparison more clearly, Table III and Table IV shows the detailed comparison of inductance values and capacitance values, respectively, for these eight topologies to achieve the same inductor current ripple and capacitor voltage ripple under the same boost factor. As shown in Table III, two parameters $K_i = V_{dc}/k_L \bar{i}_{in} f_o$ and $K_v = \bar{i}_{in}/k_V V_{dc} f_o$ are defined to simplify the expressions of inductances and capacitances. In this two parameters $K_i$ and $K_v$, the factor $k_L$ is defined as the ratio of the peak-to-peak inductor current ripple to the average inductor current, and $k_V$ is defined as the ratio of the peak-to-peak capacitor voltage ripple to the average capacitor voltage, $\bar{i}_{in}$ is the average value of the dc input current, and $f_o$ is the operating frequency of the proposed inverter, which is twice the switching frequency $f_s$=10kHz.

**Table III**

Comparison of inductance and capacitance for these high boost (q)ZSIs

| | SL-ZSI [15]/ rSL-qZSI[17] | DA-qZSI [14] (second extension) | cSL-qZSI[17] | Hybrid[14] Extended-qZSI | Enhanced Boost ZSI [21] | Enhanced Boost -qZSI [22] | Proposed qZSI |
|---|---|---|---|---|---|---|---|
| Inductances | $L=\frac{D(1-D)(1+D)}{1-3D}K_i$<br>$L_1=L_2=L_3=L_4=L$ | $L_{1,2}=\frac{D}{(1-2D)(1-D)^3}K_i$<br>$L_3=\frac{D}{(1-D)^2}K_i$<br>$L_4=DK_i$ | $L_1=\frac{D(1-3D^2)}{(1+D)(1-3D)}K_i$<br>$L_{2,4}=\frac{D(1-D)}{(1+D)(1-3D)}K_i$<br>$L_3=\frac{2D^2}{(1+D)(1-3D)}K_i$ | $L_{1,2,3}=\frac{D}{(1-D)(1-3D)}K_i$<br>$L_4=DK_i$ | $L_{1,2}=\frac{D(1-D)^2}{1-4D+2D^2}K_i$<br>$L_{3,4}=\frac{D}{1-4D+2D^2}K_i$ | $L_{1,2}=\frac{D(1-D)^2}{1-4D+2D^2}K_i$<br>$L_{3,4}=\frac{D}{1-4D+2D^2}K_i$ | $L_{1,4}=\frac{D}{1-4D+2D^2}K_i$<br>$L_{2,3}=\frac{D(1-D)^2}{1-4D+2D^2}K_i$ |
| Capacitances | $C_1'=\frac{2D(1-3D)}{(1-D)(1+D)}K_v$<br>$C_1=C_2=C_1'$ (for SL-ZSI)<br>$C_2'=\frac{1-3D}{1+D}K_v$<br>$C_1=C_1'\ C_2=C_2'$ (for rSL-ZSI) | $C_{1,2}=(1-2D)(1-D)^4K_v$<br>$C_3=2D(1-D)^4K_v$<br>$C_4=D(1-D)^2K_v$ | $C_1=\frac{2D(1+D)(1-3D)}{(1-D)}K_v$<br>$C_2=(1+D)(1-3D)K_v$ | $C_{1,3}=2(1-3D)(1-D)^2K_v$<br>$C_2=(1-3D)(1-D)^2K_v$<br>$C_4=3D(1-D)^2K_v$ | $C_{1,2}=\frac{D(1-4D+2D^2)}{(1-D)^2}K_v$<br>$C_{3,4}=D(1-4D+2D^2)K_v$ | $C_1=\frac{D(2-D)(1-4D+2D^2)}{(1-2D+D^2)}K_v$<br>$C_{2,4}=(1-4D+2D^2)K_v$<br>$C_3=\frac{D(1-D)(1-4D+2D^2)}{(1-3D+D^2)}K_v$ | $C_{1,4}=\frac{(1-D)(1-4D+2D^2)}{3-2D}K_v$<br>$C_{2,3}=\frac{(1-4D+2D^2)}{2-D}K_v$ |

**Table IV**

Comparison of the inductance and capacitance values for producing the same boost factor $B$=5.86

| | SL-ZSI [15] | DA-qZSI [14] | rSL-qZSI[17] | cSL-qZSI[17] | Hybrid[14] Extended-qZSI | Enhanced Boost ZSI[21] | Enhanced Boost-qZSI[22] | Proposed qZSI |
|---|---|---|---|---|---|---|---|---|
| $D_{sh}$ | 0.2616 | 0.3171 | 0.2616 | 0.2765 | 0.2568 | 0.235 | 0.235 | 0.235 |
| $B$ | 5.86 | 5.86 | 5.86 | 5.86 | 5.86 | 5.86 | 5.86 | 5.86 |
| $G=MB$ | 5 | 4.62 | 5 | 4.895 | 5.03 | 5.18 | 5.18 | 5.18 |
| Inductance Values | $L_{1,2,3,4}$=0.575mH | $L_{1,2}$=1.3776mH<br>$L_3$=0.345mH<br>$L_4$=0.161mH | $L_{1,2,3,4}$=0.575mH | $L_1$=0.495mH<br>$L_{2,4}$=0.465mH<br>$L_3$=0.356mH | $L_{1,2,3}$=0.762mH<br>$L_4$=0.131mH | $L_{1,2}$=0.695mH<br>$L_{3,4}$=0.407mH | $L_{1,2}$=0.695mH<br>$L_{3,4}$=0.407mH | $L_{1,4}$=0.695mH<br>$L_{2,3}$=0.407mH |
| Capacitance Values | $C_1$=$C_2$=150uF | $C_1$=$C_2$=100uF<br>$C_3$=170uF<br>$C_4$=185uF | $C_1$=150uF<br>$C_2$=211uF | $C_1$=205uF<br>$C_2$=270uF | $C_1$=$C_3$=315uF<br>$C_2$=157uF<br>$C_4$=526uF | $C_{1,2}$=85uF<br>$C_{3,4}$=50uF | $C_1$=150uF<br>$C_{2,4}$=222uF<br>$C_3$=110uF | $C_{1,4}$=63uF<br>$C_{2,3}$=119uF |

For the dc input voltage of 60V, $f_o$=20kHz, $\bar{i}_{in}$ =14.82 A, the factors $k_L$=40% and $k_V$=1%, the required shoot-through duty ratio $D$ to achieve $B$=5.86, and the corresponding inductance and capacitance values for these eight topologies are tabulated in Table IV. From this table, it can be seen that the summarized value of inductances ($L_1$, $L_2$, $L_3$, $L_4$) required at the proposed topology is slightly higher than the cSL-qZSI, same as the EB-ZSI [21] and EB-qZSI [22], but lower than the other four high boost (q)ZSIs. Additionally, the summarized capacitance values of the proposed topology is a little higher than the SL-ZSI and the EB-ZSI, but much lower than that of the other four topologies.

### D. Comparison of the Voltage and Current Stresses

For the impedance network-type power inverters, different control method, dc input voltage, and the load conditions would provide varied current and voltage stresses. For exact comparison, the ac side circuit of these seven (q)ZSI topologies is simplified as an equivalent dc load , which is represented by an inductive load impedance ($Z_l$=$R_l$+$sL_l$) plus a single active switch [6].

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2018.2873805, IEEE Journal of Emerging and Selected Topics in Power Electronics



**Table V**
Comparison of voltage and current stresses for these high boost (q)ZSIs

| | DA-qZSI [14] | SL-ZSI[15]/ rSL-qZSI[17] | cSL-qZSI [17] | Hybrid [14] Extended-qZSI | Enhanced Boost ZSI [21] | Enhanced Boost-qZSI [22] | Proposed qZSI |
|---|---|---|---|---|---|---|---|
| Boost Factor | $\frac{1}{(1-2D)(1-D)^2}$ | $\frac{1+D}{1-3D}$ | $\frac{1}{1-3D}$ | $\frac{1}{1-4D+3D^2}$ | $\frac{1}{1-4D+2D^2}$ | $\frac{1}{1-4D+2D^2}$ | $\frac{1}{1-4D+2D^2}$ |
| Capacitor Voltage Stresses ($V_C/V_{dc}$) | $DB$<br>$(1\text{-}2D)B$<br>$(1\text{-}D)(1\text{-}2D)B$ | $(1–D)B/(1+D)$<br>$2DB/(1+D)$ | $(1–D)B/(1+D)$<br>$2DB/(1+D)$ | $DB$<br>$(1\text{-}3D)B$ | $(1–D)^2B$<br>$(1–D)B$ | $(1–D)^2B$<br>$D(1–D)B$<br>$D(2–D)B$<br>$(1–3D+D^2)B$ | $D(2–D)B$<br>$D(3–2D)B$ |
| Diode Voltage Stresses ($V_D/V_{dc}$) | $B$<br>$2DB$<br>$(1\text{-}2D)B$<br>$D(3–2D)B$<br>$(1\text{-}D)(1\text{-}2D)B$ | $B$<br>$(1–D)B/(1+D)$<br>$DB/(1+D)$ | $B$<br>$2D^2B/(1\text{-}D^2)$<br>$DB/(1+D)$<br>$2DB/(1+D)$<br>$(1–D)B/(1+D)$<br>$(1\text{-}2D\text{-}D^2)B/(1\text{-}D^2)$ | $B$<br>$(1\text{-}3D)B$<br>$3DB$ | $B$<br>$DB$<br>$(1–D)B$ | $B$<br>$DB$<br>$(1–D)B$ | $B$<br>$DB$<br>$(1–D)B$ |
| Buck-Boost Factor ($G$=$MB$) | $\frac{4}{3\sqrt{3}M^2-3M}$ | $\frac{4M-\sqrt{3}M^2}{3\sqrt{3}M-4}$ | $\frac{2M}{3\sqrt{3}M-4}$ | $\frac{4}{9M-4\sqrt{3}}$ | $\frac{2M}{3M^2-2}$ | $\frac{2M}{3M^2-2}$ | $\frac{2M}{3M^2-2}$ |
| Inductor Current Stresses ($I_L/I_{PN}$) | $(1–D)B$<br>$(1–D)^2B$<br>$(1–D)^3B$ | $(1–D)B/(1+D)$ | $(1–D)B$ | $(1–D)B$<br>$(1–D)^2B$ | $(1–D)B$<br>$(1–D)^2B$ | $(1–D)B$<br>$(1–D)^2B$ | $(1–D)B$<br>$(1–D)^2B$ |
| Shoot-through Current Stresses ($I_{sh}/I_{PN}$) | $[2\text{-}D+2(1\text{-}D)^2](1–D)B$ | $4(1–D)B/(1+D)$ | $4(1–D)B$ | $[1–D+3(1–D)^2]B$ | $2[1–D+(1–D)^2]B$ | $2[1–D+(1–D)^2]B$ | $2[1–D+(1–D)^2]B$ |
| Average DC-link Current ($I_{PN}$) | $\frac{(1-D)\hat{V}_{PN}}{R_l}$ | $\frac{(1-D)\hat{V}_{PN}}{R_l}$ | $\frac{(1-D)\hat{V}_{PN}}{R_l}$ | $\frac{(1-D)\hat{V}_{PN}}{R_l}$ | $\frac{(1-D)\hat{V}_{PN}}{R_l}$ | $\frac{(1-D)\hat{V}_{PN}}{R_l}$ | $\frac{(1-D)\hat{V}_{PN}}{R_l}$ |

Assuming that these eight topologies operate under the same modulation index, dc input voltage, and output power. Then, the corresponding current and voltage stresses on the passive components and switching devices are summarized in Table V. Where $I_L$ is the average inductor current, $I_l$ is the average load current during a switching period, and $I_{sh}$ is the shoot-through current flow through the inverter bridge during the shoot-through state. Due to the shoot-through current $I_{sh}$ is higher than the average load current $I_l$, thus, $I_{sh}$ is defined as the current stress across the switching devices in the inverter bridge.

The voltage stress across the active switching devices can be defined as the ratio of the peak dc-link voltage $V_{PN}$ to an equivalent dc voltage $GV_{dc}$, as illustrated in [8], the voltage ratio represents the cost to achieve the desired voltage boost under the same dc input voltage condition. The corresponding voltage stress ratio of the proposed inverter can be derived as

$$\frac{\hat{V}_{PN}}{GV_{dc}}=\frac{BV_{dc}}{GV_{dc}}=\frac{3G}{1+\sqrt{1+6G^2}} \tag{34}$$

Fig. 8 shows the active switching voltage stress comparison for these nine topologies. It can be seen from this figure, the proposed inverter has the same switching voltage stress with EB-ZSI and EB-qZSI, but much lower than those of the other six (q)ZSIs for the same buck-boost factor $G$.

The capacitor voltage stress comparison and the inductor current stress comparison are presented in Fig. 9. Here, the capacitor voltage stress is defined as the ratio of the capacitor

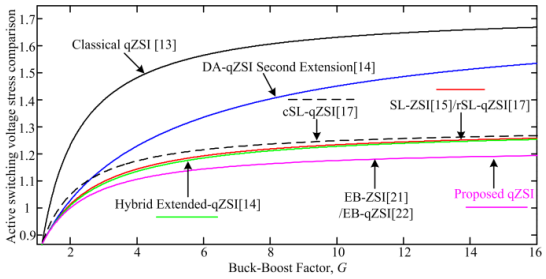



Fig. 8 Active switching voltage stress comparison.

voltage to an equivalent dc voltage $GV_{dc}$ [21]. It can be seen from Fig. 9(a) that the proposed inverter has lower capacitor voltage stress than classical-qZSI and the EB-ZSI [21]. Although the capacitor voltage stress of $V_{C1}$ and $V_{C4}$ are higher than the same value of in DA-qZSI and hybrid extended-qZSI. But the capacitor voltage stress of $V_{C2}$(=$V_{C3}$) is much lower than the same value in SL-ZSI and the rSL-qZSI/cSL-qZSI. From Fig. 9(b), it can be observed that for obtaining the same buck-boost factor $G$, the inductor current stress of $I_{L2}$(=$I_{L3}$) of the proposed method is the same as the cSL-qZSI, DA-qZSI ($I_{L4}$), EB-ZSI ($I_{L1}$,$I_{L2}$) and the hybrid extended-qZSI ($I_{L4}$). The inductor current stress of $I_{L1}$(=$I_{L4}$) of the proposed inverter is same as the EB-ZSI ($I_{L3}$,$I_{L4}$), but lower than the classical-qZSI, the SL-ZSI and the rSL-qZSI. This is because the proposed topology can produce higher buck-boost factor $G$ by using a small shoot-through duty ratio.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2018.2873805, IEEE Journal of Emerging and Selected Topics in Power Electronics



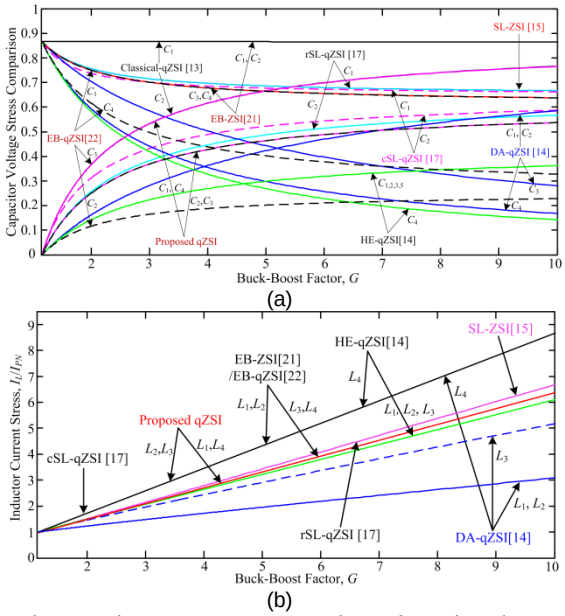



Fig. 9 Voltage and current stress comparison of passive elements. (a) Capacitor voltage stress comparison, (b) Inductor current stress comparison.

The total capacitor voltage stress and the total inductor current stress have been compared in Fig. 10. From Fig. 10(a), the total capacitor voltage stress of the proposed inverter is lower than that of the EB-ZSI, but higher than those of the other six topologies when the buck-boost factor $G$ is larger than 3. From Fig. 10(b), it can be seen that the total inductor current stress of the proposed method is lower than the cSL-qZSI, same as the EB-ZSI and EB-qZSI, but a little higher than the DA-qZSI, rSL-qZSI and the SL-ZSI.

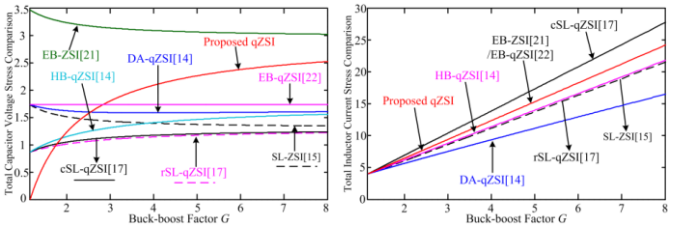



Fig. 10 (a) Total capacitor voltage stress comparison, (b) Total inductor current stress comparison.

In order to better quantify the current and voltage stresses of diodes and MOSFEs in the proposed topology, total switching device power (SDP) is calculated. The SDP of a switching device is defined as the product of its current stress and voltage stress. The total SDP of an inverter system is expressed as the summation of SDP of all the switching components used in the circuit, which is a good measure for the total semiconductor device requirement, thus an important cost indicator of an inverter system [3]. Based on the definition of the total peak and average SDP in [3]. The average SDP and peak SDP (for MOSFETs) of the proposed inverter are derived as

$$\begin{cases} SDP_{(av\_MOSFETs)} = \dfrac{2P_{out}\left(4-3M^2\right)}{3M^2-2} + \dfrac{4\sqrt{3}P_{out}}{\cos\phi\pi} \\ SDP_{(pk\_MOSFETs)} = \max\left(\dfrac{4P_{out}}{\cos\phi M} + \dfrac{4P_{out}\left(2+\sqrt{3}M\right)}{3M^2-2}, \dfrac{8P_{out}}{\cos\phi M}\right) \end{cases} \tag{35}$$

where $P_{\text{out}}$ is the inverter's output power, $\cos\phi$ is the load power factor of ac side.

Based on (35), the comparison of $SDP_{(\text{av-MOSFETs})}$ and $SDP_{(\text{pk-MOSFETs})}$ factors for these eight topologies have been plotted in Fig. 11. From Fig. 11(a), it can be seen that the peak SDP of the proposed method is lower than the cSL-qZSI, same as the EB-ZSI and EB-qZSI, but slightly higher than the other four topologies. From Fig. 11(b), it is clear that the proposed inverter has the lowest average SDP for MOSFETs than those of the other qZSIs.

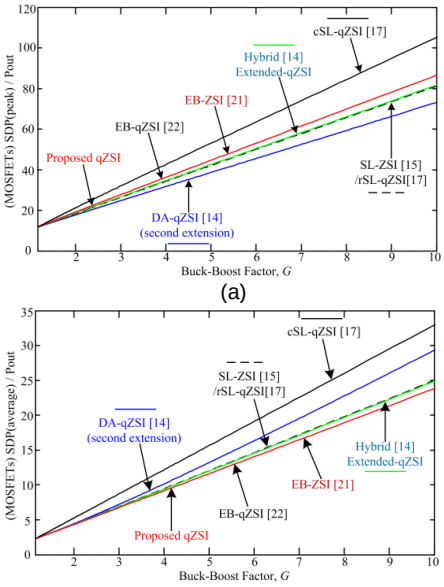



Fig. 11 SDP comparison for active MOSFETs. (a) SDP(peak) comparison, (b) SDP(average) comparison.

Similarly, the total average SDP and peak SDP for diodes are calculated as follows:

$$\begin{cases} SDP_{(av\_diodes)} = \dfrac{3-4D+4D^2}{1-4D+2D^2} P_{out} \\ SDP_{(pk\_diodes)} = \dfrac{3-2D}{(1-D)\left(1-4D+2D^2\right)} P_{out} \end{cases} \tag{36}$$

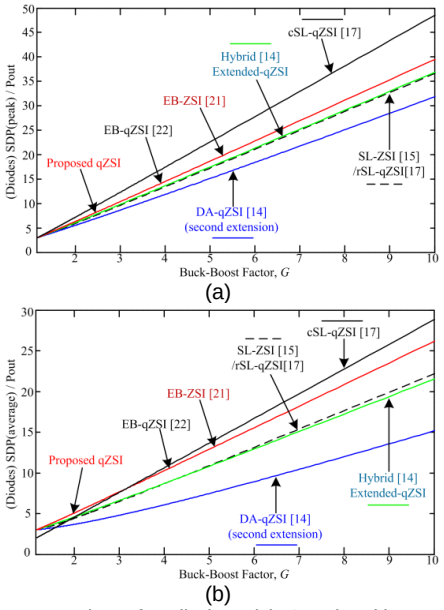



Fig. 12 SDP comparison for diodes. (a) SDP(peak) comparison, (b) SDP(average) comparison.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2018.2873805, IEEE Journal of Emerging and Selected Topics in Power Electronics



Fig. 12 shows the comparison of the average SDP and peak SDP of diodes for these high boost qZSIs. From this figure, it can be seen that for the same buck-boost factor, the $SDP_{(av\_diodes)}$ and $SDP_{(pk\_diodes)}$ of the proposed method are slightly higher than the DA-qZSI, HB-qZSI and the SL-ZSI/rSL-qZSI, lower than that of the cSL-qZSI, but same as the EB-ZSI and EB-qZSI.

### *E. Component Stress Factor (CSF) Comparison*

The component stress factor (CSF) in each component of each converter have been calculated and compared in this section. The definition and calculation process of the component stress factor (CSF) have been described in [34]. Based on the definition in [34], the CSF is calculated with the same component weight for all the components inside each of the topologies. The resources to be assigned are selected as one unit ( $\sum_j W_j = 1$ ) and distributed equally between the components of the same type. Then, the total inductors' winding component stress factor (WCSF), capacitors' component stress factor (CCSF), diodes' component stress factor (DCSF) and the total active semiconductors' component stress factor (SCSF) of the proposed inverter can be calculated and derived in the following:

$$\begin{cases} \mathrm{WCSF} = \dfrac{\sum_j W_j}{W_i} \cdot \dfrac{V_{L\max}^2 I_{Lrms}^2}{P^2} = \dfrac{64D^2(1-D)^4}{\left(1-4D+2D^2\right)^2} \\ \mathrm{DCSF} = \dfrac{\sum_j W_j}{W_i} \cdot \dfrac{V_D^2 I_{Drms}^2}{P^2} = \dfrac{10(1-D)^4+10D^3(1-D)+5}{(1-D)\left(1-4D+2D^2\right)^2} \\ \mathrm{CCSF} = \dfrac{\sum_j W_j}{W_i} \cdot \dfrac{V_{pk}^2 I_{Crms}^2}{P^2} = \dfrac{8D^3\left[(1-D)^2(3-2D)^2+(2-D)^2\right]}{(1-D)\left(1-4D+2D^2\right)^2} \\ \mathrm{SCSF} = \dfrac{\sum_j W_j}{W_i} \cdot \dfrac{V_{DS}^2 I_{Srms}^2}{P^2} = 16\left[\dfrac{D(2-D)^2}{\left(1-4D+2D^2\right)^2} + \dfrac{4(1-D)}{\cos^2\phi\pi^2 M^2}\right] \end{cases} \quad (37)$$

Based on (37), the CSF comparison between the proposed inverter and the other seven high boost qZSIs have been plotted and shown in Fig. 13. From Fig.13(a), it can be seen that the total inductors' winding component stress factor (WCSF) of the proposed inverter is lower than the cSL-qZSI [17], same as the EB-ZSI [21] and the EB-qZSI [22], but a little higher than the other four inverter topologies. The total capacitors' component stress factor (CCSF) comparison is shown in Fig. 13(b). It can be observed that the proposed qZSI only has a little higher CCSF than the DA-qZSI [14], same as the EB-ZSI [21], but much lower than those of the other five topologies (SL-ZSI, rSL-qZSI, cSL-qZSI, HB-qZSI and the EB-qZSI). Fig. 13(c) shows the total diodes' component stress factor (DCSF) comparison. From this figure, one can find that the proposed inverter has the same DCSF as the EB-ZSI/EB-qZSI, but much lower than those of the other five topologies. The total active MOSFETs' component stress factor (SCSF) comparison is shown in Fig. 13(d), it can be found that the SCSF of the proposed method is much lower than the cSL-qZSI, almost same as the other six topologies.

In addition, the specific CSF values of different components for these eight high boost qZSIs have been calculated and shown in Table VI when they produce the same buck-boost factor $G$=5.18. From this table, one can get the same conclusion as it is derived from Fig. 13.

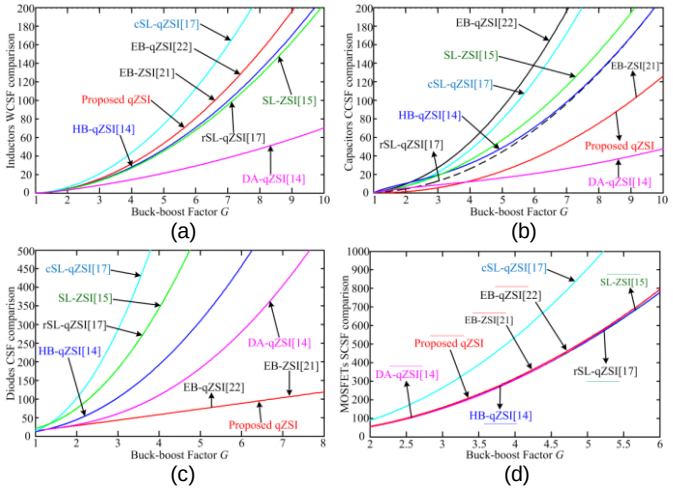



Fig. 13 Component stress factor (CSF) comparison between the proposed qZSI and the other high boost inverters. (a) Inductors' CSF comparison, (b) Capacitors' CSF comparison, (c) Diodes' CSF comparison, (d) MOSFETs' CSF comparison.

**Table VI**

Comparison of the CSF values for these high boost qZSIs under the same buck-boost factor $G$=5.18

| | DA-qZSI [14] | SL-ZSI[15] | rSL-qZSI[17] | cSL-qZSI[17] | Hybrid [14] Extended-qZSI | Enhanced Boost ZSI[21] | Enhanced Boost-qZSI[22] | Proposed qZSI |
|---|---|---|---|---|---|---|---|---|
| $D_{sh}$ | 0.3329 | 0.2642 | 0.2642 | 0.2798 | 0.259 | 0.235 | 0.235 | 0.235 |
| Boost Factor $B$ | 6.724 | 6.095 | 6.095 | 6.229 | 6.05 | 5.86 | 5.86 | 5.86 |
| Buck-boost Factor $G$=$MB$ | 5.18 | 5.18 | 5.18 | 5.18 | 5.18 | 5.18 | 5.18 | 5.18 |
| WCSF | 22.72 | 48.85 | 48.85 | 80.65 | 50.98 | 58.14 | 58.14 | 58.14 |
| CCSF | 16.87 | 61.51 | 48.31 | 86.34 | 52.3 | 25.69 | 99.76 | 25.69 |
| DCSF | 198.7 | 605 | 605 | 1021 | 334.5 | 75.88 | 75.88 | 75.88 |
| SCSF | 565.9 | 558.3 | 558.3 | 981 | 560 | 570.9 | 570.9 | 570.9 |

## VI. Power Loss Analysis and Efficiency Comparison

In order to analyze the power losses of these impedance network-based inverter topologies. The diodes are represented by the ideal diodes in series with their forward voltage drop $V_F$ and their parasitic resistances $r_D$. The MOSFETs are represented by the ideal lossless semiconductor switches in series with the equivalent drain-to-source resistance $r_{DS}$. Inductors and capacitors are represented by ideal passive components with their equivalent series resistances $r_L$ and $r_C$, respectively.

To simplify the power losses calculation of the proposed inverter, some conditions are assumed as follows: 1) Capacitor voltage ripples and inductor current ripples are neglected; 2) Off-state blocking losses of diodes and MOSFETs are ignorable; 3) The ripple losses of capacitors are small enough to be negligible.

### A. MOSFETs' Loss Calculation

Generally, the power losses of active semiconductor switches can be classified into switching power losses during the ON and OFF switching states, and the ohmic conduction power losses, respectively. Therefore, the total switching losses of MOSFETs in the proposed topology is calculated as

$$P_{sw} = \left(t_{on} + t_{off}\right) f_{sw} \frac{2\left(2-D\right)}{1-4D+2D^2} P_{out} \tag{38}$$

where $t_{on}$ is the turn-on delay time, $t_{off}$ is the turn-off delay time, $f_{sw}$ is the switching frequency.

The total conduction power losses of switches can be calculated by

$$P_{cond} = \left[\frac{8}{3} D\left(2-D\right)^2 i_{in}^2 + \frac{1.081\left(1-D\right)P_{out}^2}{M^2 B^2 \left(\cos\phi\right)^2 V_{dc}^2}\right] r_{DS} \tag{39}$$

where $i_{in}$ is the average input current of the dc power supply, $\cos\phi$ is the load power factor of ac side, $r_{DS}$ is on-resistance of MOSFETs.

### B. Diodes' Loss Calculation

Power loss on diode is composed of the conduction loss in forward voltage drop $V_F$ and the loss associated with the forward resistance $r_F$. By assuming that the ripples of the inductor currents are free, then the overall conduction power losses of diodes can be derived as

$$P_{Dloss} = 3V_F i_{in} + \frac{3-2D}{1-D} r_F i_{in}^2 \tag{40}$$

### C. Inductors' Loss Calculation

The power losses in inductors can be segregated into core loss and winding conduction loss. Typically, due to the small ripples of inductor currents, the core loss is negligible when compared with the total power losses of inductors. The winding loss is determined by the winding resistance and the rms value of the current flow through it. Thus, the total conduction power losses in inductors can be calculated as

$$P_{rLloss} = 2r_L i_{in}^2 + 2\left(1-D\right)^2 r_L i_{in}^2 \tag{41}$$

### D. Capacitors' Loss Calculation

By taking the ESR of capacitors into consideration, the total conduction power losses in capacitors is

$$P_{rCloss} = \frac{2D\left(2-2D+D^2\right)}{1-D} r_C i_{in}^2 \tag{42}$$

**Table VII**

Parameters used for power loss calculation and efficiency comparison

| Diode | Semiconductor switch (IGBT) | Inductor core | Copper wire resistivity | ESR of capacitor |
|---|---|---|---|---|
| RURG3060CC | BSM100GB60DLC | KS300125A ($142nH/N^2$) | $1.724\cdot10^{-6}\Omega\cdot cm$ | 110mΩ |

Based on the loss-related parameters that are summarized in Table VII. The comparison of power losses of each component among these eight high boost (q)ZSI topologies are shown in Fig. 14. From Fig. 14(a), it can be seen that the MOSFETs power losses of the proposed topology is same as the EB-ZSI and EB-qZSI, lower than the cSL-qZSI, but slightly higher than the other four topologies. The diode power losses comparison is shown in Fig. 14(b), although the proposed method has a little higher diode loss than the SL-ZSI/rSL-qZSI, DA-qZSI and hybrid extended-qZSI, it would be much lower than the cSL-qZSI. From Fig. 14(c), it can be observed that, for the same buck-boost factor *G*, the inductor loss of the proposed topology is slightly higher than those of the SL-ZSI/rSL-qZSI, DA-qZSI and the HE-qZSI, lower than the cSL-qZSI, but same as the EB-ZSI and EB-qZSI. The capacitor power losses for the proposed inverter, which is shown in Fig. 14(d), is only a little higher than the DA-qZSI, and same as the EB-ZSI, but much lower than those of the other five inverters (EB-qZSI, SL-ZSI, rSL-qZSI/cSL-qZSI, HE-qZSI).

In addition, the power loss distribution percentage of each component in the proposed topology is summarized in Fig. 14(e). It can be concluded that for higher values of the buck-boost factor *G*, the major power losses come from inductors, MOSFETs and capacitors. Among them, the conduction power loss of inductors is obviously the largest. Hence, the higher parasitic resistances of inductors in the power loop will result in higher power losses of the inverter, and finally, leading to lower efficiency.

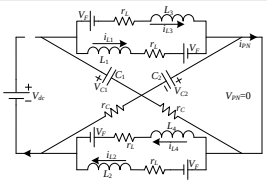
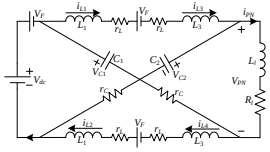
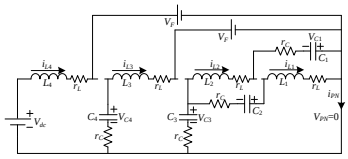
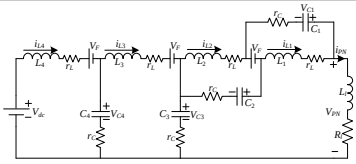
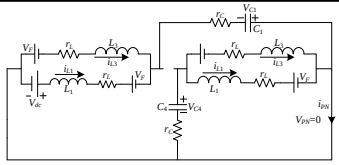
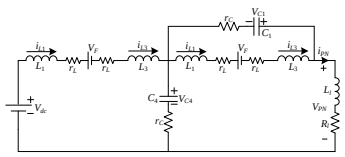
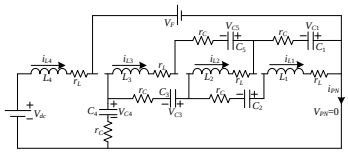
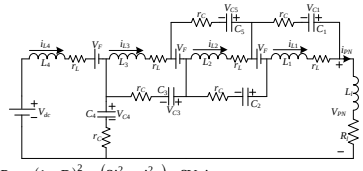
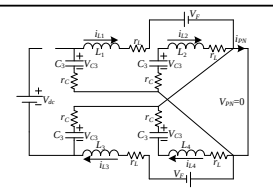
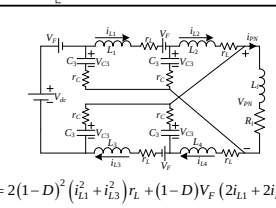
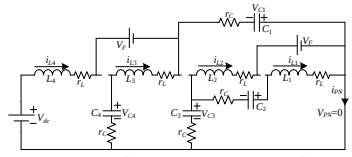
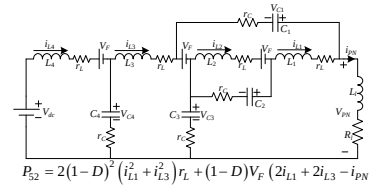
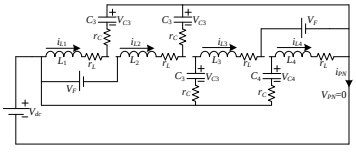
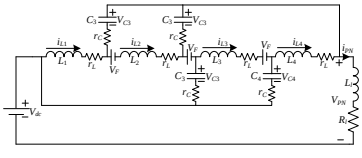
### E. Efficiency Comparison

Based on the power loss analysis of each component, the efficiency expressions of these high boost (q)ZSIs have been derived in Table VIII. Using the parasitic parameters in Table VII, the calculated efficiencies of the proposed scheme and the other high boost inverters versus the buck-boost factor are shown in Fig. 14(f). From the efficiency comparison results in Fig. 14(f), it can be seen that for the same buck-boost factor, the proposed inverter provides higher efficiency than those of the SL-ZSI, rSL-qZSI/cSL-qZSI, hybrid extended-qZSI and the EB-qZSI, same as the EB-ZSI, but lower than that of the DA-qZSI (second extension), this is because it has lower passive and active components' losses than the proposed scheme.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2018.2873805, IEEE Journal of Emerging and Selected Topics in Power Electronics



Table VIII
Derivation of the efficiency expressions for these high boost (q)ZSIs

| Topology | Equivalent circuits and their expressions in Shoot-through state | Equivalent circuits and their expressions in Non-shoot-through state | Efficiency($\eta$) |
|---|---|---|---|
| SL-ZSI[15] |  $P_{11}=4D^2i_L^2\left(r_L+2r_C\right)+4DV_Fi_L$ |  $P_{12}=2\left(1-D\right)^2\left[2i_L^2r_L+\left(i_L-i_{PN}\right)^2r_C\right]+V_F\left(1-D\right)\left(4i_L-i_{PN}\right)$ | $\eta_{SL-ZSI}=\frac{V_{PN}I_{PN}}{P_{11}+P_{12}+V_{PN}I_{PN}}$<br>$\eta_{SL-ZSI}=\frac{1}{A_1+B_1+C_1+1}$<br>$A_1=\frac{4r_L}{R_l}\frac{\left(1-D\right)^3}{\left(1-3D\right)^2}\left[\left(1-D\right)^2+D^2\right]$<br>$B_1=\frac{16r_C}{R_l}\frac{D^2\left(1-D\right)^3}{\left(1-3D\right)^2}$<br>$C_1=\frac{3V_F\left(1-D\right)}{V_{dc}}$ |
| DA-qZSI [14] (second extension) |  $P_{21}=D^2r_L\left(2i_{L1}^2+i_{L3}^2+i_{L4}^2\right)+D^2r_C\left(6i_{L1}^2+i_{L3}^2\right)+DV_F\left(i_{L3}+i_{L4}\right)$ |  $P_{22}=\left(1-D\right)^2r_L\left(2i_{L1}^2+i_{L3}^2+i_{L4}^2\right)+\left(1-D\right)V_F\left(2i_{L1}+i_{L3}+i_{L4}-i_{PN}\right)+\left(1-D\right)^2r_C\left[2\left(i_{L1}-i_{PN}\right)^2+\left(i_{L3}-i_{PN}\right)^2+\left(i_{L4}-i_{L3}\right)^2\right]$ | $\eta_{DA-qZSI}=\frac{V_{PN}I_{PN}}{P_{21}+P_{22}+V_{PN}I_{PN}}$<br>$\eta_{DA-qZSI}=\frac{1}{A_2+B_2+C_2+1}$<br>$A_2=\frac{r_L}{R_l}\frac{2\left(1-D\right)^4+\left(1-D\right)^2+1}{\left(1-D\right)\left(1-2D\right)^2}\left[\left(1-D\right)^2+D^2\right]$<br>$B_2=\frac{2r_C}{R_l}\frac{D^2\left(1-D\right)\left[6\left(1-D\right)^2+1\right]}{\left(1-2D\right)^2}$<br>$C_2=\frac{V_F\left(1-D\right)}{V_{dc}}\left(3-3D+D^2\right)$ |
| cSL-qZSI[17] |  $P_{41}=4D^2i_{L1}^2r_L+8D^2i_{L1}^2r_C+4DV_Fi_{L1}$ |  $P_{42}=4\left(1-D\right)^2i_{L1}^2r_L+\left(1-D\right)V_F\left(4i_{L1}-i_{PN}\right)+2\left(1-D\right)^2\left(i_{L1}-i_{PN}\right)^2r_C$ | $\eta_{cSL-qZSI}=\frac{V_{PN}I_{PN}}{P_{41}+P_{42}+V_{PN}I_{PN}}$<br>$\eta_{cSL-qZSI}=\frac{1}{A_4+B_4+C_4+1}$<br>$A_4=\frac{4r_L}{R_l}\frac{\left(1-D\right)^3}{\left(1-3D\right)^2}\left[\left(1-D\right)^2+D^2\right]$<br>$B_4=\frac{16r_C}{R_l}\frac{D^2\left(1-D\right)^3}{\left(1-3D\right)^2}$<br>$C_4=\frac{3V_F\left(1-D\right)}{V_{dc}}\left(1+D\right)$ |
| Hybrid [14] Extended-qZSI |  $P_{31}=D^2r_L\left(3i_{L1}^2+i_{L4}^2\right)+D^219i_{L1}^2r_C+DV_Fi_{L4}$ |  $P_{32}=\left(1-D\right)^2r_L\left(3i_{L1}^2+i_{L4}^2\right)+3V_Fi_{L1}+\left(1-D\right)^2r_C\left[\left(i_{L1}-i_{PN}\right)^2+\left(\frac{1-2D}{1-D}i_{L1}-i_{PN}\right)^2+\frac{14D^2i_{L1}^2}{\left(1-D\right)^2}\right]$ | $\eta_{Hybrid-qZSI}=\frac{V_{PN}I_{PN}}{P_{31}+P_{32}+V_{PN}I_{PN}}$<br>$\eta_{Hybrid-qZSI}=\frac{1}{A_3+B_3+C_3+1}$<br>$A_3=\frac{r_L}{R_l}\frac{\left(1-D\right)\left[1+3\left(1-D\right)^2\right]}{\left(1-3D\right)^2}\left[\left(1-D\right)^2+D^2\right]$<br>$B_3=\frac{r_C}{R_l}\frac{38D^2\left(1-D\right)^3}{\left(1-3D\right)^2}$<br>$C_3=\frac{V_F\left(1-D\right)}{V_{dc}}\left(3-2D\right)$ |
| Enhanced Boost ZSI [21] |  $P_{41}=2\left[D^2\left(i_{L1}^2+i_{L3}^2\right)\left(r_L+r_C\right)+DV_Fi_{L1}\right]$ |  $P_{42}=2\left(1-D\right)^2\left(i_{L1}^2+i_{L3}^2\right)r_L+\left(1-D\right)V_F\left(2i_{L1}+2i_{L3}-i_{PN}\right)+2\left(1-D\right)^2r_C\left[\left(i_{L1}-i_{L3}\right)^2+\left(2i_{L3}-i_{L1}-i_{PN}\right)^2\right]$ | $\eta_{En-ZSI}=\frac{V_{PN}I_{PN}}{P_{41}+P_{42}+V_{PN}I_{PN}}$<br>$\eta_{En-qZSI}=\frac{1}{A_4+B_4+C_4+1}$<br>$A_4=\frac{2r_L}{R_l}\frac{\left(1-D\right)^3\left[1+\left(1-D\right)^2\right]}{\left(1-4D+2D^2\right)^2}\left[\left(1-D\right)^2+D^2\right]$<br>$B_4=\frac{4r_C}{R_l}\frac{D^2\left(1-D\right)^3\left[1+\left(1-D\right)^2\right]}{\left(1-4D+2D^2\right)^2}$<br>$C_4=\frac{3V_F\left(1-D\right)}{V_{dc}}$ |
| Enhanced Boost-qZSI [22] |  $P_{51}=2D^2\left[\left(i_{L1}^2+i_{L3}^2\right)r_L+\left(i_{L1}^2+2i_{L3}^2\right)r_C\right]+2DV_Fi_{L1}$ |  $P_{52}=2\left(1-D\right)^2\left(i_{L1}^2+i_{L3}^2\right)r_L+\left(1-D\right)V_F\left(2i_{L1}+2i_{L3}-i_{PN}\right)+2\left(1-D\right)^2r_C\left[\left(i_{L1}-i_{L3}\right)^2+\left(i_{L3}-i_{PN}\right)^2\right]$ | $\eta_{EB-qZSI}=\frac{V_{PN}I_{PN}}{P_{51}+P_{52}+V_{PN}I_{PN}}$<br>$\eta_{EB-qZSI}=\frac{1}{A_5+B_5+C_5+1}$<br>$A_5=\frac{2r_L}{R_l}\frac{\left(1-D\right)^3\left[1+\left(1-D\right)^2\right]}{\left(1-4D+2D^2\right)^2}\left[\left(1-D\right)^2+D^2\right]$<br>$B_5=\frac{4r_C}{R_l}\frac{D^2\left(1-D\right)^3\left[5-6D+2D^2\right]}{\left(1-4D+2D^2\right)^2}$<br>$C_5=3V_F\left(1-D\right)/V_{dc}$ |
| Proposed qZSI |  $P_{41}=D^2r_L\left(2i_{L1}^2+2i_{L2}^2\right)+D^2r_C\left(2i_{L1}^2+2i_{L3}^2\right)+2DV_Fi_{L2}$ |  $P_{42}=\left(1-D\right)^2r_L\left(2i_{L1}^2+2i_{L2}^2\right)+\left(3-2D\right)V_Fi_{L2}+\left(1-D\right)^2r_C\left[2\left(i_{L1}-i_{L2}\right)^2+2\left(2i_{L1}-i_{L2}-i_{PN}\right)^2\right]$ | $\eta_{Proposed-qZSI}=\frac{V_{PN}I_{PN}}{P_{41}+P_{42}+V_{PN}I_{PN}}$<br>$\eta_{proposed-qZSI}=\frac{1}{A_4+B_4+C_4+1}$<br>$A_4=\frac{2r_L}{R_l}\frac{\left(1-D\right)^3\left[1+\left(1-D\right)^2\right]}{\left(1-4D+2D^2\right)^2}\left[\left(1-D\right)^2+D^2\right]$<br>$B_4=\frac{4r_C}{R_l}\frac{D^2\left(1-D\right)^3\left[1+\left(1-D\right)^2\right]}{\left(1-4D+2D^2\right)^2}$<br>$C_4=\frac{3V_F\left(1-D\right)}{V_{dc}}$ |

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2018.2873805, IEEE Journal of Emerging and Selected Topics in Power Electronics



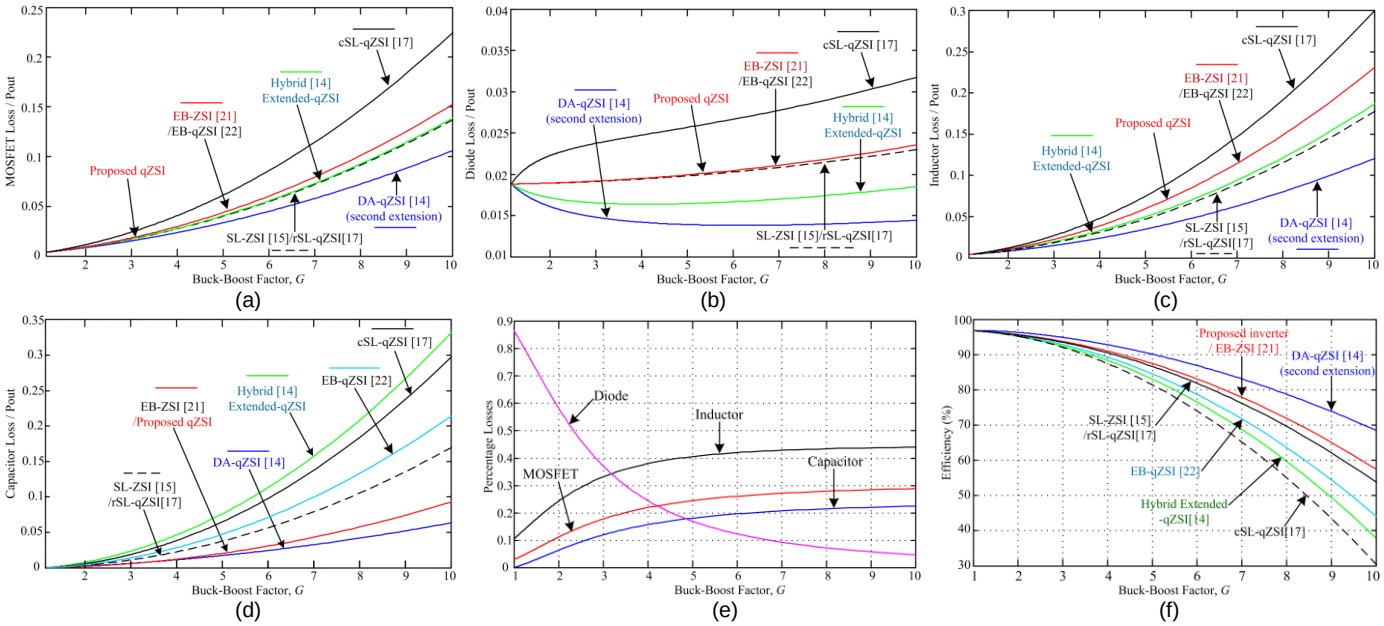



Fig. 14 Power loss analysis and efficiency comparison: (a) MOSFET loss comparison, (b) Diode loss comparison, (c) Inductor loss comparison, (d) Capacitor loss comparison, (e) Percentage power loss distribution of the proposed topology, (f) Efficiency comparison for these high boost (q)ZSIs.

## VII. Simulation and Experimental Results

### A. Simulation Results

To validate the effectiveness of the proposed high boost qZSI, the simulations are firstly verified by the Matlab/Simulink® software platform. And the simulation parameters are selected as:1) DC input voltage $V_{dc}$=60V, 2) inductors $L_1$=$L_2$=$L_3$=$L_4$=1mH, 3) capacitors $C_1$=$C_2$=$C_3$=$C_4$=470uF, 4) fundamental frequency $f$=50Hz, 5) switching frequency $f_s$=10kHz, 6) output filter inductor $L_f$=2mH, 7) output filter capacitor $C_f$=50uF, 8) three phase inductive load $R_L$=50Ω, $L_l$=5mH. All the components are ideal in the simulation part.

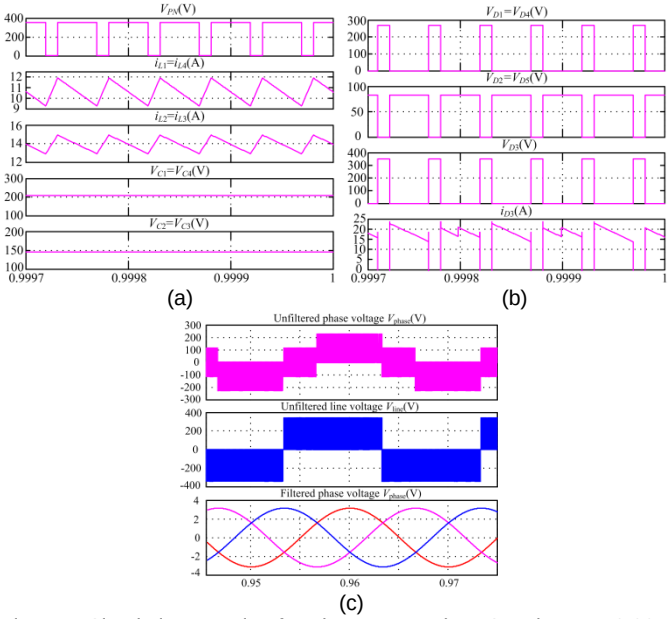



Fig. 15 Simulation results for the proposed qZSI when $D$=0.235, $M$=0.8834, $G$=5.18.

In order to produce the output phase voltage of 110Vrms from the 60V dc input voltage with constant boost control method, a shoot-through duty ratio $D$=0.235 is needed at modulation index $M$=0.8834 for the proposed inverter. Thus, from (14)-(15), we obtain the boost factor $B$=5.86, and the buck-boost factor $G$=$MB$=5.18. Fig. 15 shows the simulation results for the proposed inverter when $D$=0.235, $M$=0.8834. From Fig. 15(a), it can be observed that the capacitor voltages $V_{C1}$(=$V_{C4}$) and $V_{C2}$(=$V_{C3}$) are boosted to 208V and 145V in the steady state, and the peak dc-link voltage $V_{PN}$ is boosted to 351V. Hence, the boost factor $B$ can be calculated to be 351/60=5.85. Meanwhile, the peak ac output voltage is boosted to 155V, and the corresponding buck-boost factor $G$ can be calculated as 155/30=5.17, which are in consistent with the calculated values from (13) and (15). Therefore, it can be concluded that in steady state, there is a good agreement between simulation results and the theoretical analysis.

The diode ($D_1$/$D_4$, $D_2$/$D_5$, $D_3$) voltage stresses are shown in Fig. 15(b). From this figure, it can be observed that the diode voltages $V_{D1}$(=$V_{D4}$), $V_{D2}$(=$V_{D5}$) and $V_{D3}$ are 268.5V, 82.6V and 351V respectively in steady state condition, which are matching well with the values obtained in theoretical analysis. Besides, the simulation waveforms of phase voltage ($V_{phase}$), line voltage ($V_{line}$), and phase current ($i_{phase}$) are shown in Fig. 15(c). Therefore, these results clearly verify the high boosting capability of the proposed topology.

### B. Experimental Results

In this section, the experimental prototype of the proposed inverter in Fig. 16 was built in laboratory to verify the operating principle. Table IX lists the parameters used for the experiments, which are the same as the simulation parameters. And three inductive loads ($R_L$=50Ω, $L_l$=5mH) are connected to the three-phase ac outputs in a Y-connection. Based on the constant boost control method in [8], the gating signals of the three-phase inverter bridge are generated by a 32 bit TMS320F28335 DSP operating with a clock frequency of 150MHz. All the power switches are driven by the 2BB0108T basic board with driver 2SC0108T, and all the diodes are

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2018.2873805, IEEE Journal of Emerging and Selected Topics in Power Electronics



selected the RURG3060CC(600V, 30A). In addition, the control block diagram and the switching logic for control signal generation of the proposed inverter are shown in Fig. 17.

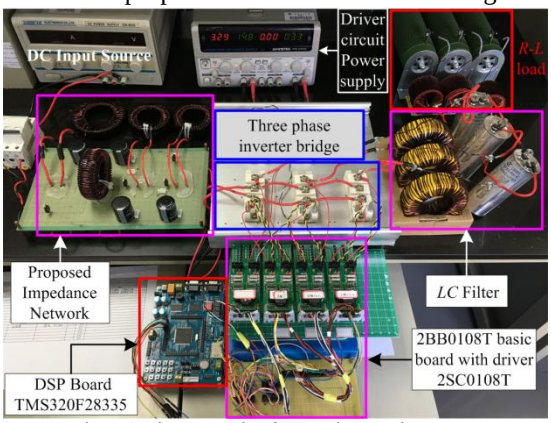
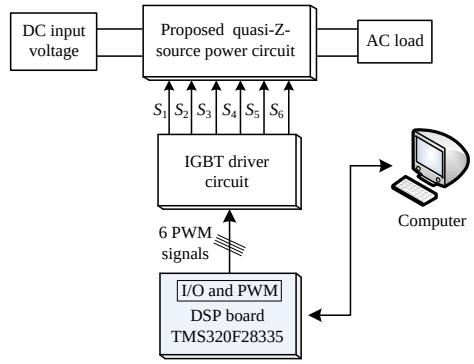



Fig. 16 Photograph of experimental set-up.

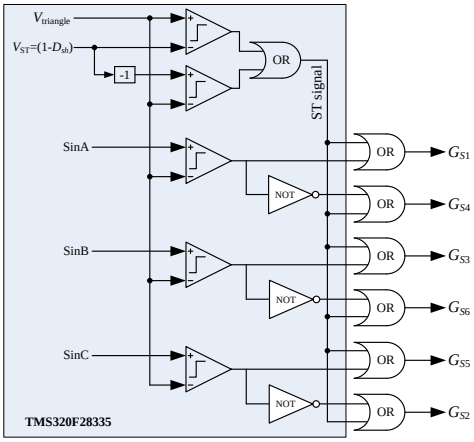
**Table IX**

Parameters used for experiments

| S.no | Parameters/Descriptions | Values |
|---|---|---|
| 01 | DC input voltage | 60V |
| 02 | Modulation index, $M$ | 0.8834 |
| 03 | Shoot-through duty ratio, $D$ | 0.235 |
| 04 | Inductors ($L_1$=$L_2$=$L_3$=$L_4$) | 1mH |
| 05 | Capacitors ($C_1$=$C_2$=$C_3$=$C_4$) | 470uF |
| 06 | Fundamental frequency, $f$ | 50Hz |
| 07 | Switching frequency, $f_s$ | 10kHz |
| 08 | Output filter inductor, $L_f$ | 2000uH |
| 09 | Output filter capacitor, $C_f$ | 50uF |
| 10 | Switches (BSM100GB60DLC) | 600V, 100A |
| 11 | Diodes (RURG3060CC) | 600V, 30A |
| 12 | Three phase inductive loads | $R_L$=50Ω, $L_f$=5mH |




(a)




(b)

Fig. 17 (a) Block diagram of the Experimental system, (b) Switching logic for control signal generation.

Fig. 18 shows the experimental results for the proposed inverter when $V_{dc}$=60V, shoot-through duty ratio $D$=0.235, and modulation index $M$=0.8834. As shown in Fig. 18(a) and (c), the peak dc-link voltage $V_{PN}$ is boosted from 60V to 329V, which is slightly less than the theoretical value (60*5.86=351.6V) calculated from (12) due to the voltage reduction on inductors, capacitors and diodes. The capacitor voltage $V_{C1}$(=$V_{C4}$), $V_{C2}$(=$V_{C3}$) are boosted to 200V and 138V, respectively. While the calculated values from (9) and (10) are 208V and 145.8V, which are a little higher than the experimental values. The inductor currents $i_{L1}$(=$i_{L4}$) and $i_{L2}$(=$i_{L3}$) are measured and presented in Fig. 18(b). From this figure, it can be seen that the inductors are charged in the shoot-through state, while in the non-shoot-through state, the energy stored in these inductors are discharged and transferred to the main circuit. Besides, the voltage stresses across all the diodes are measured and shown in Fig. 18(d), which shows a good agreement with the simulation results in Fig. 15(b). Meanwhile, as shown in Fig. 18(e), the rms value of the ac output phase voltage is measured about 107V, which is slightly lower than the desired value, due to the parasitic effect of passive/active components. In addition, the experimental waveforms of the unfiltered/filtered ac output phase voltage, line voltage and the phase current are also measured in Figs. 18(e) and (f), which are fit well with the simulation results in Fig. 15(c), except for some spikes and switching noise superimposed, which are generated at nearly all semiconductor switching instants.

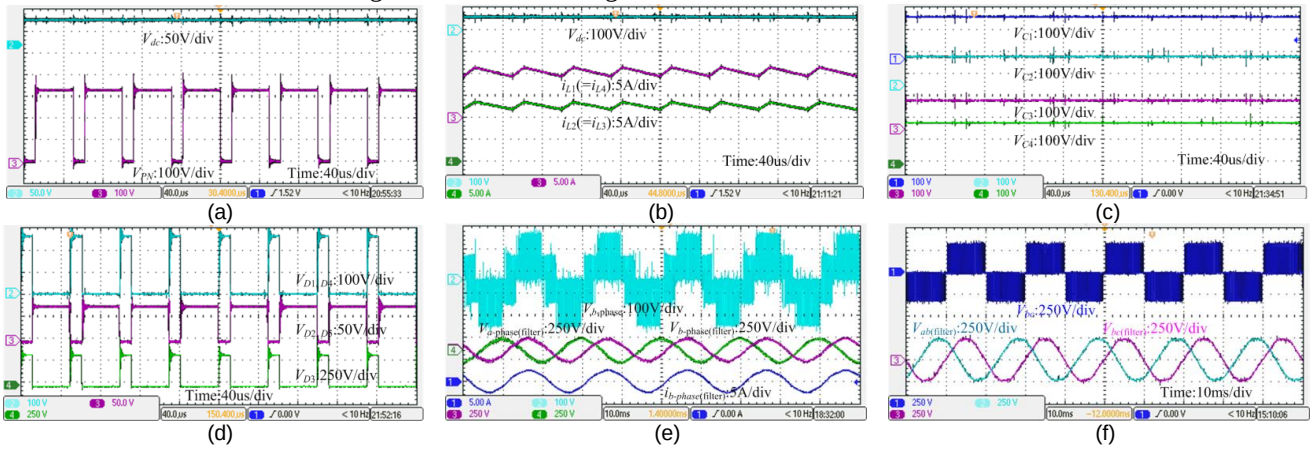



Fig. 18 Experimental results for the proposed inverter when $V_{dc}$=60V, $D$=0.235, $M$=0.8834, $B$=5.86.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2018.2873805, IEEE Journal of Emerging and Selected Topics in Power Electronics



Table X shows the comparison between the simulation and experimental results for the peak dc-link voltage and capacitor voltages. From this table, it can be observed that the simulated peak dc link voltage and capacitor voltages are, respectively, 6.27%, 3.85% and 4.82% higher than the corresponding experimental values. This is due to the fact that the voltage drops on inductors, capacitors and diodes were ignored in simulation, whereas these cannot be ignored in practical applications.

**Table X**

Peak DC link and capacitor voltages in simulation and experiment

| | Simulation | Experimental | Δ Experimental |
|---|---|---|---|
| Peak DC link voltage | 351V | 329V | 6.27% |
| Capacitor voltage, $V_{C1}=V_{C4}$ | 208V | 200V | 3.85% |
| Capacitor voltage, $V_{C2}=V_{C3}$ | 145V | 138V | 4.82% |

Additionally, the experimental harmonic spectrum of the unfiltered ac output line voltage ($V_{bc}$), filtered ac output phase current are measured and shown in Fig. 19. From Fig. 19(a), it can be observed that the harmonic spectrum of the unfiltered ac output line voltage $V_{bc}$ is mainly distributed near the switching frequency (10kHz) and its integer multiple frequencies, which shows a good accordance with the theoretical analysis. Fig. 19(b) shows the measured harmonic spectrum of the filtered ac output phase current. From this figure, one can find that the main spectrum components are the fundamental frequency (50Hz) components, and the measured total harmonic distortion (THD) of the load current is about 2.43%.

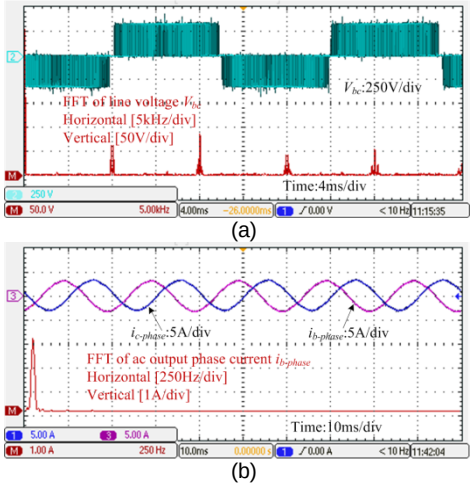



Fig. 19 Experimental results of the harmonic spectrums for the proposed qZSI when $D$=0.235, $M$=0.8834. (a) Harmonic spectrum of the unfiltered line voltage ($V_{bc}$), (b) Harmonic spectrum of the load phase current.

In order to better evaluate the dynamic response performance of the proposed converter. The transient-state experimental results with load change (from no load to full load and vice versa) have been measured and shown in Fig. 20. Fig. 20(a) shows the experimental results of filtered line voltage ($V_{ab}$, $V_{bc}$) and phase current ($i_b$, $i_c$) from no load to full load, and Fig. 20(b) is the zoom-in of Fig. 20(a). Fig. 20(c) shows the experimental results from full load to no load, and Fig. 20(d) is the zoom-in of Fig. 20(c).

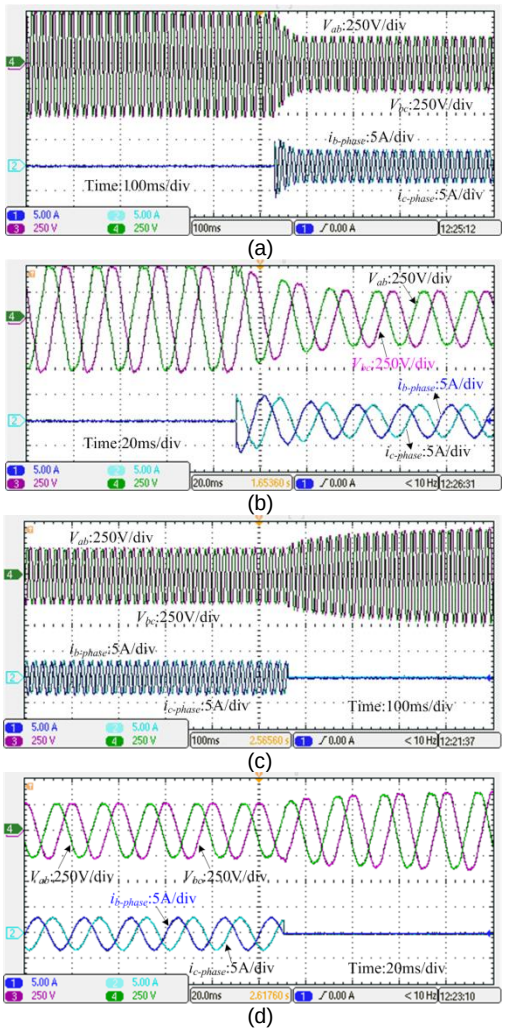
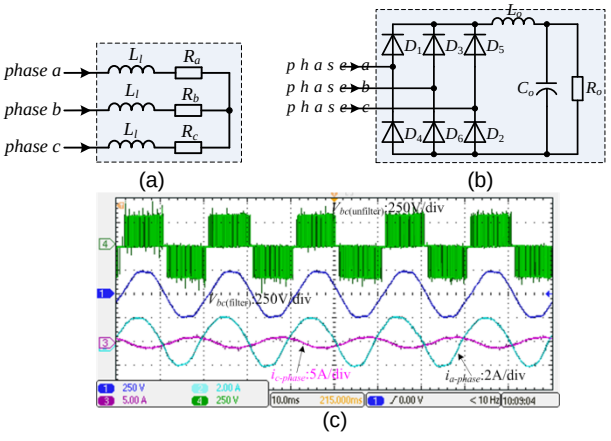


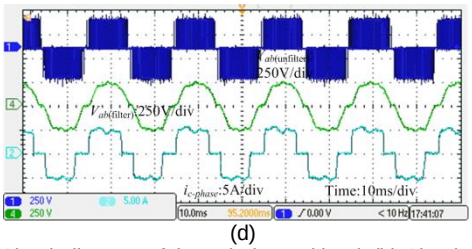

Fig. 20 Experimental results of the transient-state with load change. (a) From no load to full load, (b) Zoom in of Fig. 20(a), (c) From full load to no load, (d) Zoom in of Fig. 20(c).

Fig. 21 shows the experimental results when the load type is considered to be unbalanced and nonlinear. For the unbalanced load type, as shown in Fig.21(a), we set the load resistances of phase A, B and C are $R_a$=50Ω, $R_b$=100Ω, $R_c$=150Ω, respectively. For the nonlinear load type, a three-phase diode bridge rectifier feeding to the *R-L-C* load is constructed, which is shown in Fig. 21(b), and the $L_o$=15mH, $C_o$=470uF, $R_o$=50Ω. Fig. 21(c) shows the experimental results of the proposed inverter when it is operated at the unbalanced load type. Due to



This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2018.2873805, IEEE Journal of Emerging and Selected Topics in Power Electronics






(d)

Fig. 21 (a) Circuit diagram of the unbalanced load, (b) Circuit diagram of the nonlinear load, (c) Experimental results of the proposed qZSI under the unbalanced load condition, (d) Experimental results under the nonlinear load condition.

the load resistance of phase A, B and C is different, the measured load phase currents have different amplitude values, as shown in Fig. 21(c), the peak value of load current $i_a$ is about 2A, while for the phase current $i_c$, the peak value is about 1.2A. The experimental results of the proposed qZSI under nonlinear load type is measured and shown in Fig. 21(d). From this figure, it can be observed that the measured filtered line voltage and phase current both have severe distortion, and the measured THD value of the load current is about 36%.

Fig. 22 shows the comparison between the calculated and the experimental boost factors. From this figure, it can be seen that by increasing the value of the duty cycle the difference between calculated and experimental results are increased. This is due to the high conduction power losses on devices during a large shoot-through interval, which exists in all kinds of (q)ZSIs.

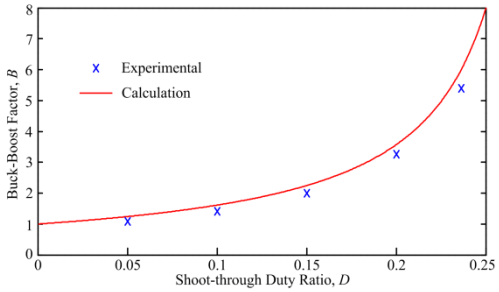



Fig. 22 Calculated and experimental values of boost factor.

The efficiency of the proposed inverter with different output power has been measured and depicted in Fig. 23 by changing the load from 250W to 756W keeping the input voltage is 60V to obtain 110Vrms ac output phase voltage. From this figure, it can be seen that the maximum measured experimental efficiency was about 91%, which was not high. This can be explained by the fact that the proposed qZSI has a shoot-through state and the passive/active components selection were not optimal in the experimental setup. When the shoot-through duty cycle is large for high voltage gain, the power losses in passive and active components would be significant.

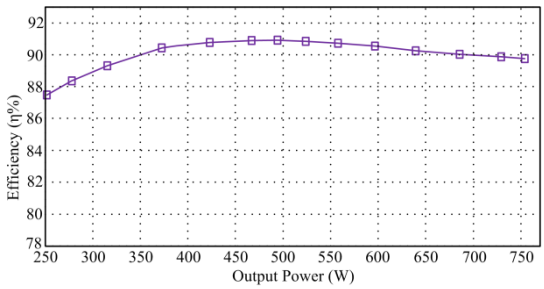



Fig. 23 Measured efficiency versus different output power.

## VIII. Conclusion

A new high boost quasi-Z-source inverter with combined two quasi-Z-source network was proposed in this paper. The operating principle analysis, power loss analysis, and performance comparison with other high boost (q)ZSIs have been described in detail. Finally, both the simulation and experimental results are presented to validate the effectiveness of the proposed topology. Compared with the conventional high boost (q)ZSIs, the proposed inverter not only has a common ground between the input source and the inverter bridge, but also can provide higher boost factor over the whole shoot-through duty ratio range, smaller inductance and capacitance at the impedance network, and lower active switching voltage stress across the main inverter for the same dc input and ac output voltages. Although the proposed topology has the same voltage boost factor with the EB-ZSI and EB-qZSI, it has lower capacitor voltage stresses than EB-ZSI and has higher efficiency than EB-qZSI. Therefore, it would be applicable for the renewable energy system (like PV or fuel-cell stacks) where the high boost inversion ability is required for the low-voltage DG (distributed generation) sources.

## References

[1] N. Mohan, T. M. Undeland, W. P. Robbins, *Power Electronics: Converters, Application and Design*. New York: Wiley, 2003.

[2] A. Ioinovici, *Power Electronics and Energy Conversion Systems*. Hoboken, NJ, USA: Wiley, 2013.

[3] M. Shen, A. Joseph, J. Wang, F. Z. Peng, D. J. Adams. 'Comparison of traditional inverters and Z-source inverter for fuel cell vehicles', *IEEE Trans. Power Electron.*, 2007, vol. 22, no. 4, pp. 1453–1463, DOI: 10.1016/j.renene.2017.08.032

[4] F. Z. Peng, 'Z-source inverter',: *IEEE Trans. Ind. Appl*., 2003, vol. 39, no. 2, pp. 504–510, DOI: 10.1109/TIA.2003.808920

[5] P. C. Loh, D. M. Vilathgamuwa, C. J. Gajanayake, Y. R. Lim, C. W. Teo, 'Transient Modeling and Analysis of Pulse-Width Modulated Z-Source Inverter', *IEEE Trans. Power Electron*., 2007, vol. 22, no. 2, pp.498-507, DOI: 10.1109/TPEL.2006.889929

[6] J. Liu, J. Hu, L. Xu, 'Dynamic modeling and analysis of z source converter—Derivation of AC small signal model and design-oriented analysis', *IEEE Trans. Power Electron.*, 2007, vol. 22, no. 5, pp. 1786–1796, DOI: 10.1109/TPEL.2007.904219

[7] P. C. Loh, D. M. Vilathgamuwa, Y. S. Lai, G. T. Chua, and Y. Li, 'Pulse width modulation of Z-source inverters', *IEEE Trans. Power Electron.*, 2005, vol. 20, no. 6, pp. 1346–1355, DOI: 10.1109/TPEL.2005.857543

[8] M. Shen, J. Wang, A. Joseph, F.Z. Peng, L.M. Tolbert, D.J. Adams, 'Constant boost control of the Z-source inverter to minimize current ripple and voltage stress', *IEEE Trans. Ind. Appl.*, 2006, vol. 42, no. 3, pp. 770–778, DOI: 10.1109/TIA.2006.872927

[9] Y. Tang, S. J. Xie, J. D. Ding, 'Pulse width Modulation of Z-Source Inverters With Minimum Inductor Current Ripple', *IEEE Trans. Power Electron*., 2014, vol. 61, no. 1, pp.98-106, DOI: 10.1109/TIE.2013. 2240632

[10] M. S. Diab, A. A. Elserougi, A. M. Massoud, A. S. Abdel-Khalik, and S. Ahmed, "A pulse width modulation technique for high-voltage gain operation of three-phase Z-source inverters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 2, pp. 521–533, Mar. 2016.

[11] Y. Tang, S. J. Xie, C. H. Zhang, Z. Xu, 'Improved Z-source inverter with reduced Z-source capacitor voltage stress and soft-start capability', *IEEE Trans. Power Electron.*, 2009, vol. 24, no. 2, pp. 409–415, DOI: 10.1109/TPEL.2008.2006173

[12] Y. Tang, S. J. Xie, C. H. Zhang, 'An improved Z-source inverter', *IEEE Trans. Power Electron.*, 2011, vol. 26, no. 12, pp. 3865–3868, DOI: 10.1109/TPEL.2009.2039953

[13] J. Anderson, F. Z. Peng,: 'Four quasi-Z-source inverters', in *Proc. IEEE Power Electron. Spec. Conf*. (PESC'08), Jun. 2008, pp. 2743–2749, DOI: 10.1109/PESC.2008.4592360

[14] C. J. Gajanayake, F. L. Luo, H. B. Gooi, P. L. So, L. K. Siow,

'Extended-boost Z-source inverters', *IEEE Trans. Power Electron.*, 2010, vol. 25, no. 10, pp. 2642–2652, DOI: 10.1109/TPEL.2010.2050908

[15] M. Zhu, K. Yu, F. L. Luo, 'Switched-inductor Z-source inverter', *IEEE Trans. Power Electron.*, 2010, vol. 25, no. 8, pp. 2150-2158, DOI: 10.1109/TPEL.2010.2046676

[16] M.K. Nguyen, Y.C. Lim, G.B. Cho, 'Switched-inductor quasi-Z-source inverter', *IEEE Trans. Power Electron.*, 2011, vol. 26, no. 11, pp. 3183-3191, DOI: 10.1109/TPEL.2011.2141153

[17] M.K. Nguyen, Y.C. Lim, J.H. Choi, 'Two switched-inductor quasi z-source inverters', *IET Power Electron.*, 2012, vol. 5, no. 7, pp. 1017–1025, DOI: 10.1049/iet-pel.2011.0297

[18] D. Li, P. C. Loh, M. Zhu, F. Gao, and F. Blaabjerg, 'Generalized multicell switched-inductor and switched-capacitor Z-source inverters', *IEEE Trans. Power Electron.*, 2013, vol. 28, no. 2, pp. 837–848, DOI: 10.1109/TPEL.2012.2204776

[19] A.V. Ho, T.W. Chun, and H. G. Kim, 'Extended Boost Active-Switched-Capacitor/Switched-Inductor Quasi-Z-Source Inverters', *IEEE Trans. Power Electron.*, 2015, vol. 30, no. 10, pp. 5681–5690, DOI: 10.1109/TPEL.2014.2379651

[20] A. Ahmad, V. K. Bussa, R. K. Singh, R. Mahanty, "Switched-Boost Modified Z-Source Inverter Topologies with Improved Voltage Gain Capability", *IEEE J. Emerg. Sel. Topics Power Electron.*, pp. 1-1, Apr. 2018 (early access). DOI: 10.1109/JESTPE.2018.2823379

[21] H. Fathi, H. Madadi,: 'Enhanced-Boost Z-Source Inverters with Switched Z-Impedance', *IEEE Trans. Ind. Electron.*, 2016, vol. 63, no. 2, pp. 691–703, DOI: 10.1109/TIE.2015.2477346

[22] V. Jagan, J, Kotturu, and S. Das, 'Enhanced-Boost Quasi-Z-Source Inverters with Two Switched Impedance Network', *IEEE Trans. Ind. Electron.*, 2017, vol. 64, no. 9, pp. 6885–6897, DOI: 10.1109/TIE.2017.2688964

[23] M. K. Nguyen, T. D. Duong, Y. C. Lim and J. H. Choi, "High Voltage Gain Quasi-Switched Boost Inverters with Low Input Current Ripple," *IEEE Trans. Ind. Informat.*, DOI: 10.1109/TII.2018.2806933, 2018 (early access)

[24] G. Zhang, B. Zhang, Z. Li, Y. Zhang, S. Z. Chen, "A Novel Single Input-Dual-Output Impedance Network Converter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 3, pp. 1133–1141, Sep. 2017.

[25] M. Zhu, D. Li, F. Gao, P. C. Loh, and F. Blaabjerg, 'Extended topologies of tapped-inductor Z-source inverters', in *Proc. 8th IEEE ICPE & ECCE*, 2011, pp. 1599–1605, DOI: 10.1109/ICPE.2011.5944382

[26] H. Liu, Y. Ji and P. Wheeler, "Coupled-Inductor L-Source Inverter," *IEEE J. Emerg Sel. Topics Power Electron.*, vol. 5, no. 3, pp. 1298- 1310, Sept. 2017

[27] W. Qian, F. Z. Peng, and H. Cha, 'Trans-Z-source inverters', *IEEE Trans. Power Electron.*, 2011, vol. 26, no. 12, pp. 3453–3463, DOI: 10.1109/TPEL.2011.2122309

[28] M. K. Nguyen, Y. C. Lim, and Y. G. Kim, 'TZ-source inverters', *IEEE Trans. Ind. Electron.*, 2013, vol. 60, no. 12, pp. 5685-5695, DOI: 10.1109/TIE.2012.2229678

[29] Y. P. Siwakoti, F. Blaabjerg, and P. C. Loh, 'New magnetically coupled impedance (Z-) Source networks', *IEEE Trans. Power Electron.*, 2016, vol. 31, no. 11, pp. 7419-7434, DOI: 10.1109/TPEL.2015.2459233

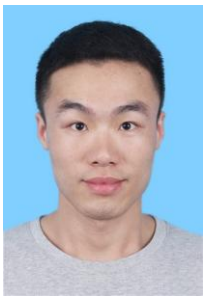
[30] D. Li, F. Gao, P. C. Loh, M. Zhu, and F. Blaabjerg, 'Hybrid-source impedance networks: Layouts and generalized cascading concepts', *IEEE Trans. Power Electron.*, 2011, vol. 26, no. 7, pp. 2028–2040, DOI: 10.1109/TPEL.2010.2101617

[31] D. Li, P. C. Loh, M. Zhu, F. Gao, and F. Blaabjerg, 'Cascaded multicell trans-z-source inverters', *IEEE Trans. Power Electron.*, 2013, vol. 28, no. 2, pp. 826–836, DOI: 10.1109/TPEL.2012.2205709

[32] D. Li, P. C. Loh, M. Zhu, F. Gao, and F. Blaabjerg, 'Enhanced-boost Z-source inverters with alternate-cascaded switched-and tapped-inductor cells', *IEEE Trans. Ind. Electron.*, 2013, vol. 60, no. 9, pp. 3567–3578, DOI: 10.1109/TIE.2012.2205352

[33] M. K. Nguyen, Y. C. Lim, S. J. Park, and D. S. Shin, 'Family of high boost Z-source inverters with combined switched-inductor and transformer cells', *IET Power Electron.*, 2013, vol. 6, no. 6, pp. 1175-1187, DOI: 10.1049/iet-pel.2013.0033

[34] Erie Wittenbreder, "Topology Selection by the Numbers," *Technical Witts Inc.*, pp. 32-43,March 2006.



**Xiaoquan Zhu** was born in Anhui, China, in 1990. He received the B.S. degree in School of Information and Control engineering from China University of Mining and Technology, Xuzhou, China, in 2014. He is currently working toward the Ph.D. degree in electrical engineering at the School of Electric Power, South China University of Technology, Guangzhou, China. His current research interests include high step-up power electronic converters and renewable energy power generation systems.

**Bo Zhang** (M'03–SM'15) was born in Shanghai, China, in 1962. He received the B.S. degree in electrical engineering from Zhejiang University, Hangzhou, China, in 1982, the M.S. degree in power electronics from Southwest Jiaotong University, Chengdu, China, in 1988, and the Ph.D. degree in power electronics from Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 1994. He is currently a Professor with the School of Electric Power, South China University of Technology, Guangzhou, China. He has authored or coauthored four books in IEEE-Wiley and Springer, more than 450 technical papers and holds 100 patents. His current research interests include nonlinear analysis, modeling and control of power electronic converters, and wireless power transfer applications.

**Dongyuan Qiu** (M'03) was born in China in 1972. She received the B.S. and M.S. degrees from the South China University of Technology, Guangzhou, China, in 1994 and 1997, respectively, and the Ph.D. degree from the City University of Hong Kong, Kowloon, Hong Kong, in 2002. She is currently a Professor with the School of Electric Power, South China University of Technology, Guangzhou, and an Associate Editor of the IEEE Transactions on Power Electronics. She has authored or coauthored one book, over 100 papers and holds 80 patents. Her main research interests include wireless power transfer, fault diagnosis, and sneak circuit analysis of power electronic systems.