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FPGA-Based Real-time Simulation of High-Power Electronic System with Nonlinear IGBT Characteristics

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***Abstract*—The hardware-in-the-loop (HiL) simulation plays a vital role in the test of high-power electronic system. Although the application of field programmable gate array (FPGA) embedded system has enabled the real-time system simulating below 500ns, the transient characteristic of high voltage insulated-gate bipolar transistor (HVIGBT) is largely compromised. In this paper, a new piece-wise HVIGBT model, considering its driver circuit effect and parasite parameter, is proposed for FPGA-based real-time simulation applications. With the attempt to reduce the simulation latency, we propose a FPGA solver with a parallel structural to divide the system into several layers. The model could not only provide accurate system-level performance of the power electronic converter but also give an insight into the transient behavior effect of high-power electronic system. At last, a case study about emulation of traction system of high-speed train is also presented. Implementations are made on a FPGA Kintex-7 embedded in National Instruments FlexRIO PXIe-7975. The obtained results show that the proposed modeling algorithm can achieve both accuracy and efficiency within a fixed real-time simulation time step of 25 nanoseconds.**

***Index Terms*— Hardware-in-the-loop; High Power Electronic System; FPGA; High voltage IGBT Model; Traction System**

V_{ces}	**Collector-emitter saturation voltage**
V_{GEth}	**Gate threshold voltage**
R_G	**Internal gate resistor**
C_{ies}	**Input capacitance**
C_{res}	**Reverse transfer capacitance**
g_m	**Forward trans-conductance**
$t_{d\ on}$	**Turn-on delay time, inductive load**
t_r	**Rise time, inductive load**
$t_{d\ off}$	**Turn-off delay time, inductive load**
t_f	**Fall time, inductive load**
I_{CE}	**Collector-emitter current**
V_{ce}	**Collector-emitter saturation voltage**
L_S	**Stray inductance module**
V_D	**Diode Forward voltage**

I. INTRODUCTION

THE high voltage insulated-gate bipolar transistor (HVIGBT) is widely used in the electrified transportation where high voltage and current are required. Advancements in power electronics applications demand IGBT operating in high switching speed as well as high switching frequency [1]. Due to dead-time, switching time, delay time and voltage drops, the output voltage and current are distorted with respect to an ideal switch performance [2]. Its model precision is crucial for model-based motor control strategy [3]. Researching HVIGBT model is an important stream for theses megawatt power electronic system simulation.

In recent years, there are three types of IGBT model used in real-time simulation. The most accurate model is numerical model, which solves the physical equations in analytical expression describing carriers and electrical behavior. The analytical model utilizes the parameter extracted from testing waveform and solves high-order physical equations. Despite these physical or device level models are assumed to be too complex to be implemented in FPGA, [4][5][6] have reported using physical or device level semiconductor simulation in FPGA. They are impressive for an FPGA implementation seeking low steps within acceptable on-chip resource utilization. However, these implementations are not suitable for a HVIGBT with high switch frequency and high switch speed. The relative slow calculation speed in their execution results a high latency between simulator and controller, which could largely affect the simulator's response to the controller. As for the behavioral model [7][8][9], it treats semiconductor devices as ideal or nearly ideal switches when the semiconductors are in either completely on or completely off states. This idealization is suitable for the fast computation speed required by the real-time. But it is incapable of showing detailed

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switching characteristics. Another related works has reported the piecewise switch method based on volt-ampere characteristics. In [10], the IGBT is composed by a fixed turn-on delay time, fixed turn-on rise time, fixed turn-off delay time and fixed turn-off fall time. But the model will not change with electromagnetic environment and it is only accurate under a specific current and voltage level. The implementation in [11] has reported in a simulation step of $12.5ns$ with a look up table method in FPGA, which requires amounts of experiment data from double pulses test.

In sum, the main hurdles in the IGBT transient simulation in HIL application are how to consider the effect of different voltage level and how to minimize the latency between simulator and controller. Aiming to address the above questions, one of the main objectives in this paper is to build the nonlinear characteristic of IGBT model for FPGA-based real-time applications. Compared with the drawback of the existing approach for modeling IGBT, the proposed model has the following benefits: 1) the computation time of IGBT model is largely reduced; 2) it provides the switch with a natural behavior that does not require a priori knowledge of the circuit topology nor operation; 3) it can be applied to high voltage level and high switching speed.

Besides, in order to apply this model to a high-power application, the traction system in the high-speed train is used as a case study. Analysis and design of such railway traction system is often a challenging task when facing such a complex system. First, it is a complex hybrid system containing dozens of semiconductors. Second, it involves stiff problem. Apart from the semiconductor switch devices, there are also asynchronous motors. The mutual effect of different components in the traction system should be evaluated. A HIL platform, which solves the above problem, could offer the ability to connect to real physical equipment in hardware to validate motor drive system controllers as well as its associated algorithm [12].

The reminder of this paper is structured as follows: the illustration of voltage distortion caused by different IGBT model is shown in Section II. Section III illustrates the IGBT model considering parasite parameter and driver circuit. Section IV proposes a parallel discrete solver in FPGA including the implementation of IGBT model. The traction system of high-speed train, which is used as case study, is shown in Section V. Section VI gives the conclusions of this work.

II. Voltage Distortion with different IGBT model

In Fig 1, a traditional two-level IGBT leg is shown. Vdc is a DC-link voltage and I_0 is the phase current. The following analysis and comparison of voltage transient assume that the driver circuit of IGBT S1 and S2 is the same.

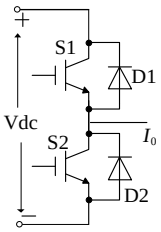

Fig 1. Two-Level Inverter Topology

When phase current $I_0 > 0$, the different combination of the switching states is shown in Fig 2. Fig 2(a) is the most commonly states. Fig 2(b) is a case when the switch unit $S2$ gets a turn-on signal while $S1$ is off. In this situation, the current will flow through the parallel diode of $S2$ rather than the IGBT device. Fig 2(c) considers the effect of dead-time. During this period, both $S1$ and $S2$ are off. The output voltage is determined by the direction of output current. Special Case is the shoot-through status used in Z Source Inverter [13], as shown in Fig 2(d). The current path is decided by idc rather than phase current. The similar results can be obtained in Fig 3 when phase current $I_0 < 0$.

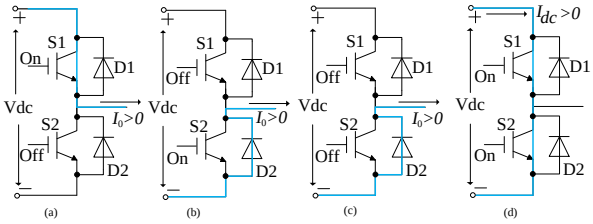

Fig 2. Current Paths for different switching conditions (Phase Current $I_0 > 0$)

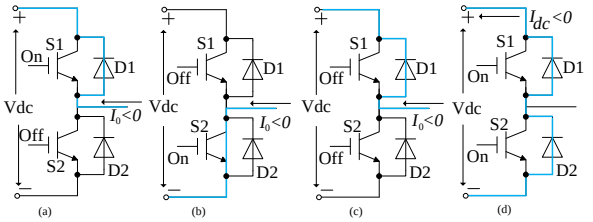

Fig 3. Current Paths for different switching conditions (Phase Current $I_0 < 0$)

The transient performance of IGBT with different working statuses is shown in Fig 4. The signal drive circuit has a dead-time period, as shown in Fig 4(a). The Black line in Fig 4(b) and Fig 4(d) represents the ideal voltage output and the Blue line is an actual output phase voltage Vn. The actual transient output voltage usually consists of four different time stages, the turn on delay time ($t_0 \sim t_1$), the turn-on time ($t_1 \sim t_2$), the turn off delay time ($t_4 \sim t_5$) and the turn-on time ($t_5 \sim t_6$). Dashed line in Fig 4(c) is a different DC voltage V_{dc}^* condition. The fixed time stage model is represented with red dashed line and the actual output voltage is presented with Blue dashed line. Despite the turn-on delay time and turn-off delay time can be assumed to be the same, different voltage level usually has a different turn-on time ($t_1 \sim t_3$) and the turn-on time ($t_5 \sim t_7$).

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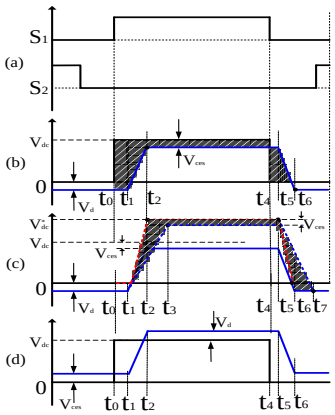


(a) Driving pulses with Dead-time; (b)(c) Output Voltage when Phase Current $I_0 > 0$; (d) Output Voltage when Phase Current $I_0 < 0$.
Fig 4. Driving Pulses and inverter output voltage.

When Phase Current $I_0 > 0$, the voltage error area [3] with the ideal switch model can be calculated as (1).

$$\begin{cases} E_{(t_0\sim t_1)} = (t_1 - t_0)(V_d + V_{dc}) \\ E_{(t_1\sim t_2)} = \frac{1}{2}(t_2 - t_1)(V_d + V_{dc} + V_{ces}) \\ E_{(t_2\sim t_4)} = (t_4 - t_2)V_{ces} \\ E_{(t_4\sim t_5)} = (t_5 - t_4)(V_{dc} - V_{ce}) \\ E_{(t_5\sim t_6)} = \frac{1}{2}(t_6 - t_5)(V_{dc} - V_{ce}) \end{cases} \quad (1)$$

Compared with fixed time stage behavior model, the voltage distraction area can be expressed as,

$$\begin{cases} E_{(t_0\sim t_1)} = (t_1 - t_0)V_d \\ E_{(t_1\sim t_3)} = \frac{1}{2}(t_3 - t_2)(V^*_{dc} - V_{ces}) \\ E_{(t_3\sim t_4)} = (t_4 - t_3)V_{ces} \\ E_{(t_4\sim t_5)} = (t_5 - t_4)V_{ces} \\ E_{(t_5\sim t_7)} = \frac{1}{2}(t_7 - t_6)(V^*_{dc} - V_{ces} + V_d) \end{cases} \quad (2)$$

From the above comparison in (1) and (2), it can be noted that at the high voltage condition ($V_{dc} \gg V_d$ and $V_{dc} \gg V_{ces}$), the main error comes from the voltage turn-on rate and turn-off rate of different voltage level.

III. IGBT Transient Model

Although highly detailed IGBT models, which consider all the capacitances, inductances and resistances associated with the IGBT, can be found in simulation programs with integrated circuit emphasis such as CAD tools, SPICE, SABER, etc., for real time simulation with an ultra-fast calculation speed, such models are neither necessary nor possible to execute (at least at the present time), due to the computational effort. As discussed in Section II, the main error comes from the voltage turn-on rate and turn-off rate of different voltage level. Thus, only turn-on rate and turn-off rate features of the IGBT are taken into account.

To control the switching behavior of HVIGBT, the digital control circuits as part of the gate drive unit are commonly used [14]. The basic idea is to use a set of parameters of HVIGBTs with the attempt to simulate achieve certain properties of the switching transients caused by the digital gate control unit. Its overall structure with a behavioral IGBT model can be seen in Fig. 5. The IGBT is replaced by its active region equivalent circuit model [15] [16] [17]. The gate is driven by an ideal step voltage source between V_{G+} and V_{G-} in series with an external gate resistance R_G. L_s is the parasitic inductance of the power electronic system. The switching transient performance is divided into several stages with different time intervals.

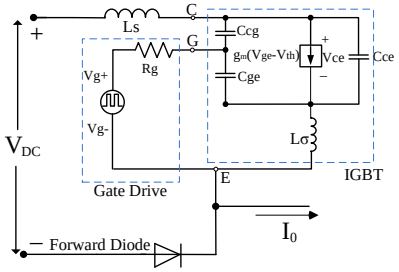
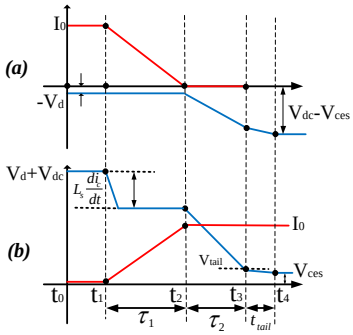


Fig 5. IGBT equivalent circuit

A. Inductive Turn-On Behavior Modeling



(a) Forward Diode turn-off waveform (b) IGBT turn-on waveform
Fig 6. Turn-on waveform under inductive load

The turn-on waveforms with inductive load considering the stray inductance Ls influence are shown in Fig. 6. The tail-voltage is represented by V_{tail}, which is approximated by $V_{tail} = k_{tail} \cdot (V_{dc} + V_d)$. The switching time intervals of tail-voltage is defined as t_{tail}. The switching time intervals defined in Fig. 6 can be calculated as follows:

$$\begin{aligned} t_0 = 0, t_1 &= t_0 + t_{d(on)} \\ t_2 &= t_1 + \frac{I_0}{\frac{dI_{ce}(\tau_1)}{dt}} \\ t_3 &= t_2 + \frac{(1-k)\cdot(V_d + V_{dc}) - L_s\frac{I_{ce}(\tau_1)}{dt} - V_{ces}}{\frac{dV_{ce}(\tau_2)}{dt}} \\ t_4 &= t_3 + t_{tail} \end{aligned} \quad (3)$$

And the rate-of-rise of voltage dV_{ce}/dt and of current dI_{ce}/dt during the turn-on process in the above equations can be expressed as [18][19][20].

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$$\frac{di_{ce}(\tau_1)}{dt} = \frac{g_m(V_g - V_{th}) - I_0}{R_g C_{ies} + g_m L_\sigma}$$
$$\frac{dv_{ce}(\tau_2)}{dt} = \frac{V_{th} - V_{g+} + I_0/g_m}{R_g C_{cg}} \quad (4)$$

During $[t_{0(on)}, t_{1(on)}]$, there is a turn-on delay time $t_{d(on)}$, within which the MOSFET channel is formed and IGBT is off. I_c and V_{ce} are defined as

$$I_{ce} = 0$$
$$V_{ce} = V_{dc} \quad (5)$$

During $[t_{1(on)}, t_{2(on)}]$, the current I_L starts to transfer from the freewheeling diode to the IGBT. The stray inductance L_s will cause the drop of V_{ce} as:

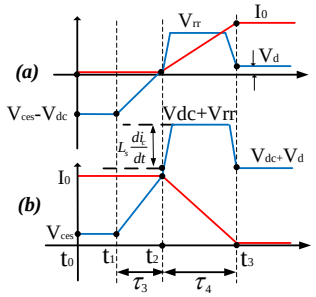
$$I_{ce} = \frac{di_{ce}(\tau_1)}{dt}(t - t_{1(on)})$$
$$V_{ce} = v_{dc} - Ls\frac{dv_{ce}(\tau_1)}{dt} \quad (6)$$

During $[t_{2(on)}, t_{3(on)}]$, the IGBT voltage will decrease to V_{tail} while current remains at I_0

$$I_{ce} = I_0$$
$$V_{ce} = V_{dc} + V_d - Ls\frac{dv_{ce}(\tau_1)}{dt} + \frac{dv_{ce}(\tau_2)}{dt}(t - t_{2(on)}) \quad (7)$$

Once the voltage reaches V_{tail}, a Miller capacitance C_{gc} occurs. With the time period of tail-voltage t_{tail}, we can approximate the tail voltage transient.

B. *Inductive Turn-off Behavior Modeling*



(a) Forward Diode turn-on waveform (b) IGBT turn-off waveform
Fig 7. Turn-off Waveform under Inductive Load

The inductive turn-off switching is shown in Fig. 7. The switching time intervals defined in Fig. 3 can be calculated as

$$t_0 = 0 \; and \; t_1 = t_0 + t_{d(off)}$$
$$t_2 = t_1 + \frac{V_{dc} - V_{ces}}{\frac{dV_{ce}(\tau_3)}{dt}}$$
$$t_3 = t_{d(off)} + \frac{V_{dc} - V_{ces}}{\frac{dV_{ce}(\tau_3)}{dt}} + \frac{I_0}{\frac{di_{ce}(\tau_4)}{dt}} \quad (8)$$

And the rate-of-rise of voltage dV_{ce}/dt and current dI_c/dt during the turn-off process in the above equations can be expressed as [18][19][20].

$$\frac{di_{ce}(\tau_4)}{dt} = \frac{g_m(V_{g-} - V_{th}) - I_L}{R_g C_{ies} + g_m L_\sigma}$$
$$\frac{dv_{ce}(\tau_3)}{dt} = \frac{V_{th} - V_{g-} + I_L/g_m}{R_g C_{cg}} \quad (9)$$

The turn-off process begins with a drop in the gate voltage V_{ge} . When it drops to the Miller plateau, the IGBT starts to build a reverse voltage. During $[t_{0(off)}, t_{1(off)}]$, the capacitance C_{ge} discharges. V_{ce} and I_c stays at their steady values.

$$I_{ce} = I_0$$
$$V_{ce} = V_{ces} \quad (10)$$

In period $[t_{1(off)}, t_{2(off)}]$, the diode is still reverse biased, which causes I_c unchanged

$$I_{ce} = I_0$$
$$V_{ce} = v_{ces} + \frac{dv_{ce}(\tau_3)}{dt}(t - t_{1(on)}) \quad (11)$$

In period $[t_{2(off)}, t_{3(off)}]$, the diode becomes forward biased. The collector current I_c starts falling and the voltage v_{ce} still continues increasing to $V_{dc} + V_{rrm}$ because of the existence of stray inductance L_s.

$$I_{ce} = I_0 + \frac{di_{ce}(\tau_4)}{dt}(t - t_{3(on)})$$
$$V_{ce} = V_{dc} + V_{rr} \quad (12)$$

The overvoltage on the IGBT can be approximated by $V_{rr} = L_s\frac{di_{ce}}{dt}$. As long as the collector current Ice reaches zero, the voltage v_{ce} falls back to $V_{dc} - V_d$

$$I_{ce} = 0$$
$$V_{ce} = V_{dc} - V_d \quad (13)$$

C. *Model Validation*

The above IGBT model utilizes the current and voltage rates in transient. In this part, a double pulse test is made to validate the rate during turn-on and turn-off period. The IGBT module used in this paper is FZ1200R33KF2C. It is a 3300V IHV 190mm single switch IGBT Module, which is generous application for traction and industry [26]. The double pulses test results are shown in Fig. 8 and Fig. 9. The parameter of the IGBT in the test is given in Table I.

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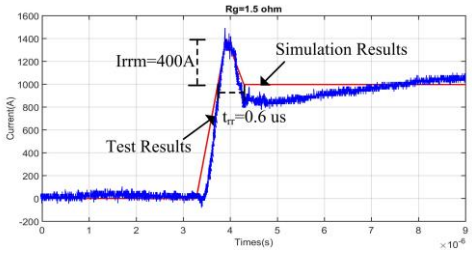
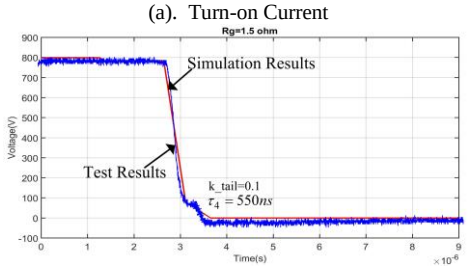
TABLE I
UNITS FOR IGBT PARAMETER

Symbol	Quantity	Value
R_G	*Driver gate resistor*	*1.5omh*
gm	*Forward Transconductance*	*259S*
Cies	*Input capacitance*	*220nF*
Cres	*Reverse transfer capacitance*	*2nF*
Ls	*IGBT Module Stray Inductance*	*110nH*
td_on	*Turn-on delay time*	*280ns*
td_off	*Turn-off delay time, inductive load*	*160ns*

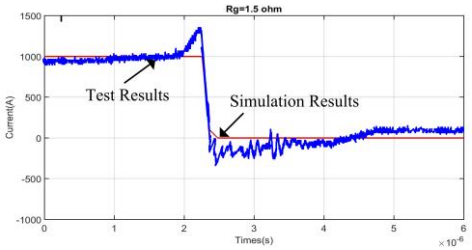


(a). Turn-on Current

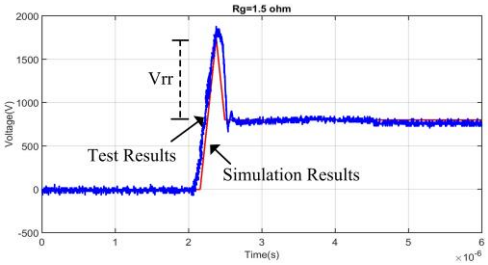


(b). Turn-on Voltage

Fig 8. Turn-on transient performance of IGBT (800V/1000A)



(a). Turn-off Current



(b). Turn-off Voltage

Fig 9. Turn-off transient performance of IGBT (800V/1000A)

The measuring results and the calculated di/dt and dv/dt during turn-on and turn-off period are shown in Fig. 8 and Fig. 9 with a gate resistor $R_G = 1.5\Omega$. In Fig .8, the overshoot phenomenon is caused by the freewheeling diode to the IGBT. With the maximum reverse current value I_{rrm} of the freewheeling diode and the diode reverse process period t_{rr}, the behavior model of the IGBT considering the effect of the freewheeling diode can be obtained [27]. The coefficient of the tail-voltage is set to $k_{tail} = 0.1$, the duration of the tail-voltage is 550 ns. In Fig.9, the overshoot in the turn-off voltage is caused by the stray inductance L_s. The value of the Ls is 110 nH, which causes the overvoltage V_{rr} reaching about 770V. The comparison illustrates that the current or current transient rate can be approximated by this model in an acceptable way.

IV. CIRCUIT SOLVER WITH FPGA

The high parallelism offered by FPGAs and their implementation have made it conduct a simulation within hundreds of nanoseconds. With FPGA platform, many papers have provided various methods to write the state-space based method for modeling and simulating power electronic cases [21]. They usually use lower order explicit integration method with a circuit partitioning to achieve a high execution speed. It usually introduces step latency between different sub-circuits, thus the accuracy could be compromised. The method proposed in this section is a parallel method which suited for modeling power electronic system.

A. Formulation and Solver of State Equations

The state-space model of a linear element is given by

$$\frac{dx}{dt} = Ax + Bu \tag{14}$$

where A, B are the state-space matrices, x is the sate vector and u is the input vector. For a power electronic simulation, variables are the voltage across the capacitance and the current flowing through the inductance. Compared with the common explicit method using only the known value $x[n]$ from last time point, our method is written in two steps: Prediction step (P-step) and Corrector-step (C-step).

P-step: Compute the predictor $\hat{x}_{n+2}$ by an explicit numeric solver method;

C-step: Apply the $\hat{x}_{n+1}$ using an implicit method to obtain the corrector x_{n+1};

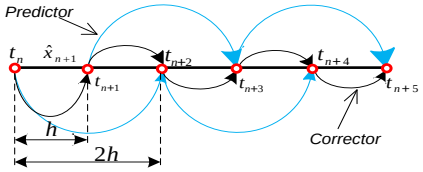


Fig 10. The Predictor-Corrector Solver

The time sequence of the method is shown in Fig 10. In the current time point t_n, it calculates the predictor value $\hat{x}_{n+2}$ at time point t_n during the process of solving x_{n+1} with known value x_n. In the next step t_{n+1}, when we estimate the value of x_{n+2}, the value of $\hat{x}_{n+2}$ will be already known from previous step t_n. Thus, $\hat{x}_{n+2}$ and x_{n+2} are known at the same time. Given the ordinary differential equation $\dot{x} = f(x,u)$, the combination of the 2 step Euler Backward Method are given by:

$$\mathbf{P-step}: \hat{x}_{n+2} = x_n + 2h \cdot f(t_n, x_n) \tag{15}$$

$$\mathbf{C-step}: x_{n+1} = x_n + h \cdot f(t_{n+1}, \hat{x}_{n+1}) \tag{16}$$

Assume that the truncation error is R_{n+1}, the exact solution value X_{n+1} at time point $t(n+1)$ can be calculated,

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$$X_{n+1} = R_{n+1} + x_n + h \cdot F_{n+1} \tag{17}$$

where $F_{n+1} = f(t_n, X(t_{n+1}))$

Assume $X_{n+2-i} = x_{n-i}, (i = 2,3 \ldots k-1)$, we can use the identity

$$\begin{aligned} X_{n+1} - x_{n+1} &= R_{n+1} + h\big(F_{n+1} - f(t_{n+1}, \hat{x}_{n+1})\big) \\ &= R_{n+1} + h\frac{\partial f(t_{n+1}, \varepsilon_{n+1})}{\partial x}(X_{n+1} - \hat{x}_{n+1}) \end{aligned} \tag{18}$$

where ε_{n+1} is a value between X_{n+1} and $\hat{x}_{n+1}$.

Since function f satisfies the Lipschitz continuity theory, a Lipschitz constant L_f meeting the conditions of $|f(x1) - f(x2)| \leq Lf\,|x1 - x2|$ for all $x1, x2 \in I$, hence

$$\left|\frac{\partial f(t_{n+1}, \varepsilon_{n+1})}{\partial x}\right| \leq Lf$$

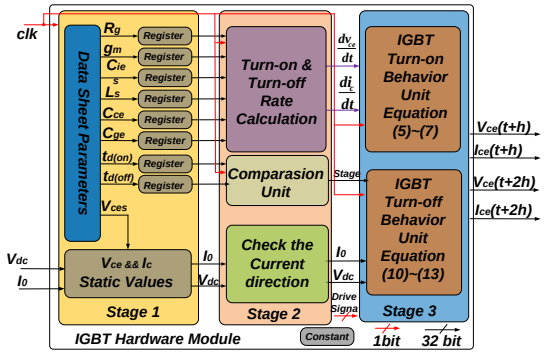
The global error of the predictor equation (Forward Euler Method) is $O(h)$ and the global error of the corrector equation (Backward Euler Method) is $O(h^2)$. Thus, the above equation can be rewritten as

$$\begin{aligned} |X_{n+1} - x_{n+1}| &\leq |R_{n+1}| + h \cdot Lf \cdot |X_{n+1} - \hat{x}_{n+1}| \\ &= |R_{n+1}| + h \cdot Lf \cdot \left|R^p_{n+1}\right| \\ &= O(h^2) + h \cdot Lf \cdot O(h) \\ &= O(h^2) \end{aligned} \tag{19}$$

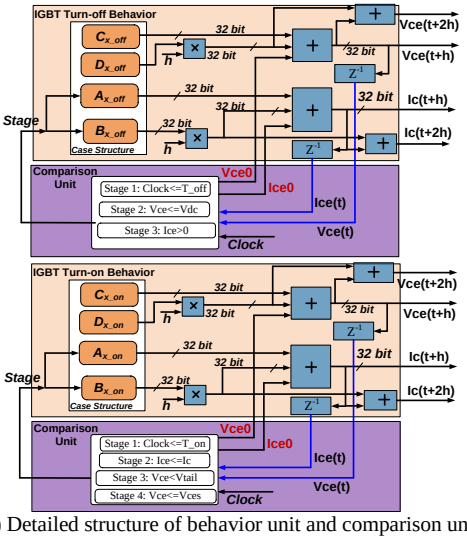
Thus, the equation proves that the order of the corrector equation and its corresponding parallel equation are 2. With this solver, we could reach the same speed as the forward Euler Method but more accurate.

This method can be used when the simulation time step is relatively small. Based on the above parallel strategy, a circuit partitioning method, which utilizes the predictor values to separate the IGBT semiconductor and circuit elements devices into different subsystem, could be achieved.

B. IGBT Behavior Model Implementation



(a) Overall Structure of IGBT model



(b) Detailed structure of behavior unit and comparison unit

Fig 11. Implementation of IGBT Model

The internal hardware structure of IGBT unit (shown in Fig. 11(a)) illustrates the interface with circuit element. The operation has three stages. The whole system starts to operate under the reset signal coming from the FPGA board. External voltage Vdc and current Ic is the prediction value from the circuit. The IGBT parameters are stored in register. The stage 1 is prior to the operation of another stage. The stage 2 read the parameter from stage 1 and is driven by the turn-on or turn-off signals from semiconductor driver circuit. It calculates the turn-on or turn-off rate. The stage 3 has a compare unit, where judges the different stages. At last, the unit calculates the voltage and current change.

There are total 12 equations ((5)-(7) and (10)-(13)) about the behavior model of the IGBT to be implemented on FPGA. A re-organized generic formulation is developed, which contains only 4 equations, to be implemented in the FPGA. Each equation is independent and can be calculated at the same time. Consider the proposed generic expression in (20),

$$\begin{aligned} I_{ce} &= I_{ce0} + A_x + B_x \cdot h \\ V_{ce} &= V_{ce0} + C_x + D_x \cdot h \end{aligned} \tag{20}$$

The coefficient in (20) is determined by equation ((5)-(7) and (10)-(13)) under different IGBT transient stage during turn-on or turn-off period. It should be noted B_x and D_x is the slop as expressed in (1), the numerical value ($\mathrm{V_{ce}}(\mathrm{t}+2\mathrm{h})$ and $\mathrm{I_{ce}}(\mathrm{t}+2\mathrm{h})$) can also be obtained at the current time point t. Their detailed structure is as shown in Fig. 11(b).

C. Circuit Element Simulation

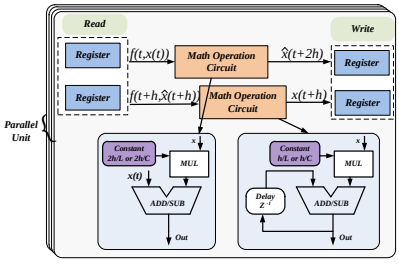


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Fig 12. Implementation of Circuit Element Model

The internal hardware structure of circuit element unit is shown in Fig. 12. Every element unit can be executed at the same time. Inside the framework, the circuit element has two layers. One is the C-step layer which calculates output variable $x(t+h)$. The other layer is the P-step layer which executes with a time step $2h$ to predict $\hat{x}(t+2h)$. Both of these two layers have a similar math calculation unit, consisting of fixed-point multiplications and Sub/Add operation. After the calculation is done, results are stored in register.

Since both P-step and C-step are executed at the same time, the total calculation time in this framework is determined by the longest route in Prediction step or Correction step. This framework is based on the explicit and implicit Euler method, which has the least number of math operation unit. Advantage could involve of a fast calculation speed and accurate solver process.

V. High Power Traction System Simulation Study

Traction system in high-speed train is a type of Megawatt power electronic system that provides the train with a significantly faster speed than traditional rail traffic. The application of high efficiency and high-power converters associating with motors under each carriage is one of its main features. Fig. 13 gives "AC-DC-AC" type of traction system in high speed train. It consists of two parts: the four-quadrant converter (4QC) and two-level inverter.

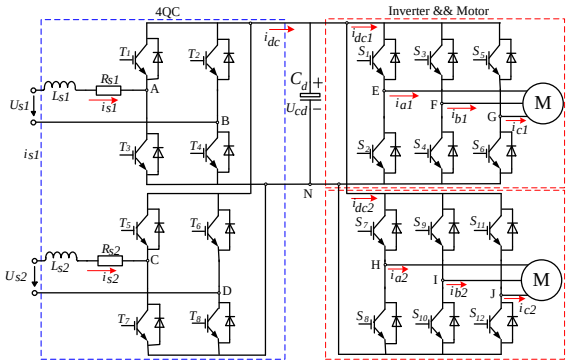

Fig 13. The Architecture Diagrams of Traction System

A. Circuit Modeling

The model for the traction system is based on the formation of state-space equation. The current $is1$ is calculated by the (21):

$$L_{s1}\frac{di_{s1}}{dt} = u_{s1} - R_{s1}i_{s1} - U_{ab} \tag{21}$$

Its discretization formulation with Predictor-Corrector can be expressed as (22),

$$\begin{aligned}\hat{i}_{s1(n+2)} &= i_{s(n)} + \frac{2h}{L_{s1}}\left(u_{s1(n)} - R_{s1}i_{s1(n)} - U_{ab(n)}\right)\\ i_{s1(n+1)} &= i_{s1(n)} + \frac{h}{L_{s1}}\left(u_{s1(n+1)} - R_{s1}\hat{i}_{s1(n+1)} - \hat{U}_{ab(n+1)}\right)\end{aligned} \tag{22}$$

Similarly, the current $is2$ can be calculated by (23),

$$\begin{aligned}\hat{i}_{s2(n+2)} &= i_{s(n)} + \frac{2h}{L_{s2}}\left(u_{s2(n)} - R_{s2}i_{s2(n)} - U_{cd(n)}\right)\\ i_{s2(n+1)} &= i_{s1(n)} + \frac{h}{L_{s2}}\left(u_{s2(n+1)} - R_{s2}\hat{i}_{s2(n+1)} - \hat{U}_{cd(n+1)}\right)\end{aligned} \tag{23}$$

As for the voltage udc, the mathematical expression can be described as (24):

$$C_d\frac{dU_c}{dt} = i_{dc} - i_{dc1} - i_{dc2} \tag{24}$$

where

$$\begin{aligned}I_{dc} &= -I_{T1} - I_{T2} - I_{T5} - I_{T6}\\ I_{dc1} &= I_{S1} + I_{S3} + I_{S5}\\ I_{dc2} &= I_{S7} + I_{S9} + I_{S11}\end{aligned}$$

Its discretization formation can be obtained in (25)

$$\begin{aligned}\hat{u}_{c(n+2)} &= u_{c(n)} + \frac{2h}{C_d}\cdot\left(i_{dc(n)} - i_{dc1(n)} - i_{dc2(n)}\right)\\ u_{c(n+1)} &= u_{c(n)} + \frac{h}{C_d}\cdot\left(\hat{i}_{dc(n+1)} - \hat{i}_{dc1(n+1)} - \hat{i}_{dc2(n+1)}\right)\end{aligned} \tag{25}$$

The motor model here is a generalized model based on the stator stationary reference frame. This model is described with electrical and rotor fluxes [22][23]. The mechanical characteristic can use the rotor electrical speed as state variable. The input variable $u_{s\alpha}, u_{s\beta}$ are the voltage U_{il}, U_{jl}, U_{kl} after Clark transformation. The model can be described by (26).

$$\begin{bmatrix}\frac{d\varphi_{r\alpha}}{dt}\\ \frac{d\varphi_{r\beta}}{dt}\\ \frac{di_{s\alpha}}{dt}\\ \frac{di_{s\beta}}{dt}\end{bmatrix} = A\cdot\begin{bmatrix}\varphi_{r\alpha}\\ \varphi_{r\beta}\\ i_{s\alpha}\\ i_{s\beta}\end{bmatrix} + B\cdot\begin{bmatrix}u_{s\alpha}\\ u_{s\beta}\\ 0\\ 0\end{bmatrix} \tag{26}$$

where,

$$A = \begin{bmatrix}-\frac{1}{T_r} & -\omega & \frac{L_m}{T_r} & 0\\ \omega & -\frac{1}{T_r} & 0 & \frac{L_m}{T_r}\\ \frac{L_m}{\sigma L_s L_r T_r} & \frac{L_m\omega}{\sigma L_s L_r T_r} & -\frac{R_s L^2{}_r + R_r L^2{}_m}{\sigma L_s L^2{}_r} & 0\\ \frac{-L_m\omega}{\sigma L_s L_r T_r} & \frac{L_m}{\sigma L_s L_r T_r} & 0 & -\frac{R_s L^2{}_r + R_r L^2{}_m}{\sigma L_s L^2{}_r}\end{bmatrix};$$

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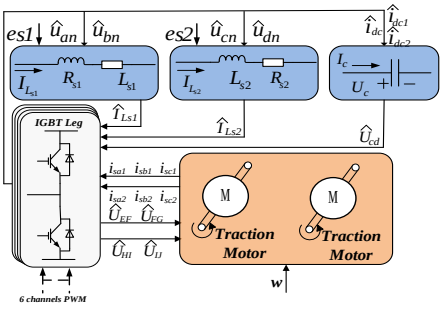
$$B=\begin{bmatrix}0 & 0 & 0 & 0\\ 0 & 0 & 0 & 0\\ 0 & 0 & \frac{1}{\sigma L_s} & 0\\ 0 & 0 & 0 & \frac{1}{\sigma L_s}\end{bmatrix};\sigma=1-\frac{L_m^2}{L_s L_r};T_r=\frac{L_r}{R_r}$$

$L_m$is the mutual inductance; L_{ls}, L_{lr} are the stator and rotor inductances; Rs, Rr are the stator and rotor resistances; n_p is the number of poles and J is the total rotor inertia. ω_r is the electrical rotor speed, which is calculated by the (27).

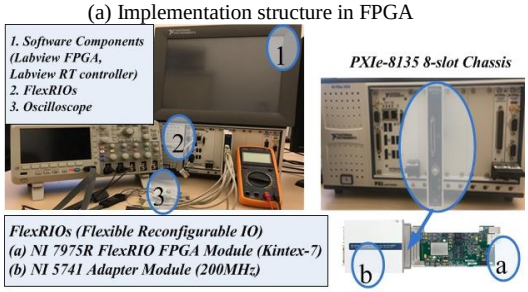
$$\frac{d\omega}{dt}=\frac{n_p^2 L_m}{JL_r}\left(i_{s\beta}\varphi_{r\alpha}-i_{s\alpha}\varphi_{r\beta}\right)-\frac{n_p}{J}T_L \qquad (27)$$

B. FPGA implementation

The implementation of a hardware calculation in real-time is benefited from parallel calculation method in Section III. It only consists of accumulators and addition or subtraction operation. Each subsystem can predict or calculate the state of single circuit element. With the prediction value, the whole circuit is divided into several levels of parallel subsystems, shown in Fig 14(a). The calculation time is able to reduce largely in this way. Compared with Forward Euler method, the accuracy and stable are enhanced with the introduction of both prediction and correction process.



(a) Implementation structure in FPGA



(b) PXIe-8135 NI Platform

Fig 14. Real-time Simulation Software and Hardware Setup

The hardware setup for the case studies is presented in Fig.14. The Kintex-7 XC7K410T FPGA is embedded in the NI PXIe-7975R FlexRIO PXI Express FPGA module [24], which has 400 Mb/s single-ended configuration rates [25]. Each unit in Fig. 14(a) is realized by the Single-cycle Timed Loop (SCTL) provided by LabVIEW FPGA Module. The shift register is used to pass data between different units. The hardware consumption in this case study is presented in Table II. It reports the speed performance and area utilization achieved by the proposed solvers on the FPGA board. The approach adopted in this paper relies on the fixed-point representation. A 40MHz Frequency is met in final timing routing. With the 40 MHz clock in the SCTL, the latency in the traction model is 3 while the latency in the IGBT model and the circuit element is only 1.

TABLE II. HARDWARE RESOURCE UTILIZATION FOR THE CASE STUDY

Resources	Total	Used	Percentage
Total Slices	633550	248985	39.3%
Slice Registers	508400	49823	9.8%
Slice LUTs	254200	68876	27.1%
Block RAMs	795	101	12.7%
DSP48s	1540	410	26.6%

C. Simulation results

The IGBT modules used in the inverter is FZ1200R33KF2C [26] (3300 V, 1200 A). Simulation Parameters in the traction system are shown in Table III. The input voltage source $Us1$ and $Us2$ are sinusoid waveform with 3600V amplitude and 50Hz frequency. An open loop control PWM pulses (carrier frequency is 2000 Hz, the modulation index is 0.4, and output voltage frequency is 50 Hz) is used to control the inverter. On the other hand, with the attempt to verify the IGBT model diversity, the four-quarter-converter will operate in uncontrollable converter status.

TABLE III
UNITS FOR MAGNETIC PROPERTIES

Symbol	Quantity	Value
L_{s1}, L_{s2}	*Inductance*	*2mH*
R_s	*Resistor*	*0.039omh*
C_d	*Capacitance*	*9.01mF*
R_G	*Driver gate resistor*	*10omh*
R_{s1}, R_{s2}	*Stator and Rotor Resistance*	*0.087omh*
L_{sl1}, L_{sl2}	*Stator and Rotor Inductance*	*8.01e-04H*
L_m	*Mutual Inductance*	*0.03469 H*
gm	*Forward Transconductance*	*259S*
Cies	*Input capacitance*	*220nF*
Cres	*Reverse transfer capacitance*	*2nF*
Ls	*IGBT Module Stray Inductance*	*10nH*
td_on	*Turn-on delay time*	*280ns*
td_off	*Turn-off delay time, inductive load*	*160ns*

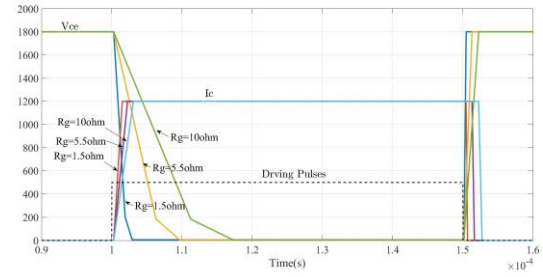


Fig 15. IGBT Transient Performance with different gate driver resistor(1800V/1200A)

When the gate resistors changes, the turn-off voltage rate stage and turn-on voltage falling rate will change accordingly. In Fig 15, we test the gate resistor R_g with the value of 1.5Ω, 5.5Ω and 10Ω respectively. As the gate resistance is increased, both the turn-off voltage rate stage and turn-on voltage falling rate are decreased. Due to the relatively small stray inductance

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value (10nH) in the FZ1200R33KF2C module [26], the overvoltage V_{rr} is less than 70V. Consider the voltage range (1800V), both the voltage drop value during turn-on period and overvoltage value in the turn-off voltage are not obvious.

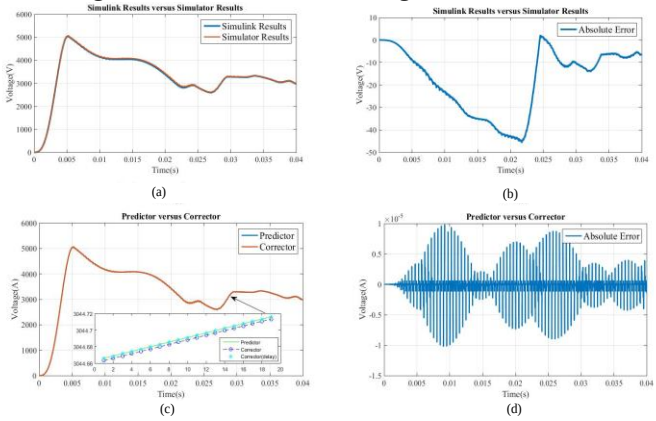

Fig 16. Voltage waveform of u_{cd} between capacitance C_d

Fig. 16 represents the voltage u_{cd}. Fig. 16(a) is the comparison with Matlab/Simulink. Their corresponding absolute error is shown in Fig 16(b). Considered its numerical value, this absolute error is acceptable. Fig. 16(c) is the comparison between predictor value and corrector value. The zoom-in part consists of 20 simulation steps. The predictor value $\hat{u}_{dc(n+2)}$ and corrector value $u_{dc(n+1)}$ has one-step latency (25ns). If we add one simulation step delay to the corrector $u_{dc(n+1)}$, $u_{dc(n)}$ will have a high agreement with predictor $\hat{u}_{dc(n)}$. Their difference is shown in Fig. 16(d) with the expression with absolute error. The maximum absolute error is 1e-5 V.

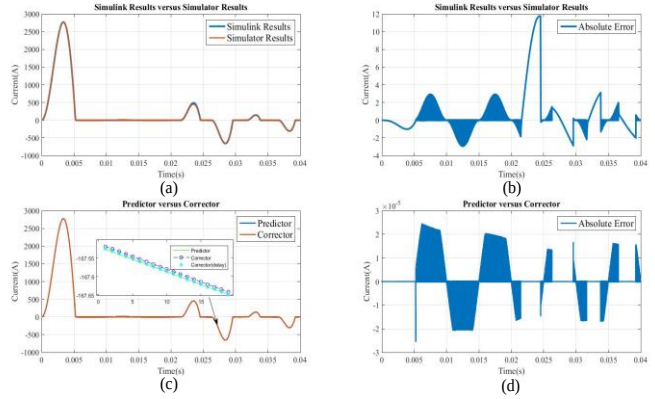

Fig 17. Current waveform of I_{Ls1} flowing through inductance Ls1

Fig. 17 is the current waveform of I_{Ls1}. When the current is positive, it flows through the anti-parallel diode in T1. Otherwise, the current path is through diode in T3. The comparison with Matlab/Simulink is shown in Fig. 17(a), accompanied by the absolute error (shown in Fig. 2(b)). The Fig. 17(c) is the comparison between predictor value and corrector value. The zoom-in part contains 20 simulation steps. The correction value is one-time step (25ns) behind the prediction value, but the absolute error (Fig. 17(d)) between them is less than 3e-5 A. It is consistent with the modeling time sequence of circuit solver.

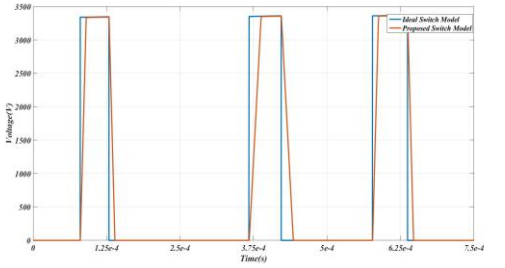

Fig 18. Transient performance of phase-to-phase voltage V_{FG}

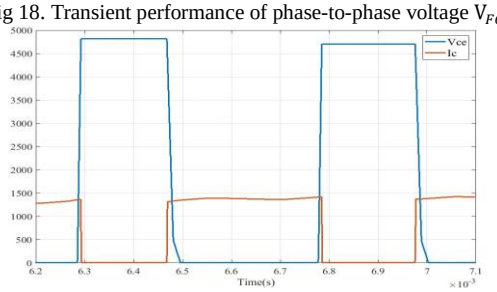

Fig 19. Transient performance of IGBT S1

The transient behavior of the phase-to-phase voltage V_{FG} and transient performance of IGBT S1 can ben seen in Fig. 18 and Fig. 19 respectively. In Fig. 18, the blue line is a voltage output with ideal switch model. The different turn-on and turn-off rate of the voltage in red line is caused by different current rate flowing through the IGBT. Fig 19 is the transient performance of the IGBT during turn-on and turn-off period.

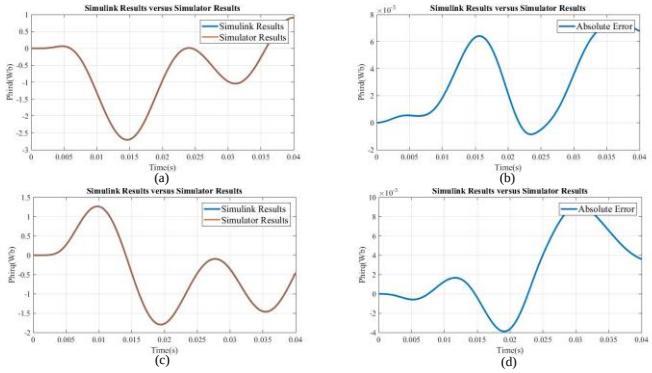

Fig 20. Flux waveform (the stationary reference frame) in the traction motor

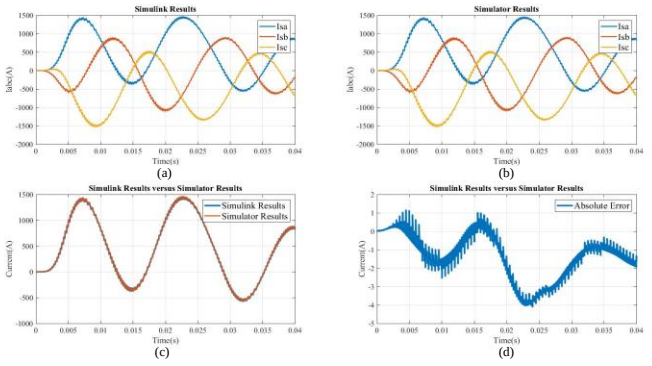

Fig 21. Current waveform in the traction motor

The machine is connected to a constant rotor speed (80 rad/s). Fig. 20 is the flux waveform of the rotor in the stationary reference frame. Fig.20(a) is the rotor flux in the d frame. The difference with Matlab/Simulink results is lower than 7e-3. Fig.20 (b) is the rotor lux in the q frame. The absolute error is

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less than 8e-3 wb. Fig. 21 is the stator current comparison with Matlab/Simulink. As can be seen from Fig. 21(d), the absolute error is less than 4 A. The model has a high agreement with the Simulink Results.

The simulation results show that the proposed method can simulate the transient performance of the HVIGBT with different voltage and current external environment. The prediction value and correction value in the results have a highly agreement, which can be used as the data communication among different units.

VI. CONCLUSIONS

This paper presented a piece-wise behavior model of IGBT considering the parasite parameter and the driver resistance with the condition of inductive load. Compared with former work considering the transient performance, it benefits from the following aspects: 1) It is a piece-wise model, which could execute within 25 nanoseconds; 2) The proposed model considers the influence of the different voltages on the transient characteristics of IGBT turn-on and turn-off stages; 3) Most of the IGBT parameter in the model can be obtained from data sheet.

A parallel calculation solver based on FPGA is proposed. The presented method involved two processes, prediction and correction process. The prediction erases the latency between different subsystems and the correction solves the whole system in implicit method. Compared Explicit Euler method, the proposed prediction and correction method could solve and partition the system without time step latency. Compared with the modified Euler method, the proposed method reduces by half the calculation time with its parallel calculation structure.

The proposed modeling method has applied to a case study about the traction system in high speed train. This case has been implemented in FlexRIO PXIe-7975R. The IGBT model could be finished within 25ns. The results could provide insight into the transient behavior of the traction system.

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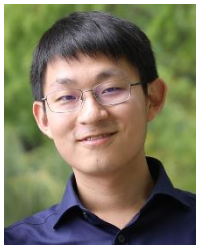

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