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A Reliable Three-Phase Single-Stage Multi-Port Inverter for Grid-Connected Photovoltaic Applications

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***Abstract*— This paper presents a new three-phase Single-Stage Multi-Port Inverter (SSMPI). The proposed topology contains no electrolytic capacitors. Therefore, its reliability and lifetime are improved in comparison with well-known two-stage multi-port Voltage Source Inverters (VSIs). In addition, the SSMPI has a modular structure and the number of input ports can be easily increased. The input ports of the SSMPI can be fed by different Photovoltaic (PV) strings. Therefore, the SSMPI can be used in photovoltaic power plants with multiple PV strings to enhance the reliability and the lifetime of the power plant. The SSMPI can extract the maximum power from multiple PV strings with different irradiations, orientations and characteristics. In this paper, the SSMPI structure and its challenges in switching command generation and control are explained. Afterward, a new switching algorithm based on Space Vector Modulation (SVM) and a novel control strategy are developed to fulfill the requirements of the SSMPI. The simulation and experimental test results of a 2.4 kW prototype show that the proposed converter can inject three-phase currents to the grid with a unity power factor and without using any ac current sensors. Moreover, the maximum power is extracted from the input ports in different test conditions.**

***Index Terms*— electrolytic capacitor elimination, grid-connected inverter, multi-port converter, maximum power point tracking, photovoltaics.**

I. Introduction

In recent years, the share of renewable energy sources, especially solar and wind, for electricity generation has been increased and it is expected to see further growth of photovoltaic power plants in the next decades [1]. The reliability and the maximum power extraction are two important parameters of the photovoltaic power plants. Solar inverters have an important role in determining these two parameters [2]. Different types of solar inverters are used for integration of PV systems into the electricity network. Among them, multi-string inverters are appropriate and economical solutions for grid-connected PV systems due to their beneficial features such as flexibility, controllability and reliability [2]–[9]. In the multi-string structure, the number of strings can be increased easily. Furthermore, each string can be controlled independently and the net energy yield can be maximized.

A lot of research has been conducted to evaluate and improve the performance of the two-stage multi-string VSIs [3]–[6], [10]–[12]. Although, multi-string voltage source inverters are very popular, they need bulky electrolytic capacitors, which restrict their lifetime and they are known as a cause of reliability reduction and inverter failure [13]–[20]. Therefore, converters without electrolytic capacitors are preferred from the reliability viewpoint. Much research has been done to eliminate the electrolytic capacitors in the converters or to reduce their required capacity. In [8] and [21], electrolytic capacitors are omitted by using a high-frequency ac link. In the multi-string single-stage inverters with a high-frequency link, the circulating power in the high-frequency link affects the efficiency. Furthermore, due to interrupted input currents, large input capacitors are required to draw smooth currents from the PV strings, which may restrict the lifetime. The topology proposed in [8] provides a high-frequency isolation and utilizes no electrolytic capacitors, but it needs a relatively high number of semiconductor devices. Multi-string single-stage single-phase current-fed inverters are presented in [22]–[25]. These types of converters suffer from even harmonics and high ripple input currents and typically need large inductors. Furthermore, their application is limited to residential and low power systems. Single-stage three-phase Current Source Inverters (CSIs) for PV applications are studied in [26]–[35]. The main advantages of the three-phase single-stage CSIs are: continuous dc input currents, high reliability due to electrolytic capacitors elimination, inherent boost capability. Nonetheless, these structures encounter the lack of flexibility and poor energy harvesting due to the single input structure.

In this paper, a new three-phase Single-Stage Multi-Port Inverter (SSMPI) is presented, which not only preserves the aforementioned advantages of the current fed topologies, but also accumulates the beneficial features of the multi-string inverters. In the SSMPI, reliability and lifetime are increased by removing the bulky electrolytic capacitors. The proposed topology with the presented control strategy ensures the maximum power extraction from different PV strings. The efficiency of the SSMPI is improved by using Silicon Carbide (SiC) power devices and proper switching schemes.

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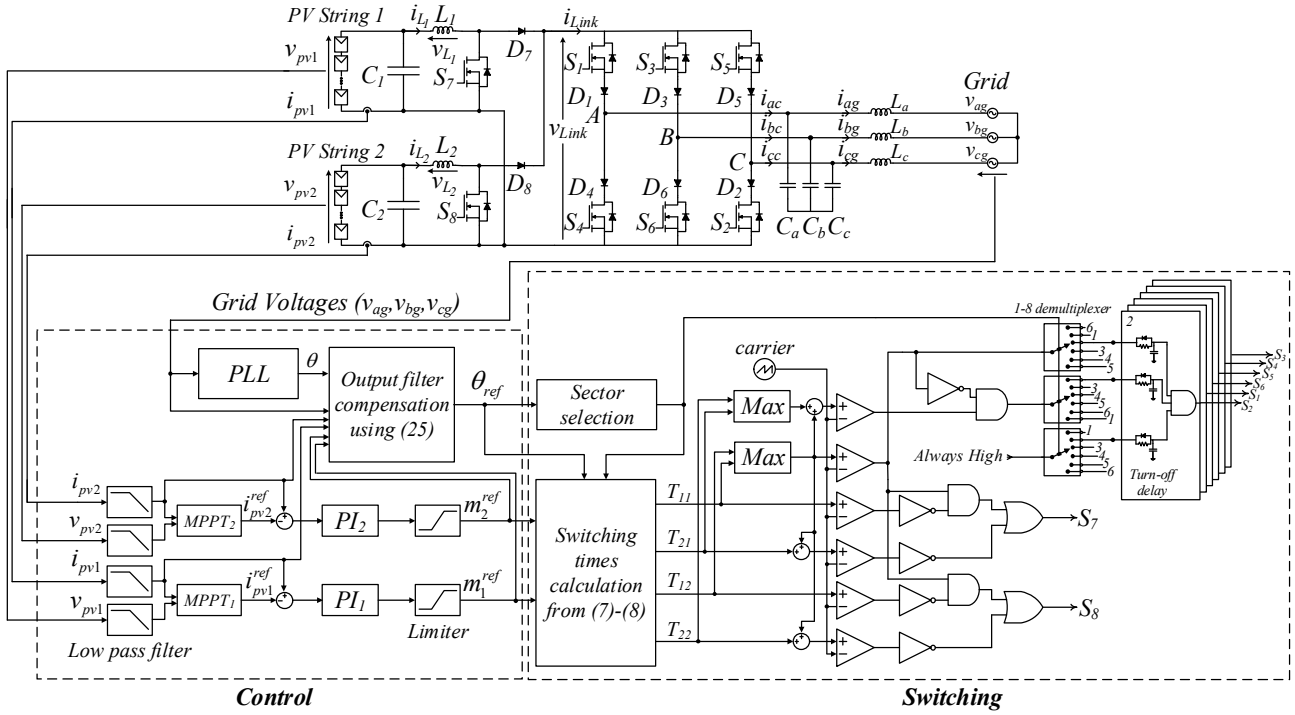

Fig. 1. Topology of the Single-Stage Multi-Port Inverter (SSMPI), with its control block diagram and switching algorithm implementation.

The rest of the paper is organized as follows: section II describes the configuration of the proposed topology and its switching states. Section III demonstrates the switching algorithm of the converter. The switching requirements such as providing a continuous current path and a balanced volt-second product for the dc inductors are discussed in this section. An appropriate switching pattern is suggested to meet these requirements. Section IV introduces the control scheme of the system. Extracting the maximum power from the input ports and realizing a unity power factor operation without using ac current sensors is explained in this section. The reliability improvement by using the SSMPI is analyzed in section V. Simulation and experimental test results along with performance comparisons with other topologies are provided in sections VI and VII.

II. Proposed Topology and its Switching States

A. The SSMPI topology

The SSMPI with two input ports is shown in Fig. 1. Each input is fed by an individual PV string. Due to the modularity of this topology, the number of input ports can easily be increased. Compared with the well-known two-stage multi-input VSIs with an LCL output filter ([3], [12], [36]–[39]), the dc link capacitors and the converter-side output filter inductors are eliminated in the SSMPI. Elimination of the electrolytic capacitor improves the reliability of the converter. In addition, the dc link capacitors and the output filter inductors are large components in the two-stage VSI. Therefore, eliminating them in the proposed converter leads to a reduction of the converter weight and volume.

The SSMPI is a single-stage topology. Therefore, its control is different from the two-stage multi-input VSIs control method; where the dc link capacitors decouple the PV-side converter from the grid-side converter. Moreover, in contrast to the two-stage VSIs, the switching commands of all the switches in the proposed converter should be synchronized to provide a continuous current path for the input inductors currents. In addition, a balanced volt-second product should be provided for the input inductors. With respect to these facts, two questions should be answered for the proposed topology:

- How to determine the modulation index for S_1-S_6, while no common dc link and no ac current sensors exist.
- How to generate the gate pulses in order to satisfy the switching requirements and also realize an independent operation for all the input ports.

These questions are answered in the next sections. Also, it is proved that the SSMPI with the proposed switching and control strategies, is able to extract the maximum available power from the individual PV strings with different operating conditions and characteristics. A unity power operation with an acceptable Total Harmonic Distortion (THD) is also reached by the proposed structure, without using any ac current sensors.

B. Switching states of the SSMPI

In order to maintain the continuity of the dc inductor currents, S_1-S_6 should provide a current path when S_7 or S_8 is turned off. Under this constraint, the SSMPI has 18 active and one zero switching states. In the zero state both of S_7 and S_8 are turned on and all the output side switches (S_1-S_6) are turned off. Also, in order to implement each active state, two output side switches must be turned on and at least one of S_7 or S_8 must be turned off. It is important to note that in the two-stage VSIs or CSIs, the switching states of the input and output stages are independent; but in the SSMPI all the switching commands are synchronized with each other. The

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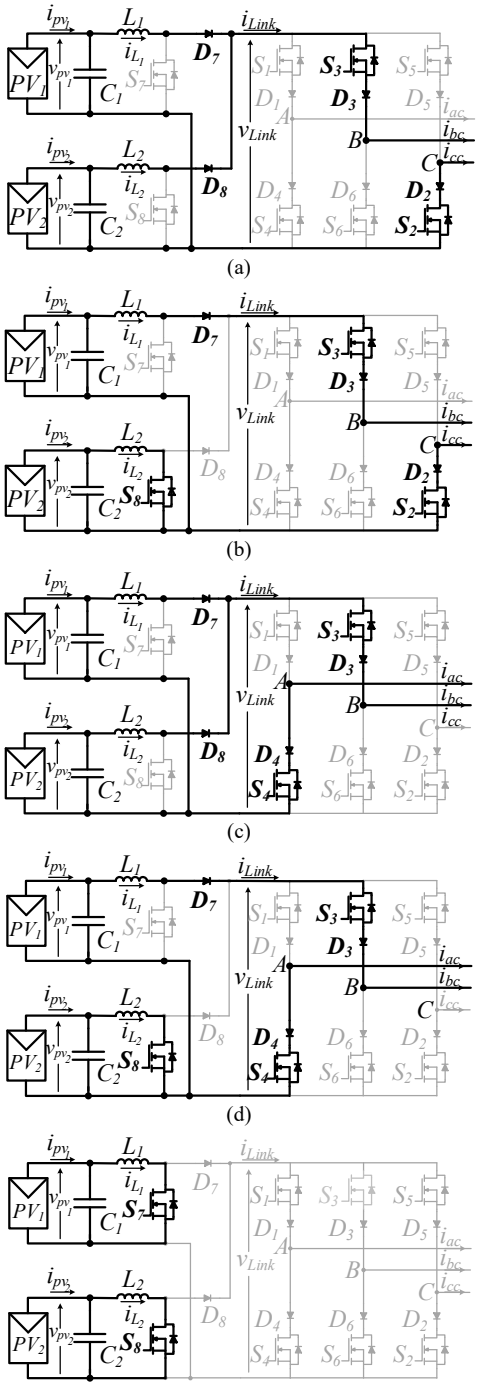

Fig. 2. Different switching states of the SSMPI with two independent PV strings with the assumption that $i_{pv1} < i_{pv2}$.

reference output current is synthesized using a combination of four active states followed by a zero state with specific dwell times in each switching cycle. As an example, different switching states in one switching period are shown in Fig. 2. In this case, it is assumed that $i_{pv1} < i_{pv2}$. As it can be seen, the first switching state is {23} (Fig. 2(a)), in which a current equal to $i_{pv1}+i_{pv2}$ is injected to the phase b. the second state is {23-8} (Fig. 2(b)). In this state, S_8 is turned on and the second input current is bypassed. With respect to Fig. 2, It can be observed that the switching states in which only S_7 is on are not used when $i_{pv1} < i_{pv2}$. Therefore, from 18 active states only

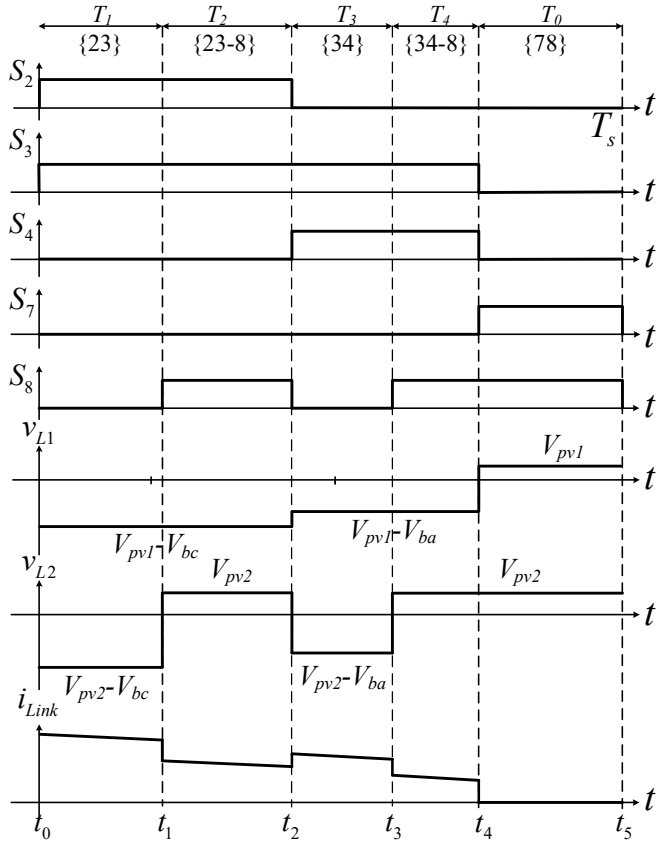

Fig. 3. Switching states and key waveforms of the SSMPI having two PV strings with the assumption that $i_{pv1} < i_{pv2}$.

12 of them are used. The details of the switching sequence and gate commands are illustrated in Fig. 3. As it can be seen in Fig. 3, the switching pattern of S_8 is different from the switching pattern used in the conventional boost converters. Therefore, a proper strategy is required to calculate the switching states dwell times and generate the required pattern.

III. Switching Algorithm

A. Dwell time calculation for the switching states

In the SSMPI, i_{link} and v_{link} are not constant and depend on the state of the switches. Furthermore, the input currents (i_{pv1} and i_{pv2}) in Fig. 1 are not equal and may vary with time. Therefore, based on the SVM technique [40] and using the superposition theorem, two space vector diagrams can be plotted as shown in Fig. 4, with the assumption that $i_{pv1} < i_{pv2}$. In Fig. 4 (a), it is assumed that only the first string is present and in Fig. 4 (b), only the second string is considered. Therefore, the active space vectors in Fig. 4 can be expressed as:

$$\vec{I}_{k1} = \frac{2}{\sqrt{3}} i_{pv1} e^{j\left(\frac{(k-1)\pi}{3} - \frac{\pi}{6}\right)}, \quad 1 \le k \le 6 \tag{1}$$

$$\vec{I}_{k2} = \frac{2}{\sqrt{3}} i_{pv2} e^{j\left(\frac{(k-1)\pi}{3} - \frac{\pi}{6}\right)}, \quad 1 \le k \le 6 \tag{2}$$

Where k is the sector number. Based on the phase angle of the reference current (θ_{ref}), the appropriate sector and adjacent space vectors are identified. In Fig. 4, it is arbitrarily assumed

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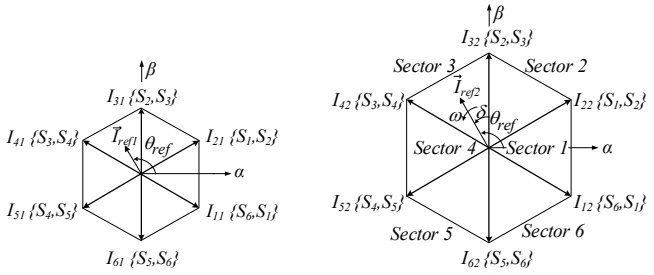

Fig. 4. Space vector diagrams assuming $i_{pv1} < i_{pv2}$ (a) when only string 1 is present, (b) when only string 2 is present.

that the reference current is located in the third sector. The output reference current ($\vec{I}_{Cref}$) is defined as:

$$\vec{I}_{Cref} = \vec{I}_{ref1} + \vec{I}_{ref2}$$
$$\left|\vec{I}_{Cref}\right| = \left|\vec{I}_{ref1} + \vec{I}_{ref2}\right| = m_1^{ref} i_{pv1} + m_2^{ref} i_{pv2} \quad (3)$$

Where the modulation indexes can be expressed as:

$$m_i^{ref} = \frac{\left|\vec{I}_{refi}\right|}{i_{pvi}}, \qquad i = 1,2 \quad (4)$$

The reference current is synthesized using a combination of selected space vectors with specific dwell times. Calculation of the dwell times is based on the ampere-second balance principle, which can be formulated as:

$$T_s \vec{I}_{refi} = T_{1i}\vec{I}_{3i} + T_{2i}\vec{I}_{4i} + T_{0i}\vec{I}_{0i}, \qquad i = 1,2 \quad (5)$$

$$T_s = T_{1i} + T_{2i} + T_{0i}, \qquad i = 1,2 \quad (6)$$

Where T_s is the switching period and T_{1i} and T_{2i} are the dwell times for the nearby space vectors $\vec{I}_{3i}$ and $\vec{I}_{4i}$, respectively. Substituting for current vectors in (5)-(6) and solving the resultant equations leads to:

$$T_{1i} = m_i^{ref} T_s \,\mathrm{Sin}(\frac{\pi}{3} - \delta), \qquad 0 < \delta \le \frac{\pi}{3} \quad (7)$$

$$T_{2i} = m_i^{ref} T_s \,\mathrm{Sin}(\delta), \qquad 0 < \delta \le \frac{\pi}{3} \quad (8)$$

$$T_{0i} = T_s\left(1 - m_i^{ref}\,\mathrm{Sin}(\delta + \frac{\pi}{3})\right), \qquad 0 < \delta \le \frac{\pi}{3} \quad (9)$$

Where δ is defined in Fig. 4. From (7)-(9) it can be concluded that the largest modulation index corresponds to the largest dwell times for the active vectors. With respect to the switching states and the gate pulses in Fig. 3, the dwell time for each switching state when $i_{pv1} < i_{pv2}$, can be calculated as:

$$T_1 = T_{12} \quad (10)$$

$$T_2 = T_{11} - T_{12} \quad (11)$$

$$T_3 = T_{22} \quad (12)$$

$$T_4 = T_{21} - T_{22} \quad (13)$$

$$T_0 = T_s - T_{11} - T_{12} \quad (14)$$

As it can be seen, the reference angle and the modulation indexes are required to calculate the switching times. These parameters are obtained from the control routine as explained in the next section. Knowing the switching times, a procedure is required to generate the specified switching pattern.

B. Generation of the switching pattern

After calculating the switching times, the circuit shown in Fig. 1 is used to generate the switching commands. For driving S_7 and S_8, four pulses with a frequency of $1/T_s$ and the pulse width equal to T_{11}, $T_{1max}+T_{21}$, T_{12}, $T_{1max}+T_{22}$ are generated; where T_{1max} is defined as the maximum of T_{11} and T_{12}. The same carrier signal is used for all the switches to achieve a synchronized switching scheme. The required switching pattern for S_7 and S_8 is generated by using 8 logic gates as shown in Fig. 1.

Based on the presented switching algorithm, no extra calculations are necessary to generate the switching commands for S_1-S_6. As it can be seen in Fig. 1, the maximum of T_{11} and T_{12} and the maximum of T_{21} and T_{22} are used to generate the switching pulses. Two pulses with the widths of T_{1max} and T_{2max} are generated by means of the logic gates and fed into two demultiplexers (T_{2max} is the maximum of T_{21} and T_{22}). The input of the third demultiplexer is always high. The numbers associated with the outputs of the demultiplexers correspond to the inverter switches S_1-S_6. It should be noted that the switch position of the demultiplexers from up to down correspond to the six sectors shown in Fig. 4. In order to avoid an open circuit of the dc inductor, a small overlapping time is added by means of Resistor-Capacitor-Diode (RCD) circuits shown in Fig. 1. Three RCD circuits are used for each switch of the CSI. The outputs of these RCD circuits are connected to an AND gate which produces the final gate pulse for S_1-S_6. The corresponding circuit for generating the gate pulse of S_2 is only shown in Fig. 1.

C. Waveforms analysis

It is assumed that two different PV strings are connected to the input ports of the converter and $i_{pv1} < i_{pv2}$. Also with respect to (4), $m_1^{ref} > m_2^{ref}$. The gate pulses of S_2, S_3, S_4, S_7 and S_8 along with the voltage across the input inductors (v_{L1} and v_{L2}) and the link current (i_{link}) are illustrated in Fig. 3. T_{11} and T_{21} are determined by m_1^{ref} and they are larger than T_{12} and T_{22}, respectively. As shown in Fig. 3, S_2 and S_3 are conducting from t_0 to t_1 (for T_{12} seconds) and the link voltage is equal to V_{bc} and the link current is the sum of i_{L1} and i_{L2} (Fig. 2(a)). At t_1, S_8 is turned on. By turning on S_8, D_8 is turned off with the reverse voltage of V_{bc}. From t_1 to t_2, the link current is equal to i_{L1} and the link voltage is still equal to V_{bc}. This switching state is illustrated in Fig. 2(b), in which L_1 is discharging and L_2 is charging. At t_2, S_8 and S_2 are turned off and S_4 is turned on. From t_2 to t_3, the link voltage is equal to V_{ba}, the link current is equal to $i_{L1}+i_{L2}$ and both inductors are discharging (Fig. 2 (c)). At t_3, S_8 is turned on and D_8 is turned off again. From t_3 to t_4, the link current is equal to i_{L1} and the link voltage is equal to V_{ba} (Fig. 2(d)). At t_4, S_7 is also turned on and D_7 is reverse biased with the voltage V_{ba}. Therefore, the link current falls to zero. From t_4 to t_5 both input inductors are charging (Fig. 2 (e)). As it can be seen, all of S_1-S_6 are turned off and the inductors currents are conducted by just one switch. In the conventional single-stage CSIs, the dc inductor current passes through four semiconductor devices (two diodes and two switches) when applying a zero vector in which two switches from one leg are turned on. Therefore, the conduction losses would be rather high, especially when the

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dc input voltage is very low and the zero vector dwell time has a large value. Reduction of conducting semiconductor devices from four to one in this operating mode of the SSMPI decreases the conduction losses significantly and compensates the additional losses caused by adding D_7 and D_8.

Based on the presented switching algorithm and with reference to Fig. 3, the duty cycle of input-side switches can be expressed as:

$$D_{S_7} = 1 - m_1^{ref}\ \mathrm{Sin}(\delta + \frac{\pi}{3}), \qquad 0 \le \delta < \frac{\pi}{3} \tag{15}$$

$$D_{S_8} = 1 - m_2^{ref}\ \mathrm{Sin}(\delta + \frac{\pi}{3}), \qquad 0 \le \delta < \frac{\pi}{3} \tag{16}$$

D. Volt-second balance of the input inductors

The inductor volt-second balance should be maintained at the steady-state condition. With respect to the voltage of the inductors in Fig. 3, the volt-second balance can be written as:

$$T_{1i}(V_{pvi} - V_{bc}) + T_{2i}(V_{pvi} - V_{ba}) + V_{pvi}T_{0i} = 0, \qquad i = 1,2 \tag{17}$$

Which can be simplified as:

$$T_{1i}V_{bc} + T_{2i}V_{ba} = V_{pvi}T_s, \qquad i = 1,2 \tag{18}$$

The right term of (18) is a constant value and as a result the left term of the equation should be constant during one switching period. Assuming a unity power factor at the output side of the SSMPI and the α-β plane as shown in Fig. 4 three-phase line-to-line voltages are given by:

$$v_{ab}(t) = \sqrt{3}V_m\ \mathrm{Cos}(\omega t + \frac{\pi}{6}) \tag{19}$$

$$v_{bc}(t) = \sqrt{3}V_m\ \mathrm{Cos}(\omega t + \frac{\pi}{6} - \frac{2\pi}{3}) \tag{20}$$

Replacing for the switching times in (18) from (7) and (8) and also replacing for the related line-to-line voltages from (19)-(20) and doing some mathematical operations leads to:

$$\frac{3}{2}m_i^{ref}V_m = V_{pvi}, \qquad i = 1,2 \tag{21}$$

Therefore, the volt-second balance requirement can be met by using the calculated switching times and the switching pattern as shown in Fig. 3.

IV. Control Strategy

The control block diagram of the SSMPI is illustrated in Fig. 1. It is assumed that two independent PV strings are connected to the input ports of the SSMPI. The reference modulation indexes (m_1^{ref}, m_2^{ref}) obtained from the controllers are used by the switching algorithm to generate the required gate signals. In addition to the modulation indexes, a reference angle is also needed to define the switching times. The reference angle is used for all the switches to realize a synchronized switching pattern. The reference angle is determined from the phase of the grid voltage as demonstrated in Fig. 1. The grid voltage phase angle (θ) is obtained from the PLL block. In order to achieve a unity power factor operation, the phase displacement due to the output CL filter is compensated and the reference angle (θ_{ref}) is attained. To do this, the following relationship between the grid side and the converter side currents with respect to Fig. 1 can be written:

$$I_c = I_g(1 - \omega^2 L_f C_f) + jV_g\omega C_f \tag{22}$$

Where I_c and I_g are the phasor of the converter-side and grid-side output currents, respectively. C_f and L_f are the output filter capacitor and inductor values. From (22) I_g can be calculated as:

$$I_g = \frac{\sqrt{|I_c|^2 - (V_g\omega C_f)^2}}{1 - \omega^2 L_f C_f} \tag{23}$$

By replacing $|I_c|$ in (23), the grid current can be expressed as:

$$I_g = \frac{\sqrt{(m_1^{ref}I_{pv1} + m_2^{ref}I_{pv2})^2 - (V_g\omega C_f)^2}}{1 - \omega^2 L_f C_f} \tag{24}$$

The value of I_g obtained from (24) is used to calculate the reference angle. For a unity power operation, the grid voltage (V_g) and the grid current (I_g) should be in phase; therefore, the required phase angle of I_c relative to the grid voltage from (22) is determined by:

$$\theta_{ref} = \angle I_c = \theta + \tan^{-1}\left(\frac{V_g\omega C_f}{I_g(1 - \omega^2 L_f C_f)}\right) \tag{25}$$

The reference angle along with the modulation indexes are used by the switching algorithm to generate the appropriate switching commands. As it can be observed, all required parameters are extracted without any ac current measurements. Thus, isolated ac current sensors can be eliminated. Moreover, the intermediate dc link and its sensor which is commonly used in the two-stage VSIs and CSIs, are removed. As a result, the number of required controllers are also reduced, which simplifies the implementation of the control routine and saves the resources.

V. Reliability Improvement

While the PV modules lifetime has reached 20 years, the inverters have a lower lifetime and are known as the main cause of reliability issues in PV power plants [41], [42]. Inverter failure not only increases the maintenance cost, but also leads to the loss of opportunity to produce power in the repairing interval. The semiconductor switches and the electrolytic capacitors are two vulnerable components and have the most important role in inverter failures [43]. In the SSMPI, the number of semiconductor switches is the same as the two-stage VSIs, but the electrolytic capacitors are eliminated. Therefore, a significant improvement in reliability is achieved.

In order to compare the reliability of the SSMPI and the conventional two-stage VSI, the failure rates of the components are calculated based on the data and methods presented in [44], [45]. According to [44], the failure rate of each component can be calculated by multiplying the base failure rate by the acceleration factors. The failure rate of the semiconductor switches, capacitors, diodes and inductors are calculated as follows, respectively:

$$\lambda_{SW} = \lambda_b\pi_T\pi_A\pi_Q\pi_E \qquad (Failures/10^6\ Hours) \tag{26}$$

$$\lambda_C = \lambda_b\pi_T\pi_C\pi_V\pi_{SR}\pi_Q\pi_E \qquad (Failures/10^6\ Hours) \tag{27}$$

$$\lambda_D = \lambda_b\pi_T\pi_S\pi_{CC}\pi_Q\pi_E \qquad (Failures/10^6\ Hours) \tag{28}$$

$$\lambda_L = \lambda_b\pi_T\pi_Q\pi_E \qquad (Failures/10^6\ Hours) \tag{29}$$

Where π_T is the temperature factor and is calculated as:

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TABLE I
RELIABILITY-RELATED PARAMETERS

	λ_b Base failure rate	π_A Application factor	π_Q Quality factor	π_E Environment factor	π_C Capacitance factor	π_V Voltage stress factor	π_{SR} Series resistance factor	π_S Electrical stress factor	π_{CC} Contact construction factor
MOSFET	0.012	10	2.4	6	-	-	-	-	-
Capacitor	0.00012	-	10	10	$C^{0.23}$ *	$\left(\frac{V_{op}}{0.6V_r}\right)^{10}+1$**	1	-	-
Diode	0.003	-	2.4	6	-	-	-	$\left(\frac{V_{op}}{V_r}\right)^{2.43}$**	2
Inductor	0.00003	-	3	6	-	-	-	-	-

* C = *Capacitance*
** V_{op} = *Operating Voltage*, V_r = *Rated Voltage*

TABLE II
SYSTEM PARAMETERS

Parameter	Comments	Value
P_n	Nominal power of each input port	1.2 [kW]
N_s	Number of independent PV strings	2
L_1,L_2	Input inductance of each boost converter	1 [mH]
C_a, C_b, C_c	Output filter capacitor	9 [uF]
L_a, L_b, L_c	Output filter inductor	220 [uH]
C_1,C_2	Input filter capacitor	9.4 [uF]
f_s	Switching frequency	18 [kHz]
V_g	Grid RMS phase voltage	220 [V]
f_g	Grid frequency	50 [Hz]
V_{pv}	PV input voltage	50 –200 [V]
$I_{pv\text{-}max}$	PV maximum input current per string	8 [A]

$$\pi_T = e^{\left(-K\left(\frac{1}{T+273}-\frac{1}{298}\right)\right)} \tag{30}$$

Where T is the junction temperature for semiconductor devices and the ambient temperature for capacitors. Also, K is a constant, which is equal to 1925, 4062, 3091 and 1276 for MOSFETs, capacitors, diodes and inductors, respectively. The other reliability-related parameters are explained in Table I. Based on MIL-HDBK-217F, a Ground-Fixed environment is selected and the quality and the environment factors are chosen. Moreover, it is assumed that the converter is working at the rated power which is the worst-case scenario for a PV inverter. The power losses are calculated for the rated power and based on the thermal resistance data (which are obtained from the datasheets), the junction temperatures are calculated. The components values and ratings used in the two-stage VSI are obtained from [38]. The parameters of the SSMPI topology are given in Table II.

The failure rate of the converter is found by adding the failure rates of all the components. Afterward, the Mean Time Between Failures (MTBF) is calculated as:

$$MTBF = \frac{1}{\sum_i \lambda_i} \tag{31}$$

With these assumptions, the failure rate of the two-stage VSI and the SSMPI are calculated equal to 28.94 and 22.28 $\frac{Failures}{10^6 hou}$, respectively. Considering that a PV inverter operates eight hours per day, the MTBF of the two-stage VSI and the SSMPI are obtained equal to 11.8 and 15.4 years, respectively. As it can be seen the lifetime of the SSMPI is 30% longer than the two-stage VSI.

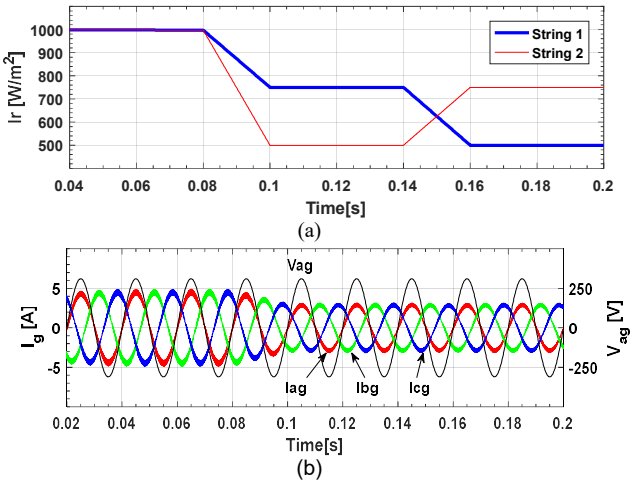

Fig. 5. (a) Simulated irradiance (I_r) profile for the two strings, (b) Simulated three-phase output currents and grid phase voltage.

VI. SIMULATION RESULTS

The SSMPI is simulated in MATLAB Simulink environment with the parameters as demonstrated in Table II. The adaptive perturb and observe method is used to find the Maximum Power Point (MPP) in both the simulation and the experimental tests. The existing model of REC220AE solar module in MATLAB Simulink 2016b is also used.

Two different irradiance profiles are used for the two strings. These profiles are illustrated in Fig. 5 (a). The three-phase grid currents and the grid phase voltages are shown in Fig. 5 (b). As it can be seen, the three-phase sinusoidal currents are injected to the grid with a unity power factor in different operating points. Therefore, by using the proposed control method, it is possible to control the output power factor without using ac current sensors. In the other words, the output currents are regulated directly by controlling the dc input current. The power of the two strings is depicted in Fig. 6. By comparing the extracted power and the maximum power of each string, it can be stated that with the proposed topology and control method the output power of each string can be controlled at its maximum available power, independently. Furthermore, the extracted power ripple in the steady-state conditions, is less than 5W.

The SSMPI operation at different Power Factors (PFs) and modulation indexes is also investigated. The simulation results are illustrated in Fig. 7. As it can be seen the SSMPI operates

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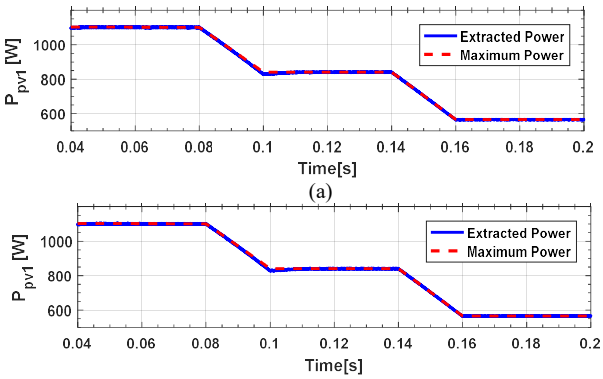

Fig. 6. Simulated power of PV strings (a) string 1, (b) string 2.

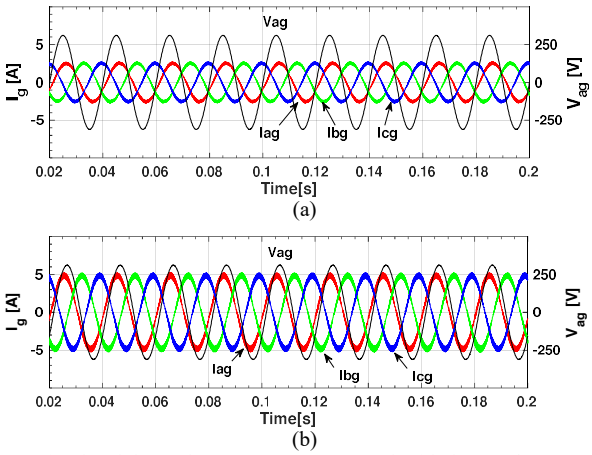

Fig. 7. Simulated three-phase output currents and grid phase voltage (a) PF = +0.9, $m_1 = m_2 = 0.305$, (b) PF = -0.9, $m_1 = m_2 = 0.345$.

at power factors of ±0.9 and different modulation indexes without any problem. It is also important to note that with the proposed switching scheme, it is necessary to have a positive link voltage all the times and as a result, the power factor of the SSMPI is limited to ±0.866.

VII. Experimental Results

A 2.4 kW prototype with the same parameters used in the simulations (as in Table II) was built to evaluate the performance of the SSMPI. The test setup is shown in Fig. 8. The SiC MOSFETs (SCT2080KE) and SiC diodes (SCS215AG) are used in the prototype. A STM32F407 microcontroller was used to implement the control and the Maximum Power Point Tracking (MPPT) algorithm. With respect to the implemented hardware limitations such as computational capability and number of analog to digital converter channels, it is possible to control up to 10 individual input ports. In the prototype, two individual PV strings are connected to the converter. Each string incorporates five REC220AE solar modules in series.

A. The SSMPI operation

In the first test, 2048 W is injected to the grid. The three-phase grid currents and the grid phase voltage are shown in Fig. 9. As it can be seen, the converter generates three-phase

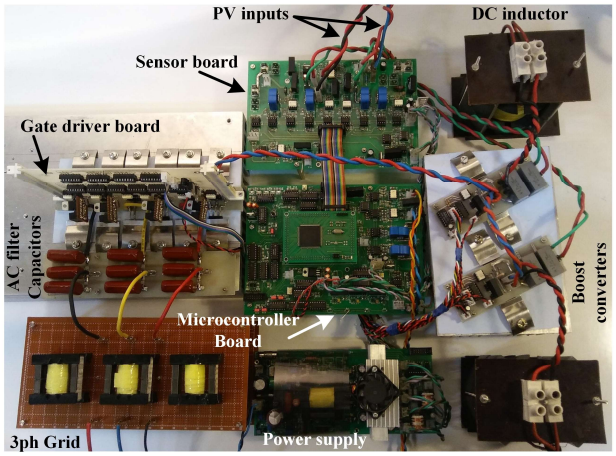

Fig. 8. Experimental test setup of the SSMPI.

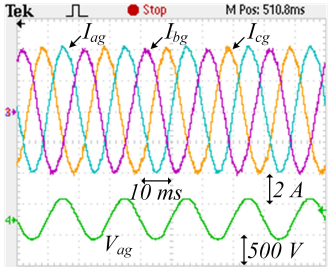

Fig. 9. Measured three phase grid currents and grid phase voltage.

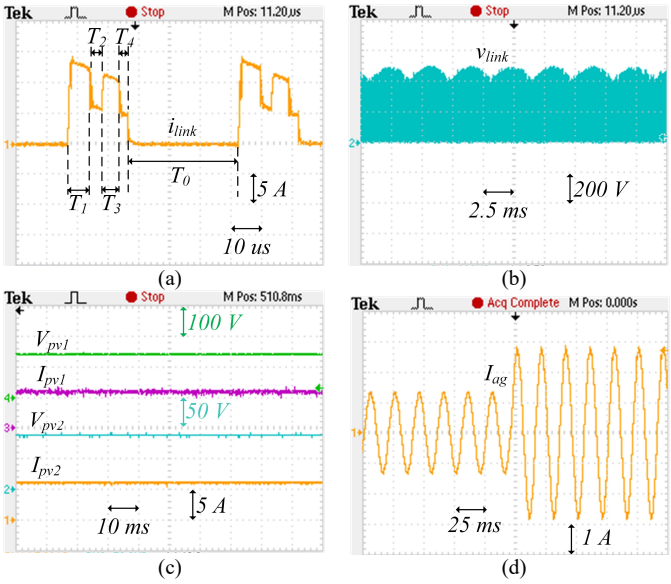

Fig. 10. (a) Measured link current, (b) Measured link voltage, (c) Measured voltage and current of the two strings, (d) Measured grid phase current during a step change of operating point.

sinusoidal balanced currents with a unity power factor without using any ac current sensors or intermediate dc link.

In the second test, the number of series PV modules connected to the second input is reduced from 5 to 3. By this test, the steady-state operation of the SSMPI interfacing with different PV strings is investigated. The link current (i_{link}) and voltage (v_{link}) are shown in Fig. 10 (a) and (b), respectively. The dwell time for different switching states is illustrated in Fig. 10 (a). As it can be seen four active switching states and

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TABLE III
MEASURED PARAMETERS OF THE MPP AND THE OPERATING POINT

Parameter	V_{MPP} [V]	V_{op} [V]	I_{MPP} [A]	I_{op} [A]	P_{MPP} [W]	P_{op} [W]
String 1	145.1	141	5.85	6	850	845
String 2	87.07	88	6.18	6	538	534

one zero state are used in each switching cycle. Fig. 10 (b) shows that no voltage spike exists in the link voltage waveform; which implies that a continuous current path is always provided by the switching algorithm. The current and the voltage of each string are shown in Fig. 10 (c). Using the data obtained from the oscilloscope, the average operating voltage (V_{op}), current (I_{op}) and power (P_{op}) of each string in a 100 ms time interval are calculated and reported in Table III. The MPP voltage (V_{mpp}), MPP current (I_{mpp}) and MPP power (P_{mpp}) for each string are also reported in this table. The MPPT efficiency of the SSMPI is calculated equal to 99.4% and 99.2% for the first and the second string, respectively.

In another scenario, the second string is disconnected from the converter initially. While the power is extracted from the first string, the second string is connected to the converter. By this way, a step change of operating point is implemented. It should be noted that each string contains five modules in series in this test. Using the voltage and current data, the output power of each string is calculated. The average extracted power from the first string is 692 W and it is 689 W for the second string. Also, the maximum available power is measured equal to 698 W and 695 W for the first and the second string, respectively. As it can be seen, the proposed SSMPI is able to extract maximum power from the two strings independently, with an MPP tracking efficiency higher than 99%. From this test, it can be concluded that even a step change in the operating point of the input ports, does not have any adverse effect on operation and control of the converter. The grid injected phase current when the second string is connected to the converter is also shown in Fig. 10 (d). As it can be seen, when the second string is connected the input power and the output power are doubled. Therefore, the output current is doubled without any problem. The peak phase current when operating only with the first string is 1.4 A and after connecting the second string it increases to 2.8 A. Furthermore, the new operating point is found and stabled in less than 10 ms.

B. *Efficiency and THD comparison*

The efficiency and the THD of the SSMPI versus the injected power to the grid are shown in Fig. 11. The maximum measured efficiency of the SSMPI is about 97.5% and the output current THD is less than 3.9% at different test conditions. The efficiencies of some other topologies are reported in Table IV. As it can be seen, by using SiC devices, eliminating the converter-side output filter inductors and intermediate dc link and utilizing a proper switching algorithm in the proposed topology, a high efficiency is reached. Also, the grid-side current THD is below the standard limit of 5%. Since no ac current sensors are used in the SSMPI, the grid current THD goes up as the grid voltage distortion increases. The simulation results show that under the grid voltage THD below 4.5%, the SSMPI output current THD will remain

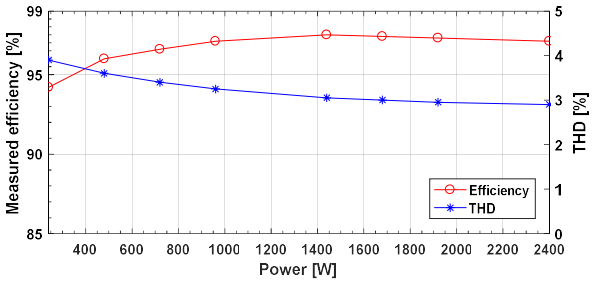

Fig. 11. Measured system efficiency and THD of the converter.

TABLE IV
PERFORMANCE COMPARISON WITH SOME OTHER RELATED TOPOLOGIES

Topology	Converter efficiency [%]	MPPT efficiency [%]	THD [%]
Multi-string two-stage single-phase VSI [4]	96.5	99.7	2
Multi-string two-stage single-phase thee-level VSI [6]	90	-	9.5
Multi-string two-stage single-phase five-level VSI [6]	86	-	5.7
Multi-string two-stage single-phase VSI [39]	81.77	-	2.31
Multi-string single-stage three-phase VSI with high-frequency link [8]	95.1	-	1.5
Current-fed dual active bridge with cascaded multi-level inverter [20]	-	99.5	1
Multi-string single stage single phase inverter [22]	-	96	-
Single-stage PV module integrated CSI [47]	97	-	4.5
Distributed flyback with a single-phase unfolding bridge [25]	90	99	4
Multi-input two-stage single-phase VSI (SB3000TL) [48]	97	-	-
Single-stage three-phase VSI with SiC devices [46]	98.8	-	-

below 5% at the rated output power. In comparison with the efficiency of single-stage three-phase VSI with SiC devices presented in [46], the SSMPI efficiency is 1.3% lower. But as discussed before, the VSIs have reliability issues due to the bulky electrolytic capacitors. The lower reliability decreases the availability of the PV power plant and the produced energy. Also, the single-stage VSIs have a lower performance in energy harvesting in comparison with multi-input inverters. Although, the SSMPI has no intermediate dc link or decoupling electrolytic capacitor, its MPPT efficiency is comparable with the two-stage multi-input VSIs.

VIII. CONCLUSION

A novel three-phase single-stage multi-port inverter suitable for grid-connected PV applications is presented in this paper. A single-stage energy conversion from solar arrays to the grid with boosting capability is provided by the SSMPI. Furthermore, The SSMPI needs just five filter inductors (with two input ports), while the conventional two-stage VSI with LCL filter needs eight inductors, at least. A control strategy is used in which the input ports are controlled individually and the maximum power is extracted in different operating conditions such as shading, interfacing with different PV

strings and etc. In addition, grid-side currents and output power factor are controlled without any ac current sensors or intermediate dc link. A new switching pattern is designed and the required switching times are calculated based on the SVM method. A novel circuit is used to implement the switching algorithm. The reliability of the SSMPI is improved by eliminating the electrolytic capacitors and its lifetime is 30% longer than the conventional two-stage VSI. The simulation results proved the performance of the SSMPI with the proposed switching method and the control procedure. The experimental results obtained on a 2.4 kW prototype show high performance such as high MPPT efficiency (99%), unity power factor operation, high power conversion efficiency (97.5%) and low current THD (3.9%).

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