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Analysis of the DC-Link Current for the Single Phase H-Bridge Inverter Under Harmonic Output Currents

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***Abstract*—This paper investigates the dc-link current to facilitate the dc-link capacitor sizing for the single phase H-bridge inverter under harmonic ac currents. As the capacitor equivalent series resistance (ESR) varies significantly until the frequency is higher than 1kHz, the expressions of the dc-link current individual low order harmonics (LOHs) and the switching harmonic currents (SHCs) root mean square (RMS) value are derived respectively to accurately evaluate the dc capacitor losses. The dc-link LOH expressions reveal that each harmonic ac current induces two harmonic currents in the dc-link. When the ac current has multiple combinations of LOHs, the dc-link current envelopes take infinite possible unusual forms, so after somewhat complicated derivation, the SHCs RMS equations are successfully derived and further simplified into one equation for easy worst case design as demonstrated by the actual case study. A single phase H-bridge inverter lab prototype is developed to inject arbitrary combinations of harmonic currents of different orders, amplitudes and angles into the grid. The good match between the computational, simulation and experimental results validate the effectiveness of proposed method. Particularly, the worst case analysis is verified by the experiment and the differences between the experiment and computation results are formulated and explained definitely.**

***Index Terms*—dc-link current, single phase H-bridge inverter, active power filter, low order harmonics, switching harmonic currents.**

I. Introduction

SIZING and rating of the capacitor is an important factor for the single phase H-bridge system design. Inaccurate evaluation of the dc-link current would result in capacitor oversizing and increase the system volume. It is well known that the dc-link current of the single phase inverter with the sinusoidal ac current contains a dc component, the 2nd order harmonic and switching harmonic currents (SHCs) with their sidebands components. The 2nd order harmonic current and the switching harmonic currents are absorbed by the dc capacitor. The dc voltage ripple is mostly determined by the low-order harmonic (LOH) currents in the dc-link, and the capacitor power losses are dependent on its equivalent series resistance (ESR) and harmonic currents in the dc-link.

A variety of dc-link current analytical methods, either in the time domain (RMS method) or in the frequency domain (Double Fourier Series Analysis method) have been reported in the literature [1]-[7]. The RMS current analytic solution is introduced in [1]-[5], where the dc-link current RMS value is expressed in terms of the modulation index, power factor, and the amplitude of output current. As the inverter output is a pulse width modulated (PWM) voltage, the output current also contains SHC ripples, whose impacts to the dc-link current RMS value are also investigated. Paper [1] and [3] derive the dc-link current RMS value expressions for the three phase and the single phase inverters, respectively. In both [1] and [3], output currents are sinusoidal. Paper [3] further evaluated the influence of the output current PWM switching harmonics (SHC ripples) on the dc-link current RMS value. Herein, the double Fourier analysis is used to get each spectral components of the switching harmonics and then it is concluded in [3] that the SHC ripples impacts can be neglected when they are less than 0.3 times of the fundamental output current. Paper [2] demonstrates that the SHC ripples have very limited influence on dc-link current by numerous simulations. Paper [4] and [5] directly derive the dc-link current RMS closed form expression. Paper [4] states that the SHC ripples in the output ac current will increase the dc-link current RMS essentially. By further exploration of the data in [4], it is clear that if the SHC ripple in the output current is neglected, the significant dc-link current RMS error only occurs when the ripple factor is much more than the normal allowable range (128.5%). The example of 24.8% error in [4] actually corresponds to a 128.5% ripple ratio. In a properly designed voltage source converter system, the SHC ripple factor at the converter side inductor has to be less than 20% or 30%. Therefore, the SHC ripples in the output current can be safely neglected when calculating the dc-link current RMS value.

As the capacitor ESR has strong frequency dependency, the dc-link current needs to be analyzed in the frequency domain

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[6]-[7] for more precise calculations of capacitor power losses. The three phase inverter dc-link current spectrum of CPWM (continuous PWM) and DPWM (discontinuous PWM) are compared by using double Fourier series method in [6]. Paper [7] proposes a general method to analyze the dc-link current spectra for most types of inverters, where it needs complicated convolution computation.

So far, nearly all the studies either with the Double Fourier Series Analysis or with the RMS method assume the sinusoidal ac current. Paper [8] investigates the dc-link current RMS expression with the unbalanced ac output current (negative sequence, still at the fundamental frequency) for three phase inverters. Therein, overall RMS values are obtained by integrating the dc-link current expression within each switching cycle over one sector, and the dc-link low order harmonic (LOH) current is obtained in the same process. When the ac current contains multiple LOHs (less than 1kHz) in applications such as the active power filter (APF), the significant impacts of the LOHs on the dc-link current are investigated in [9]. Therein, the LOHs and SHC RMS of the dc-link current are formulated individually, as the ESRs of the electrolytic and film dc capacitors nearly stay constant when harmonic frequencies greater than 1kHz [10]-[12].

It should also be noted that the previous methods all suffer from a serious difficulty in the practical worst case design, i.e. there are infinite possible RMS values due to all possible LOH phase angles combinations. To be more specific, even if the previous methods such as the double Fourier Series analysis would be used to handle the cases with the LOHs, it would still only get one solution with one set of LOH phase angle combination after intensive computation. So it would not be practical to get the worst case design result for the dc-link current.

This paper extended the work of [9], giving more detailed investigation of the dc-link current for single phase H-bridge converter under harmonic ac currents. Herein, the SHCs RMS equations are successfully simplified into one equation for easy worst case design, and a practical design case of the dc-link harmonic currents is demonstrated. In Section II, the basic models of the inverter dc-link current and duty cycles are introduced together with the capacitor power losses model. Then the general expressions of dc-link LOHs are derived based on instant power balance in Section III. Each dc-link LOH current is used separately to calculate the capacitor losses, as the capacitor ESR varies with the frequencies under 1kHz. In Section IV, it is revealed that the conventional SHC RMS equation derivation process is no longer applicable when the ac current has the LOHs. Hence, new SHC RMS equations were derived with trigonometric derivation. As a given set of LOHs in the ac current have phase angles with full ranges, infinite dc-link current envelopes and the corresponding RMS values exist. Therefore, the proposed equations are simplified for the worst case design and then demonstrated with quantitative examples in Section V. Section VI shows a single-phase H-bridge inverter prototype developed to inject different combinations of LOH currents into the grid. Despite the unusual and complicated dc-link current patterns under various combinations of LOHs, the lab results well match those from the proposed computational methods and the simulations. Particularly, the worst case analysis is verified by the experiment and the differences between the experiment and computation results are formulated and explained definitely.

II. Basic Analysis Of The DC-Link Current

A. Circuit Description

The single phase H-bridge inverter topology is depicted in Fig. 1. C_{dc} is the dc capacitor, R_{dc} and L_{dc} are the stray resistance and inductance of the dc source. $\underline{V_{dc}}$ is dc source voltage. The dc-link voltage v_c is inverted into the PWM voltage v_{out} by the H-bridge. The switching frequency ripple currents in the output is absorbed by the LC or LCL filter between the inverter and the grid (or loads). L_g and L_r are the filter inductors on the grid and the inverter side, respectively. C_f is the filter capacitor and R_d is a damping resistor.

Considering that i_{aT} and i_{bT} are the two phase leg currents, the dc-link current can be expressed as

$$i_{dc} = i_{aT} + i_{bT} = \left(S_a - S_b\right) i_{out} \tag{1}$$

where S_a and S_b are the switching states. When T_{i1} is on or off, S_i (i=a,b) equals to 1 or 0, respectively. It should be noted that the dc-link current model as in (1) defines the relationship between the switching function and the output current. Even though (1) is not used for calculating the LOH currents in dc-link, it is needed to derive the dc-link current RMS in Section IV.

B. PWM Strategy and Modulation Signals Analysis

The gating signals for the system as shown in Fig. 1 is generated by the carrier-based PWM [13]-[15] which could be either bipolar or unipolar modulation. Since the unipolar modulation has lower voltage steps and less SHC ripples in the ac side, it has been chosen as the modulation method for single phase inverters [16]. Therefore, the unipolar modulation is used in this paper. The LOHs are often present in its modulation signals. When the grid voltage has LOHs distortion, a properly designed closed loop controller of a grid-tied inverter produces the same amount of voltage harmonics, so that the grid current stays sinusoidal [17]. In APF, additional LOHs is needed in modulation signals to inject harmonic currents. In UPS applications, the LOHs are also needed in modulation signals in order to maintain sinusoidal voltage under nonlinear loads. Therefore, the general mathematical expressions of the modulation signals v_{aM} and v_{bM} for phase leg a and b as defined in (2) should consist of the fundamental frequency and multiple LOH signals.

$$\begin{cases} v_{aM} = \sum_{k=1} M_k \cos\left(k\omega_1 t - \varphi_{vk}\right) + v_z \\ v_{bM} = -\sum_{k=1} M_k \cos\left(k\omega_1 t - \varphi_{vk}\right) + v_z \end{cases} \tag{2}$$

In (2), $\omega_1 t$ is the phase angle of fundamental component in v_{out}. φ_{v1} is the slight phase angle difference between the inverter and the grid side voltages (or UPS output voltage) to induce the needed current output. v_z is common mode modulation signals. In unipolar SPWM of single phase inverter [18], v_z is zero. The M_k is the modulation index defined as

$$M_k = \frac{V_k}{v_c} \tag{3}$$

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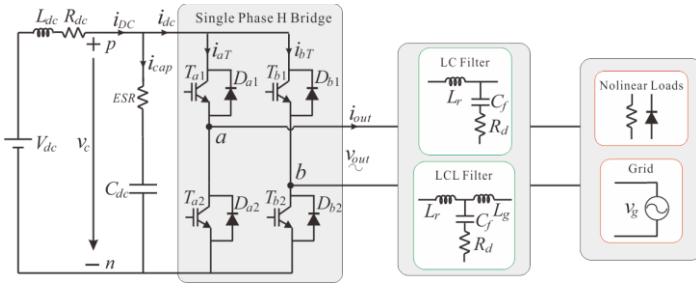

Fig. 1 Single phase H-bridge inverter topology.

where V_k is the magnitude of k^{th} voltage harmonic component in modulation signals.

C. Simplification of the Modulation Signals Expressions

Two simplifications are made to the modulation signal expressions as in (2) in the subsequent derivation process.

Firstly, the LOH signals are negligible compared to the fundamental frequency signal. As for the inverter filter inductor voltage drops, there are design rules such as in [19]-[20], where it is defined that a regular grid tied inverter allows the inductance voltage drop (at fundamental frequency) less than 10%. Therefore, only slight voltage difference between the inverter output and the grid voltage is needed to induce the rated grid-side current over the filter inductor. The same rule is also applicable in an APF system, where the fundamental frequency component of the inverter output voltage is the same as the grid voltage, and then only small amount of extra harmonic voltages from the inverter output (also <10% of the fundamental component) are needed to induce the required APF LOH currents across the filter inductor.

Secondly, the slight phase angle difference φ_{v1} between the inverter output and the grid voltage can be neglected. Fig. 2 shows the fundamental frequency voltage phasor diagram where v_L, v_{out} are the inductor voltage and inverter output voltage, respectively. The grid current i_g leads the grid voltage v_g *by* φ_1, which indicates that the inverter is also adding capacitive reactive powers to the system. It is obvious from Fig. 2 that as the inductor voltage drop is very small, the phase angle difference between grid and inverter output voltage is negligible in the subsequent derivation process. Particularly for the APF application in this paper, fundamental frequency grid current is zero, so that the two voltages are actually the same with zero φ_{v1}.

D. Capacitor Power Losses

The lifetime of capacitors follows the well-established "10 Kelvin rule": a drop of the ambient temperature by 10K doubles the lifetime. Therefore, in addition of selecting an appropriate rated voltage of the capacitor, the correct thermal design is of major importance. The capacitor core temperature T_c is determined by the ambient temperature T_a and the power dissipation in the capacitor, as caused by the capacitor RMS current [2].

$$T_c = T_a + I_{C,rms}^2 R_{ESR} R_{th,c-a} \tag{4}$$

where R_{ESR} represents the equivalent series resistance (ESR) of the capacitor, $R_{th,c-a}$ is the thermal resistance between the capacitor core and ambient air, and $I_{C,rms}$ is the capacitor current RMS value. A typical ESR vs. frequency curve is shown in Fig. 3. It should be noted that the capacitor ESR stays almost

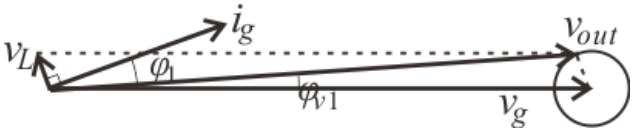

Fig. 2 The fundamental frequency components phasor diagram on the inverter ac side.

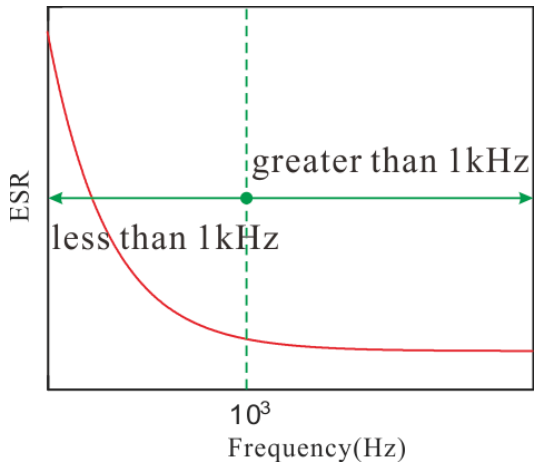

Fig. 3 Typical capacitor ESR frequency characteristic curve.

constant with the frequencies greater than 1kHz and varies greatly at the frequencies below 1kHz. Therefore, it is proposed herein that the capacitor power dissipation is computed with

$$I_{C,rms}^2 R_{ESR} = \sum_{f=f_1}^{1kHz} I_{C,rms}^2(f) R_{ESR}(f) + I_{C,rms,f>1kHz}^2 R_{ESR,f>1kHz} \tag{5}$$

where the first term and second term in (5) represent the power losses caused by the individual LOH currents and overall SHC RMS value in the dc-link, respectively.

III. DC-Link Current Low Order Harmonics Computation Methods

A straightforward instant power based computational method is proposed in this paper to analyze the dc-link LOH currents.

Firstly, compared to the fundamental frequency and switching harmonic voltages (v_{sw_harm}), the LOH voltages are negligible as explained in section II. Then the output voltage of inverter is written as

$$v_{out} = v_c M_1 \cos(\omega_1 t) + v_{sw\_harm} \tag{6}$$

Secondly, unlike the voltages, the LOHs in the ac current are the dominant components in applications like APF. Instead, current ripples (SHCs) are negligible in the ac current expression, which is defined as

$$i_{out} = \sum_{k=1} I_k \cos(k\omega_1 t - \varphi_k) \tag{7}$$

where I_k and φ_k are the magnitude and initial phase angle of k^{th} harmonic current, respectively. Then the instantaneous power on the inverter ac side is obtained by multiplying (6) with (7),

$$p_{ac} = \frac{v_c M_1}{2} \sum_{k=1} I_k \begin{bmatrix} \cos((k-1)\omega_1 t - \varphi_k) \\ +\cos((k+1)\omega_1 t - \varphi_k) \end{bmatrix} + v_{sw\_harm} i_{out} \tag{8}$$

The dc side instantaneous power could be seen as equal to (8) without considering power losses of the inverter. Hence, by dividing v_c from (8), the dc-link current is expressed as:

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$$i_{dc}=\frac{M_1}{2}\sum_{k=1}I_k\begin{bmatrix}\cos\left((k-1)\omega_1 t-\varphi_k\right)\\+\cos\left((k+1)\omega_1 t-\varphi_k\right)\end{bmatrix}+\frac{v_{sw\_harm}}{v_c}i_{out} \quad (9)$$

The two terms in (9) represent two parts in the dc-link current, i.e. the LOHs and SHCs. The SHCs in the dc-link current are to be derived in detail in the subsequent section. The expression of the LOHs in dc-link current is defined as

$$i_{dc\_low}=\frac{M_1}{2}\sum_{k=1}I_k\begin{bmatrix}\cos\left((k-1)\omega_1 t-\varphi_k\right)\\+\cos\left((k+1)\omega_1 t-\varphi_k\right)\end{bmatrix} \quad (10)$$

When the inverter design requirements are given, such as a single phase APF with a full set of the major harmonic currents to cancel, the worst case dc-link LOH currents can be readily obtained from (10) for each LOH in the ac current. Equation (10) also reveals the fact that the k^{th} harmonic in ac current induces both the $(k\text{-}1)^{th}$ and $(k\text{+}1)^{th}$ harmonic currents in the dc-link. Using the ac current with the 1st, 5th, 8th harmonics to exemplify, the 0th, 2nd, 4th, 6th, 7th, 9th harmonic currents are present in the dc-link. It is also instructive to note that if two ac current harmonics (k_1^{th} and k_2^{th}) satisfy k_1-k_2=2 and $|\varphi_{k1}-\varphi_{k2}|=\pi$, the corresponding $(k_1\text{-}1)^{th}$ and $(k_2\text{+}1)^{th}$ harmonic currents in the dc-link would cancel each other; if k_1-k_2=2 and $\varphi_{k1}=\varphi_{k2}$, the two harmonic currents in the dc-link would reinforce each other. Herein, the average dc current expression is obtained by setting k as 1 in (10).

$$I_{dc\_avg}=\frac{M_1 I_1}{2}\cos(\varphi_1) \quad (11)$$

From (10), the dc-link LOH currents RMS value (including the average dc value) could be derived as

$$I_{dc\_lowRMS}=\frac{M_1}{2}\sqrt{\begin{matrix}\left(I_1\cos(\varphi_1)\right)^2+\left(\frac{I_1}{\sqrt{2}}\right)^2+\sum_{k=2}\left(I_k\right)^2\\+\sum_{\substack{k1,k2\\k1-k2=2}}I_{k1}I_{k2}\cos\left(\varphi_{k1}-\varphi_{k2}\right)\end{matrix}} \quad (12)$$

Even though (12) is not suitable for calculating capacitor losses, it is needed to derive the dc-link SHC RMS as in Section IV.

IV. RMS Equations Of The Switching Harmonic Currents In The DC-Link Under Low Order Harmonics In AC Currents

There are 4 switching states in a single phase H bridge inverter. The dc-link current per switching state as in (1) is shown in Table I. Fig. 4 depicts the dc-link current waveform over one switching period with the unipolar modulation. The v_{tri} is the carrier signals, d_a and d_b are the duty cycle of T_{a1} and T_{b1}. The dc-link current RMS square in one switching period T_{sw} is expressed as

$$i_{dc\_RMS}^2=\frac{1}{T_{sw}}\int_{t_0}^{t_0+T_{sw}}i_{dc}^2dt \quad (13)$$

where t_0 is the initial time. From Table I and Fig. 4, equation (13) can be rewritten as

$$i_{dc\_RMS}^2=\left|d_a-d_b\right|i_{out}^2 \quad (14)$$

The duty cycles d_a and d_b are defined as

$$\begin{cases}d_a=\frac{1}{2}\left(v_{aM}+1\right)\\d_b=\frac{1}{2}\left(v_{bM}+1\right)\end{cases} \quad (15)$$

Thus the overall dc-link current RMS is obtained by integrating over one fundamental cycle as

$$I_{dc\_RMS}=\sqrt{\frac{1}{2\pi}\int_{\theta_0}^{\theta_0+2\pi}i_{dc\_RMS}^2d\omega_1 t} \quad (16)$$

where θ_0 is the start position of integration.

When the ac current is sinusoidal, it is well known that the envelope of the dc-link current is cyclic with a period of π (as shown in Fig. 5(a). From (16), the RMS value could be derived as

$$I_{dc\_RMS}=\sqrt{\frac{1}{\pi}\int_{-\pi/2}^{\pi/2}\left(d_a-d_b\right)i_{out}^2d\omega_1 t} \quad (17)$$

where the result includes contributions from the dc, 2nd order harmonic and SHCs.

When the ac current has multiple LOHs, the envelopes of the dc-link current are quite different as illustrated in Fig. (5b) and (5c) where the ac current contains the 2nd or 4th harmonics. Their repetitive periods are 2π. Although even harmonics are rare in modern applications, it does exist in some legacy applications that require simplicity and reliability such as nuclear power plant auxiliary power supplies, which use single phase ac power even with power level higher than 100kW. Here, large even harmonics need to be absorbed by APF when there are loads with half-wave rectifier front-end. The even harmonics are also discussed in [21].

Considering all possible LOH combinations in the ac current, the dc-link current RMS expression for each switching cycle varies in 3 segments within a complete fundamental cycle. By substituting (14) into (16), the dc-link current RMS value is expressed as

$$I_{dc\_RMS}^2=\frac{1}{2\pi}\times\begin{bmatrix}\int_{-\pi/2}^{\pi/2}\left(d_a-d_b\right)i_{out}^2d\omega_1 t\\+\int_{-\pi}^{-\pi/2}\left(d_b-d_a\right)i_{out}^2d\omega_1 t\\+\int_{\pi/2}^{\pi}\left(d_b-d_a\right)i_{out}^2d\omega_1 t\end{bmatrix} \quad (18)$$

By combining (2), (7), (15), and (18), after somewhat lengthy derivation process, the dc current RMS expression is formulated as (19)-(21). The RMS result as in (19) has two parts, which is further defined by (20) and (21).

$$I_{dc\_RMS}=\sqrt{\sum_k I_{dc\_kRMS}^2+\sum_{k1,k2}I_{dc\_k1k2RMS}^2} \quad (19)$$

The first part of (19) stems from the k^{th} harmonic (low order) in the ac current as defined by

$$I_{dc\_kRMS}^2=\frac{M_1 I_k^2}{\pi}\left[1-\frac{(-1)^k\cos(2\varphi_k)}{4k^2-1}\right] \quad (20)$$

The second part of (19) stems from any two LOHs (k_1^{th} and k_2^{th}) in the ac current as defined by

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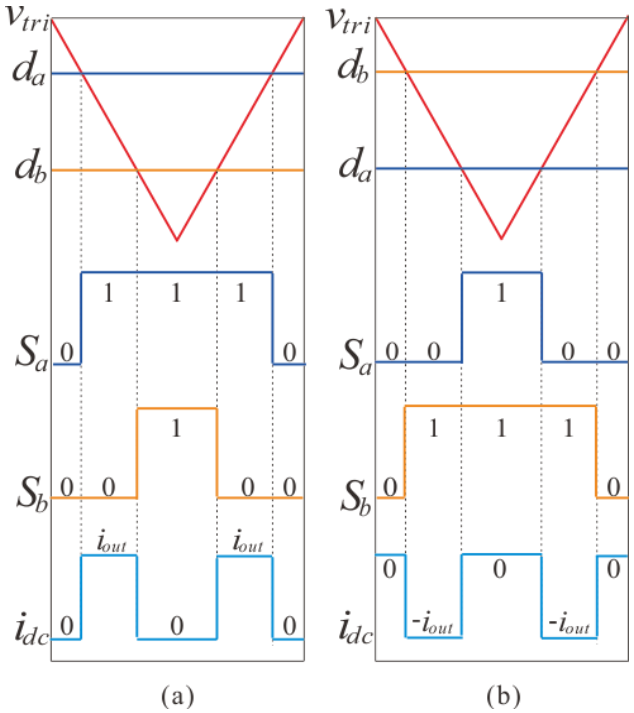

Fig. 4 The switching function and dc-link current waveforms over one switching period when (a) $d_a>d_b$; (b) $d_a<d_b$.

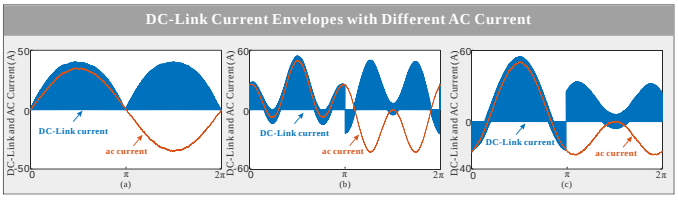

Fig. 5 The dc-link current waveforms at M_1=0.8 when the ac current contains harmonics of: (a) I_1=35A, φ_1=0; (b) I_1=I_2=25A, φ_1= φ_2=0; (c) I_1=I_4=25, φ_1= φ_4=0.

TABLE I
THE DC-LINK CURRENT IN TERMS OF AC CURRENT AND SWITCHING STATES

S_a	S_b	i_{dc}
1	1	0
1	0	i_{out}
0	1	$-i_{out}$
0	0	0

$$I_{dc\_k1k2RMS}^2 = -\frac{2M_1 I_{k1} I_{k2}}{\pi} \times \left[\frac{\cos(\varphi_{k1}+\varphi_{k2})}{(k_1+k_2)^2-1} \cos\left((k_1+k_2)\frac{\pi}{2}\right) + \frac{\cos(\varphi_{k1}-\varphi_{k2})}{(k_1-k_2)^2-1} \cos\left((k_1-k_2)\frac{\pi}{2}\right) \right] \quad (21)$$

Therefore, by eliminating the dc-link LOH currents RMS value as defined in (12), the SHC RMS in the dc-link could be obtained as

$$I_{dc\_switchRMS} = \sqrt{I_{dc\_RMS}^2 - I_{dc\_lowRMS}^2} \quad (22)$$

The equations (19)-(22) could be simplified significantly when applied to the special cases, such as the grid-tied inverter with only the fundamental component in the ac current. By setting k=1 in (22), the resulting dc-link SHC RMS expression as in (23) exactly matches (13) in [3].

$$I_{dc\_switchRMS} = I_1 \sqrt{\frac{M_1}{24\pi}\left[24+(8-3\pi M_1)\cos(2\varphi_1)-6\pi M_1\right]} \quad (23)$$

V. WORST CASE DESIGN OF THE DC-LINK CURRENTS

In practical design, the worst cases for both the SHC RMS value and individual LOH currents are needed for the capacitor losses and rating computation.

A. Simplified SHC RMS Value Equations for the Worst Case Design

It is impractical to obtain the dc-link SHC RMS maximum value by directly using the complete equation set (12), (19)-(22), as it would need to traverse the full ranges of the phase angles of each individual LOH currents, rendering infinite possible RMS values. Even though this repetitive computational practice (using MATLAB) is more advantageous than the old ways of running numerous simulation cases, it is still time consuming and not convenient for design purposes. For example, assuming the iterations of each LOH phase angle range is 628 (with the 0.01 radian phase angle interval), the total iteration number become 628^3 when the ac currents have 3 LOH currents. Therefore, some simplifications are needed to facilitate the design practice.

Firstly, it is discovered that most of the phase angle dependent terms in (19)-(21) are negligible due to their overwhelmingly large denominators, except for the cases when k=1 in (20) and k_1-k_2=2 in (21). Therefore, the overall RMS values of the dc-link current could be simplified as

$$I_{dc\_RMS} = \sqrt{\frac{M_1}{\pi}\left[\sum_{k=1} I_k^2 + \frac{I_1^2\cos(2\varphi_1)}{3}\right] + \frac{2M_1}{3\pi}\sum_{k_1-k_2=2}\left[I_{k1}I_{k2}\cos(\varphi_{k1}-\varphi_{k2})\right]} \quad (24)$$

Then by removing the RMS values of the LOHs and the dc average value as in (12), the simplified RMS expression of the dc-link SHC could be obtained as

$$I_{dc\_switchRMS} = \sqrt{\left(\frac{2M_1}{3\pi}-\frac{M_1^2}{8}\right)I_1^2 + \left(\frac{M_1}{\pi}-\frac{M_1^2}{4}\right)\sum_{k=2} I_k^2 - \left(\frac{M_1^2}{4}-\frac{2M_1}{3\pi}\right)\left(I_1\cos(\varphi_1)\right)^2 - \left(\frac{M_1^2}{4}-\frac{2M_1}{3\pi}\right)\sum_{k1-k2=2} I_{k1}I_{k2}\cos(\varphi_{k1}-\varphi_{k2})} \quad (25)$$

Apparently, once the M-index or dc voltage is given, the maximum $I_{dc\_switchRMS}$ is obtained if the third term in (25) satisfies φ_1=0 (0<M_1<0.85) or φ_1=π/2 (0.85<M_1<1) and the fourth term in (25) satisfies φ_{k1}=φ_{k2} (0<M_1<0.85) or $|\varphi_{k1}$-$\varphi_{k2}|$=π (0.85<M_1<1). Hence the maximum $I_{dc\_switchRMS}$ expression is

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$$I_{dc\_maxswitchRMS}=\sqrt{\left(\frac{2M_1}{3\pi}-\frac{M_1^2}{8}\right)I_1^2+\left(\frac{M_1}{\pi}-\frac{M_1^2}{4}\right)\sum_{k=2}I_k^2+\begin{cases}\left|\frac{M_1^2}{4}-\frac{2M_1}{3\pi}\right|I_1^2 & if\ 0<M_1<0.85\\ 0 & if\ 0.85<M_1<1\end{cases}+\left|\frac{M_1^2}{4}-\frac{2M_1}{3\pi}\right|\sum_{k1-k2=2}I_{k1}I_{k2}} \tag{26}$$

Equation (26) is a handy tool for the dc-link design cases that has many harmonics on the ac side such as the 3rd, 5th, 7th, 11th, 13th, …etc. By comparison, it would be almost impossible for the spectral analysis or RMS equations in prior art to obtain the worst case results out of infinite dc-link current envelopes as the LOHs phase angles vary within their full ranges.

B. Worst Case for Individual LOH Current Values

The dc-link LOH currents are the other design factor for the capacitor sizing. It is clear to see from (10) that each ac side LOH current induces two LOH currents in the dc-link as in Fig. 6. When the ac current consists of k_1th and k_2th harmonics (k_1-k_2=2), two dc-link LOH currents will have the same frequency, and their vector sum amplitude varies with the combinations of the LOHs phase angles. The worst case is when they add up as in Fig. 6(b) and as expressed in Table II. Other than the scenario when the ac side k_1th and k_2th harmonics (k_1-k_2=2) co-exist, the individual LOH values are fixed with their amplitude, so there is no worst case.

C. Overall Worst Case with both SHC and LOH Currents

It can be seen from (5) that the overall worst case for capacitor losses and sizing considers both the SHC RMS value and LOH currents. Table III summaries the worst cases of both the SHC RMS value and LOH currents, throughout the full M-index range. Only when the ac side k_1th and k_2th harmonics (k_1-k_2=2) co-exist, the varying terms as in Table III are non-zero and vary with the LOHs phase angles, so that the overall worst case is obtained with certain phase angles combinations.

From Table III, it is seen that the SHC RMS value and LOH currents could reach their maximum at the same time when the M-index is from 0 to 0.85, so that the worst case here is clear cut. However, as for the M-index between 0.85 and 1, if the SHC RMS value reaches its maximum, the LOH currents are at the minimum, and vice versa. In this scenario, the worst case is obtained by comparing the varying terms listed in Table III for SHC RMS and LOH currents.

$$\begin{cases}I_{SHC\_Vary1}=\left(-\frac{M_1^2}{4}+\frac{2M_1}{3\pi}\right)\sum_{k1-k2=2}\left(I_{k1}I_{k2}\cos\left(\varphi_{k1}-\varphi_{k2}\right)\right)\\ I_{LOH\_Vary2}=\frac{M_1^2}{8}\sum_{k_1-k_2=2}\left(I_{k1}^2+I_{k2}^2+2I_{k1}I_{k2}\cos\left(\varphi_{k1}-\varphi_{k2}\right)\right)\end{cases} \tag{27}$$

As for the M-index between 0.85 and 1, as illustrated in Fig. 7, it is clear that the varying terms of the LOH currents is larger than that of the SHC RMS value. Moreover, the ESR value for frequencies below 1kHz is greater than its value at switching frequencies. Therefore, the LOH currents contribute more to the capacitor power losses than the SHC RMS value with $0.85<M_1<1$. Fig. 8 gives the flow chart of the worst case design for the capacitor power losses.

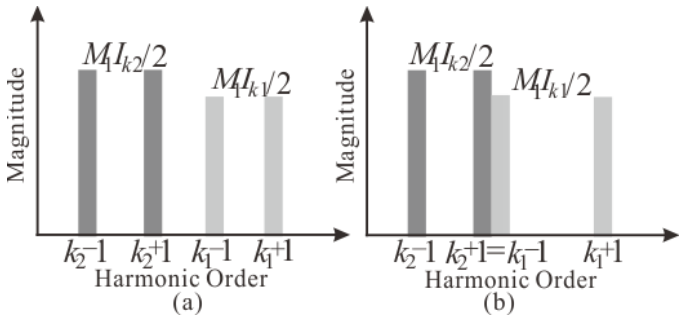

Fig. 6 The typical dc-link LOH currents spectrum when the ac current has k_1th and k_2th harmonics: (a) $k_2+1\neq k_1-1$; (b) $k_2+1=k_1-1$.

TABLE II
SUM OF TWO DC-LINK LOH CURRENTS WITH THE SAME FREQUENCY (k_1-1 = k_2+1)

dc-link LOH Current RMS	Maximum Value
$\frac{M_1}{4}\sqrt{2\left(I_{k1}^2+I_{k2}^2+2I_{k1}I_{k2}\cos\left(\varphi_{k1}-\varphi_{k2}\right)\right)}$	$\frac{\sqrt{2}M_1}{4}\left(I_{k1}+I_{k2}\right)$

D. Practical Design Case Study

In the following quantitative design case of an APF, the proposed complete equations and their simplified forms are applied to compute the dc-link current. The grid voltage is 220VRMS and the requirements of the maximum LOHs in the ac current are I_3=50A, I_5=30A. Here, two dc voltages (320V and 400V) are used to exemplify two cases with different M-indexes (0.78 and 0.97). The worst case LOH currents (when $\varphi_3=\varphi_5$) are computed and listed in Table IV.

Next, the dc-link SHC RMS values are calculated by the complete equations set (19)-(22) and its simplified form (25). For comparison, they are plotted in Fig. 9 side by side for the full ranges of phase angles (φ_3 and φ_5) of the given 3rd and 5th harmonics. In both Fig. 9(a) and Fig. 9(b), it is clear to see that the error percentages don't exceed 8%. So that equation (25) and its variant (26) are efficient for obtaining the RMS value of the dc-link SHC and its maximum value out of all possible phase angles of the LOHs in the ac current with given amplitudes.

As explained in the subsection C of Section V, as the M-index 0.78 is within [0, 0.85], the worst cases for SHC RMS value (18.6A) and LOH currents both occur with the same LOHs phase angle combination; as the M-index 0.97 is within [0.85, 1], the phase angle combination with the worst case LOH currents brings up the worst case for the overall capacitor power losses, even it corresponds to the minimum SHC RMS value (14.4A).

In practical design, the manufacture datasheet does not usually give the ESR values for the desired temperature conditions. For this design case study, 60 °C is assumed as ambient temperature inside the cabinet and the electrolytic capacitor B43504 series (TDK EPCOS) is used. The dc capacitor bank is designed with 800V peak rating by using two 400V-RATED b43504c9277M0 capacitors in series and 16 branches in parallel. Herein, the data sheet only provides the

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TABLE III
THE CONDITIONS FOR THE SHC RMS AND EACH LOH CURRENT RMS REACH THEIR MAXIMUM VALUES

Category	Modulation Index	Worst Case Angle Combo	The Varying Term
SHC RMS	$0<M_1<0.85$	$\varphi_1=0$, $\varphi_{k1}=\varphi_{k2}$	$\left(-\frac{M_1^2}{4}+\frac{2M_1}{3\pi}\right)\sum_{k1-k2=2} I_{k1}I_{k2}\cos(\varphi_{k1}-\varphi_{k2})$
	$0.85<M_1<1$	$\varphi_1=\pi/2$, $\lvert\varphi_{k1}-\varphi_{k2}\rvert=\pi$	
LOH currents	$0<M_1<1$	$\varphi_{k1}=\varphi_{k2}$	$\frac{M_1^2}{8}\sum_{k_1-k_2=2}\left(I_{k1}^2+I_{k2}^2+2I_{k1}I_{k2}\cos(\varphi_{k1}-\varphi_{k2})\right)$

TABLE IV
SUMMARY SHEET OF THE PRACTICAL DESIGN CASES

Frequency (Hz)		100	200	300	>1000
Single Capacitor Normalized ESR ($ESR_f/ESR_{100Hz\_60°C}$)		1	0.69	0.56	0.38
Capacitor Bank Normalized ESR ($ESR_f/ESR_{100Hz\_60°C}$)×(2/16)		0.13	0.09	0.07	0.05
M_1=0.78	LOH Currents (RMS) (A)	13.8	22.1	8.3	/
	SHC RMS (A)	/	/	/	18.6
	Normalized Capacitor Bank Loss (I_f^2×($ESR_f/ESR_{100Hz\_60°C}$)×(2/16))	24.76	43.96	4.82	17.30
	Total Normalized Capacitor Bank Loss	90.84			
M_1=0.97	LOH Currents (RMS) (A)	17.2	27.5	10.3	/
	SHC RMS (A)	/	/	/	14.4 (minimum)
	Normalized Capacitor Bank Loss (I_f^2×($ESR_f/ESR_{100Hz\_60°C}$)×(2/16))	38.46	68.06	7.43	10.39
	Total Normalized Capacitor Bank Loss	124.34			

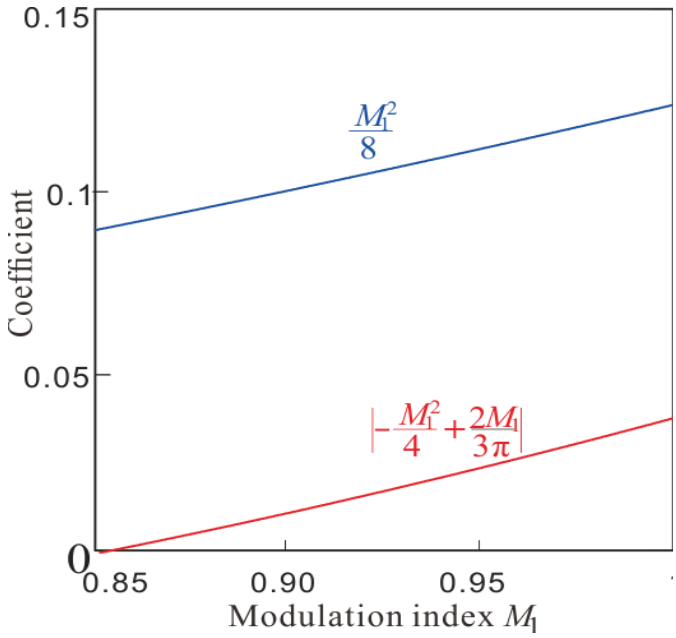

Fig. 7 Comparison of M-index related coefficients for the varying terms.

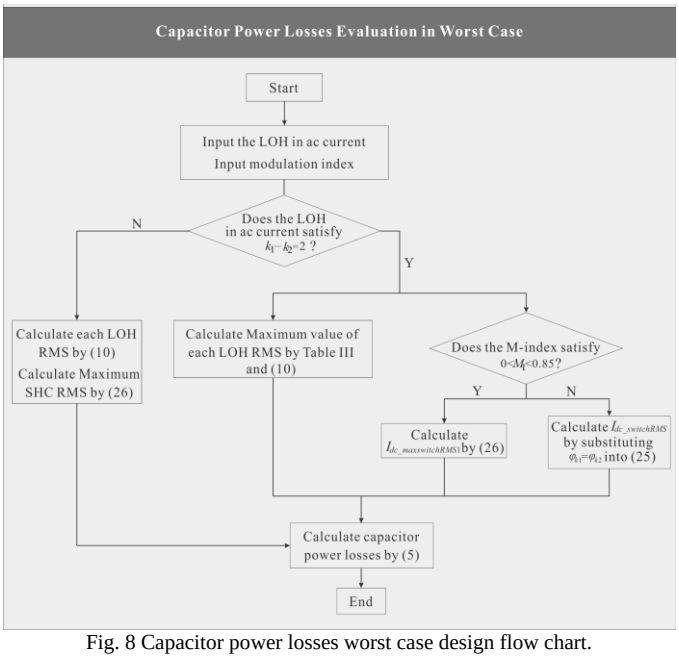

Fig. 8 Capacitor power losses worst case design flow chart.

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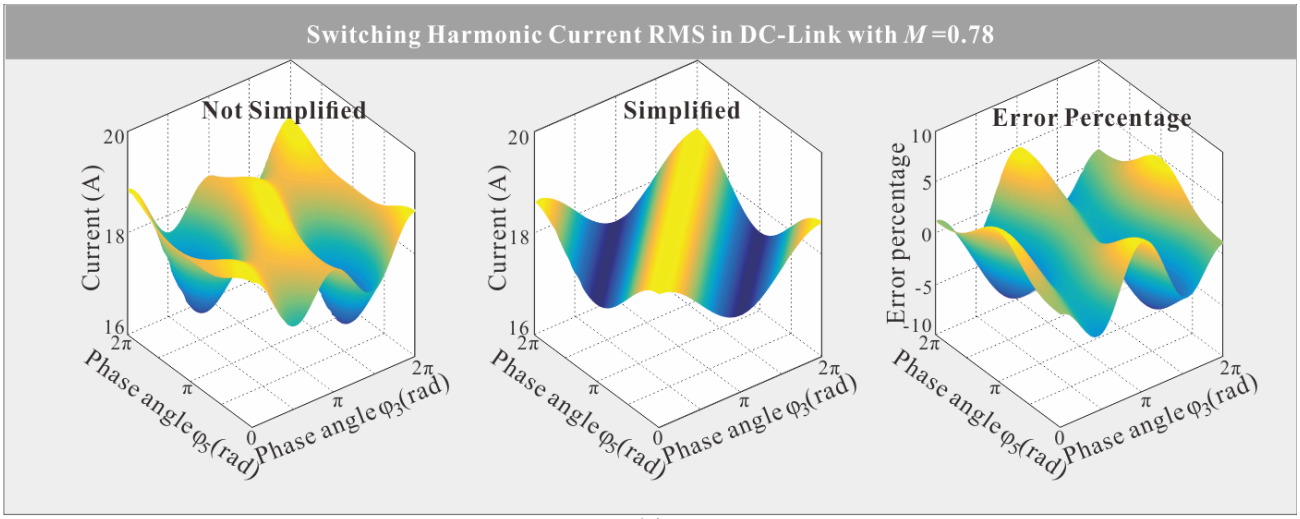
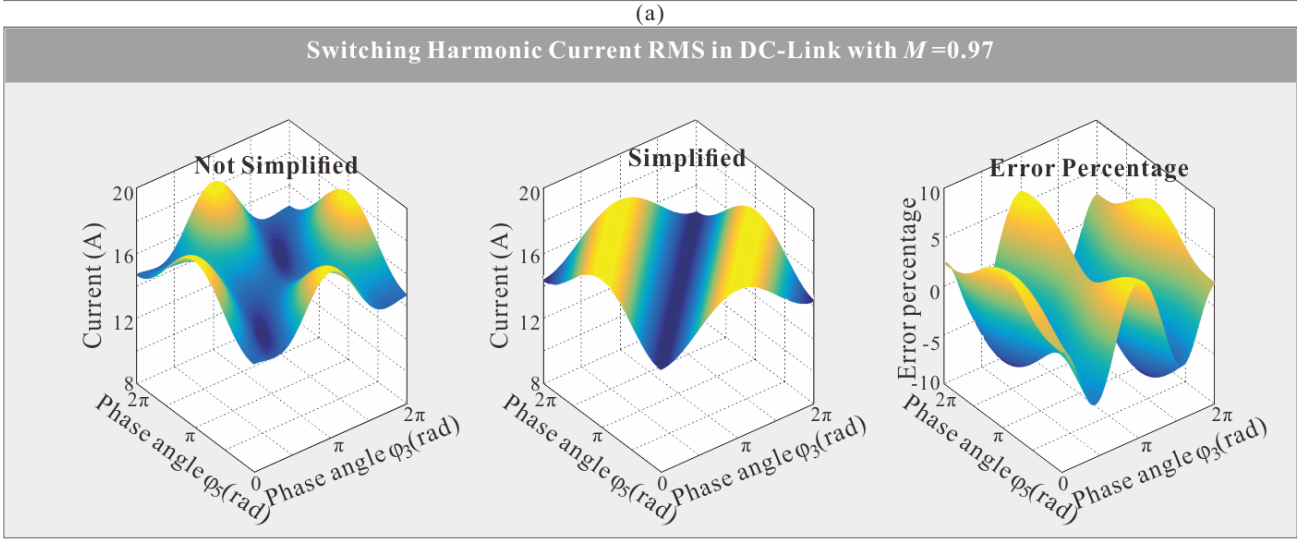


(a)



(b)

Fig. 9 The SHC RMS values in dc-link for the full ranges of phase angles of the 3rd and 5th harmonics in the ac current (I_3=50A and I_5=30A): (a) M_1=0.78; (b) M_1=0.97.

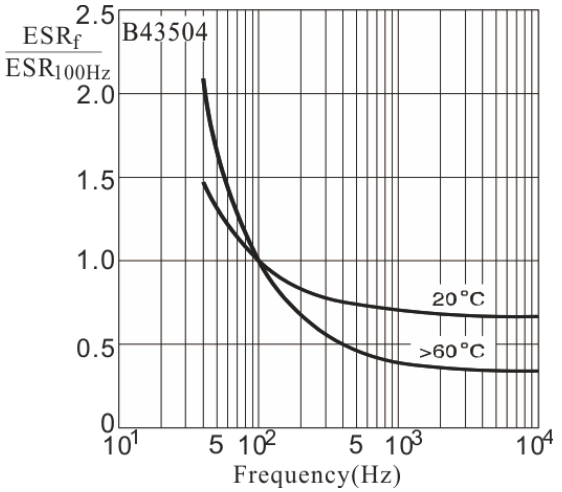


Fig. 10 B43504 series electrolytic capacitor (TDK EPCOS) ESR frequency dependency curve.

maximal permissible current (at 100Hz) at 60 ºC and the ESR value (at 100Hz) is only given for 20 ºC. Therefore, the power losses at 60 ºC of the LOHs and SHCs in the dc-link currents cannot be computed. Fortunately, the normalized ESR frequency characteristics at 60 ºC (the ratio of the ESR at certain frequency vs. the ESR at 100Hz) is given in Fig. 10. Therefore, computing the actual capacitor losses is no longer necessary. Instead, the normalized ESRs and the normalized capacitor losses at 100Hz, 200Hz, 300Hz and the switching frequencies for individual capacitors and the capacitor bank are computed and listed in Table IV.

The normalized losses of the capacitor bank and the individual capacitor are computed as 124.34 and 3.89 (M-index = 0.97), respectively. With the maximal permissible current of 3.51A (peak) at 60ºC as given by the datasheet, the allowable normalized individual capacitor loss is 6.16. Hence, there is sufficient design margin under the worst case operating point.

VI. Simulation, Experimental And Computational Results

To verify the effectiveness of the proposed computation methods, both simulation and experiment are carried out. The single phase H-bridge inverter prototype is constructed as in Fig. 11. The dc supply voltage and grid voltage are 420V and 220VRMS, respectively. The system parameters are listed in

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Table V. The dc-link capacitor bank is composed of two capacitors in series. The rated voltage, maximum permissible current and capacitance of the individual capacitor are 450Vdc, 16.3A at 60°C and 1800uF, respectively. The PWM and control loop frequency of the inverter are both 10kHz. The closed loop controller is a hybrid current regulator based on a PR in parallel with a RP controller. The H-bridge inverter is controlled as a single phase grid-tied programmable APF, which can inject into the grid multiple harmonic currents of arbitrary orders, phase angles and magnitudes, so that the dc-link harmonic currents could be conveniently evaluated. It should be noted that the H-bridge inverter test bench is constructed simply to verify the dc-link current computation models and simulation waveforms, so that its parameters and capacitor ratings are not optimally designed as demonstrated in the subsection D of Section V.

The test conditions for both the simulations and the experiments are the same and listed in Table VI. Both simulations and the experiments are done with more complicated multiple LOH currents injection into the ac grid, in order to confirm the effectiveness and accuracy of the proposed computation models for generic design cases. Moreover, the 4 test cases with the same set of the 3rd, 5th and 7th harmonics are also specifically designed to verify the worst case analysis as discussed in details in Section V.

A. Simulation Results

It is clear to see from Fig. 12 and Fig. 14(a) that the computational results of both the LOH currents and SHC RMS in the dc-link well matched the simulation results. It interesting to discover from Fig. 12(c) that, although three harmonics were present in the ac current, only the 2nd and 8th currents exist in the dc-link. This is because the 4th dc-link harmonics induced by the 3rd and 5th harmonic currents in the ac current cancel out each other. Similarly, the 6th dc-link harmonics are also cancelled out.

B. Experimental Results and Worst Case Verification

The test results and the LOH currents and SHC RMS values in the dc-link are shown in Fig. 13 and Fig. 14(b). It is clear that the experimental and computational results match very well. Also, the waveforms of the simulations and the experiments matches very well.

It should be noted that Fig. 13 (b)-(d) and Fig. 14(b) show the experimental results of LOH currents and SHC RMS value in the dc-link when the ac current contains the 3rd (10A), 5th (10A) and 7th (10A) harmonics with different phase angles. As analyzed in Section V, the worst case in this scenario is $\varphi_3 = \varphi_5$ and $\varphi_7 = \varphi_5$. This verifies the worst case analysis as in Section V.

It is very instructive to see from Fig. 13 that not only the dc-link current test results shows unusual and complicated envelope patterns, but also the same set of the LOHs in the ac current with the same amplitudes would have quite different dc-link current envelopes as their phase angles vary, so that their SHC RMS value would be different. This demonstrates that the proposed design methods provide a handy and generalized tool to analyze the dc-link current and obtain the worst case for capacitor power losses under arbitrary combinations of LOH currents in the ac current.

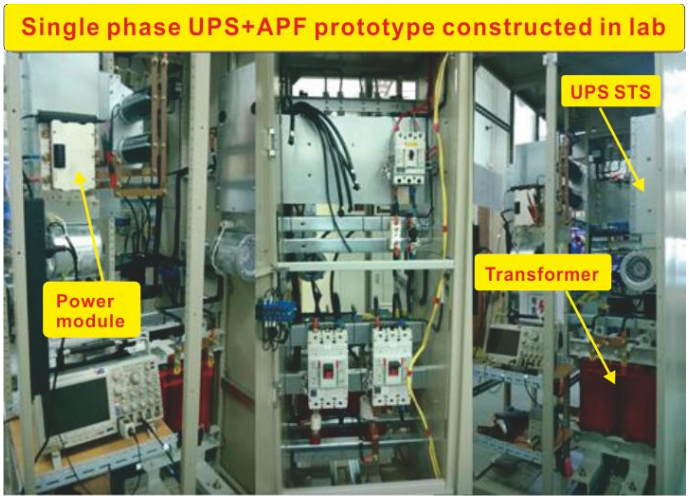

Fig. 11 Single phase H-bridge inverter prototype.

TABLE V
SYSTEM PARAMETERS

Description	Part Number	Parameters
Filter inductor on the grid side L_g	Custom-made	200uH
Filter inductor on the inverter side L_r	Custom-made	400uH
Filter capacitor (Y-connected) C_f	MKP1847610354P4	10uF
Damping resistor R_d	TEH100M1R00JE	1Ω
DC-link capacitor C_{dc}	B43725A5188M000	900uF
IGBT Power Modules	SKiiP 513GD122-3DUL	1200V

C. Error Analysis

Although both the experimental and simulation results of the dc-link LOH currents and SHC RMS value well matched the computational results, there are still slight differences among them. Table VII and Table VIII give the error percentages between the experimental and computation results for the LOH currents and the SHC RMS value, respectively. Note that the total RMS value of all the LOH currents computed with (12) as listed in Table VII is just used here to verify the overall accuracy, instead of being used for capacitor losses computation. Even though the error percentage is well within the design margin, it is very instructive to explain these differences as below.

The LOHs in the inverter output voltage, SHC ripples in the ac current and power module losses are the three main reasons for these differences. For simplicity, they are safely neglected when establishing the computation models for the dc-link LOH currents and the SHC RMS value. Suppose that the LOH voltages and SHC ripples in the ac current are considered during the derivation, the inverter output voltage as in (6) and (7) is redefined as

$$v_{out}^{'} = v_{out} + v_c \sum_{n=2} M_n \cos\left(n\omega_1 t - \varphi_{vn}\right) \tag{28}$$

$$i_{out}^{'} = i_{out} + i_{sw\_harm} \tag{29}$$

where the i_{sw_harm} represents the SHC ripples in the ac current.

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TABLE VI
TEST CASES FOR BOTH THE SIMULATIONS AND EXPERIMENTS

The tests cases for both the simulations and experiments	(a) I_1=10A (φ_1=0), I_3=10A (φ_3=0), I_5=10A (φ_5=0)	
	(b) I_3=10A (φ_3=0), I_5=10A (φ_5=0), I_7=10A (φ_7=0)	Worst case verification
	(c) I_3=10A (φ_3=0), I_5=10A (φ_5= π), I_7=10A (φ_7=0)	
	(d) I_3=10A (φ_3= π/4), I_5=10A (φ_5= 0), I_7=10A (φ_7=0)	
	(e) I_3=10A (φ_3= π/4), I_5=10A (φ_5= 0), I_7=25A (φ_7= π/4)	
	(f) I_5=10A (φ_5=0), I_7=10A (φ_7=0), I_9=10A (φ_9=0)	

Then the instantaneous power on the inverter ac side is obtained by multiplying (28) and (29) as

$$\begin{aligned} p_{ac}^{'} &= p_{ac} + v_{out} i_{sw\_harm} \\ &+ v_c i_{out} \sum_{n=2} M_n \cos\left(n\omega_1 t - \varphi_{vn}\right) \\ &+ v_c i_{sw\_harm} \sum_{n=2} M_n \cos\left(n\omega_1 t - \varphi_{vn}\right) \end{aligned} \tag{30}$$

By dividing the dc voltage v_c from (30), the dc-link current can be expressed as

$$\begin{aligned} i_{dc}^{'} &= i_{dc} + \frac{1}{2}\sum_{k=1}\sum_{n=2} I_k M_n \begin{bmatrix} \cos\left(\left(k-n\right)\omega_1 t - \varphi_k + \varphi_{vn}\right) \\ + \cos\left(\left(k+n\right)\omega_1 t - \varphi_k - \varphi_{vn}\right) \end{bmatrix} \\ &+ i_{sw\_harm} \sum_{n=2} M_n \cos\left(n\omega_1 t - \varphi_{vn}\right) + v_{out} i_{sw\_harm} / v_c \end{aligned} \tag{31}$$

Compared with the dc-link current expression in (10), the detailed dc-link current expression as in (31) has 3 extra components. The first extra component is the second term in (31), which indicates that the LOH voltages introduce additional dc-link LOH currents. The interaction between the n^{th} harmonic voltage and k^{th} harmonic current would induce the $(k\text{-}n)^{th}$ and $(k\text{+}n)^{th}$ LOH currents in the dc-link. For example, when the ac current consists of the 3rd, 5th and 7th harmonics, the inverter output voltage also has small amount of the 3rd, 5th and 7th harmonics besides the dominant fundamental frequency component. Therefore, besides the 2nd, 4th, 6th and 8th harmonic currents in the dc-link, it is deduced from (31) that the 0th, 10th, 12th LOH harmonic currents are also present in small quantities in the dc-link. This interesting phenomenon can also be observed from both the simulation and the experimental results as in the subplots (b, c, d, e) of Fig. 12 and Fig. 13. More interestingly, the experimental results in Fig. 13 have small amount of the dc-link LOH currents that are not present in the simulation. This is obviously due to the miscellaneous grid voltage harmonics not included in the simulations.

The second and the third extra components are the third and fourth terms in (31), which indicates that the LOH voltages together with SHC ripples in the ac current introduce extra SHCs in the dc-link. Therefore, the LOH voltages and SHC ripples in the actual ac current would lead to additional SHC RMS values in the dc-link in reality. Moreover, by neglecting the power module losses, the computational results will be even smaller than the reality. From Table VII and Table VIII, the deductions above are verified that the computation results are always less than experimental results. However, the computation results error percentage is reasonably low and within 9%, which can be safely absorbed by the design margin. Therefore, the LOH voltages, SHC ripples in the ac current and the power module losses can be safely neglected in deriving all the computation models in this paper.

VII. CONCLUSION

An analytical method for the dc-link current of the single phase H-bridge inverter with harmonic ac currents is presented in this paper. Due to the capacitor ESR frequency characteristics, the dc-link current harmonics are decomposed into the LOHs and SHC RMS, and formulated separately. The proposed method is effective to analyze various unusual dc-link current patterns under arbitrary combinations of LOHs in the ac current. Moreover, to accelerate the worst case dc capacitor design, the SHC RMS equations are further simplified into one equation. The comprehensive rule and the design flow chart are established to compute the capacitor losses worst case in a quantitative dc-link capacitor design case, considering both the SHC RMS values and LOH currents, under different M-index. In contrast, the spectral analysis or RMS equations in prior art are not possible to handle the design cases with multiple LOHs in the ac current. Finally, the various complicated dc-link current patterns in the simulations and the lab tests demonstrate that the proposed method is a practical and generalized tool to analyze the dc-link current of the single phase inverter under arbitrary harmonic ac currents. Moreover, the worst case analysis is verified by the experiment and the differences between the experiment and computation results are formulated and explained definitely.

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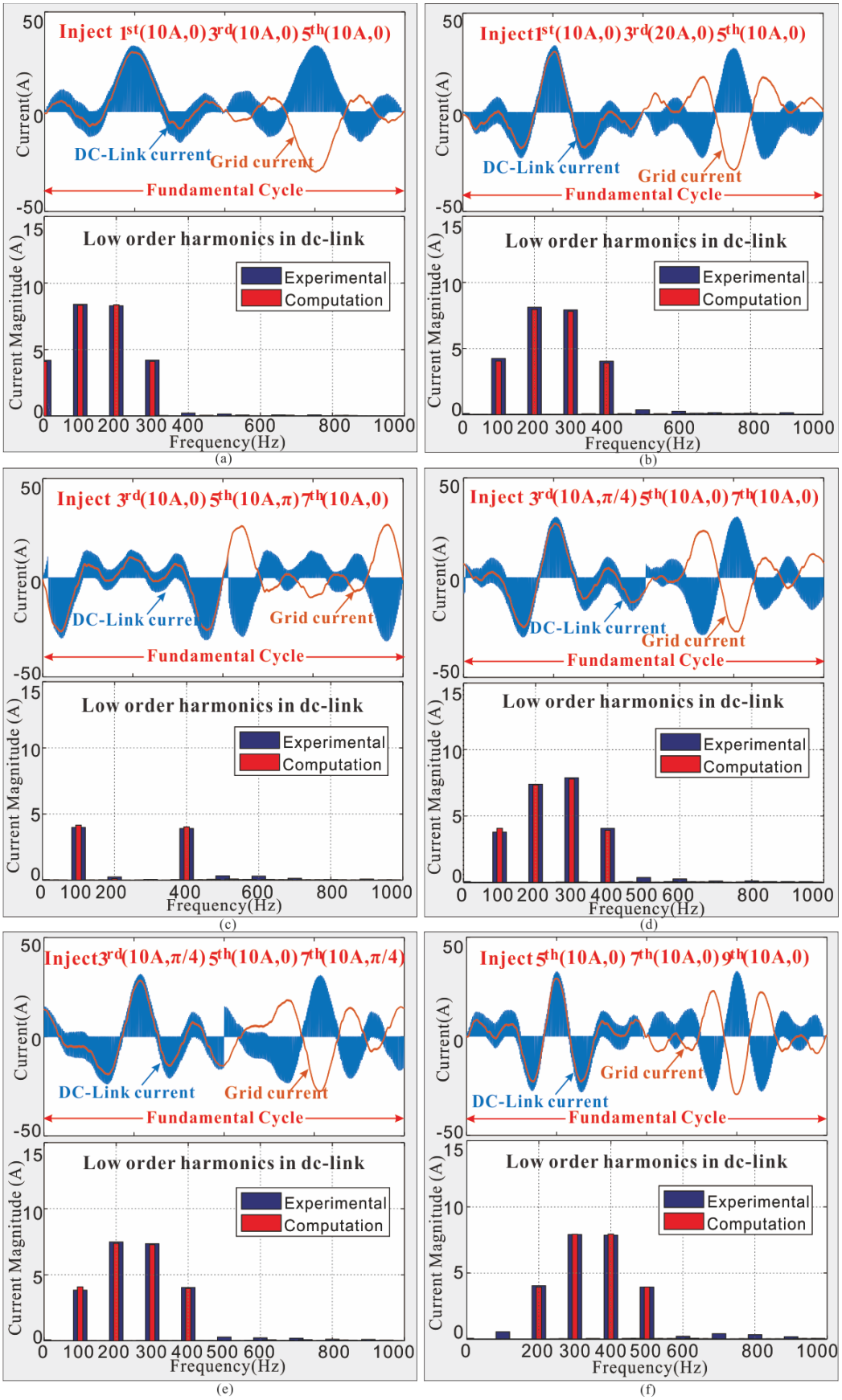

Fig. 12 Simulation and computational results of LOHs in the dc-link with six different combinations of harmonics in the ac current

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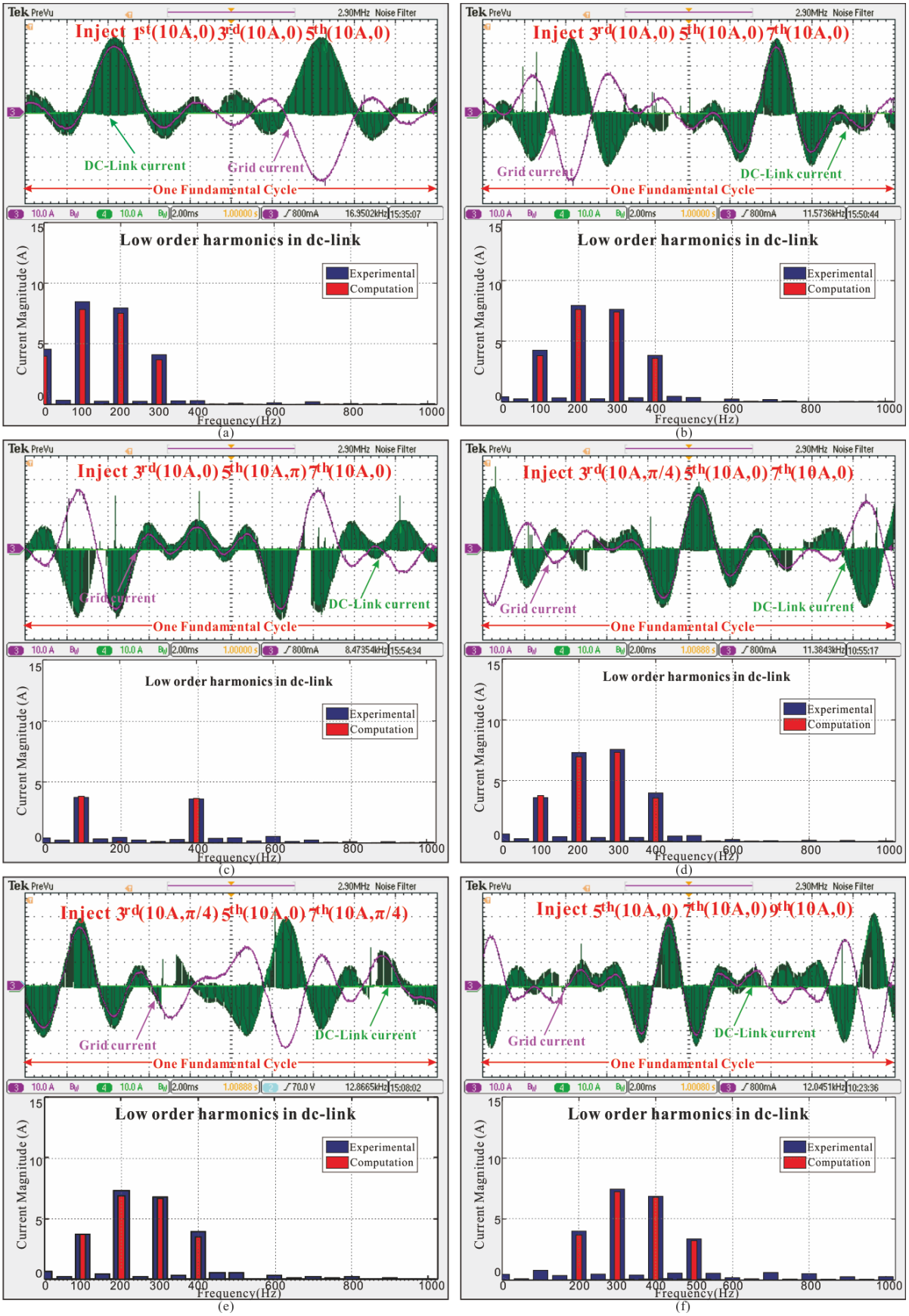

Fig. 13 Experimental and computational results of LOHs in the dc-link six different combinations of harmonics in the ac current.

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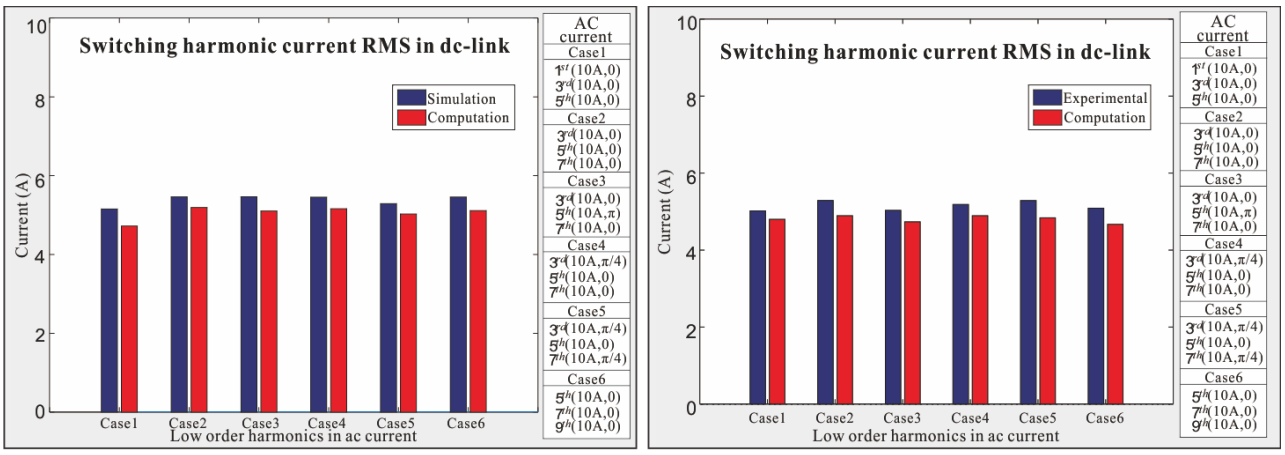

(a) (b)

Fig. 14 Simulation, experimental and computation results of the dc-link SHC RMS value with six different combinations of harmonics in the ac current (a): Simulation results; (b) Experimental results.

TABLE VII
THE TOTAL RMS RESULTS OF THE LOH CURRENTS (0-1KHZ) IN THE DC-LINK AS COMPUTED WITH (12)

AC Current	Experimental	Computation	Error Percentage
Inject 1st(10A,0), 3rd (10A,0), 5th (10A,0)	9.29A	8.58A	7.7%
Inject 3rd(10A,0), 5th (10A,0), 7th (10A,0)	8.80A	8.37A	4.9%
Inject 3rd(10A,0), 5th (10A,π), 7th (10A,0)	3.75A	3.73A	0.5%
Inject 3rd(10A,π/4), 5th (10A,0), 7th (10A,0)	8.41A	8.06A	4.2%
Inject 3rd(10A,π/4), 5th (10A,0), 7th (10A,π/4)	8.07A	7.66A	5.1%
Inject 5th(10A,0), 7th (10A,0), 9th (10A,0)	8.15A	7.83A	3.9%

TABLE VIII
THE SHC RMS VALUE (>1KHZ) IN THE DC-LINK

AC Current	Experimental	Computation		Error Percentage	
		NS	Simplify	NS	Simplify
Inject 1st(10A,0), 3rd (10A,0), 5th (10A,0)	5.02	4.80	5.28	4.4%	-5.2%
Inject 3rd(10A,0), 5th (10A,0), 7th (10A,0)	5.29	4.89	5.14	7.6%	2.8%
Inject 3rd(10A,0), 5th (10A,π), 7th (10A,0)	5.03	4.73	4.80	6.0%	4.6%
Inject 3rd(10A,π/4), 5th (10A,0), 7th (10A,0)	5.18	4.89	5.13	5.6%	0.97%
Inject 3rd(10A,π/4), 5th (10A,0), 7th (10A,π/4)	5.00	4.69	5.12	6.2%	-2.4%
Inject 5th(10A,0), 7th (10A,0), 9th (10A,0)	5.09	4.67	4.89	8.3%	3.9%

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