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PII: S0038-1101(18)30292-2
DOI: https://doi.org/10.1016/j.sse.2018.10.013
Reference: SSE 7481

To appear in: *Solid-State Electronics*

Received Date: 12 July 2018
Revised Date: 2 October 2018
Accepted Date: 16 October 2018

Please cite this article as: Li, Z., Zhou, K., Zhang, L., Xu, X., Li, L., Li, J., Dai, G., A Simple Multistep Etched Termination Technique for 4H-SiC GTO Thyristors, *Solid-State Electronics* (2018), doi: https://doi.org/10.1016/j.sse.2018.10.013

A Simple Multistep Etched Termination Technique for 4H-SiC GTO Thyristors

Zhiqiang Li, Kun Zhou, Lin Zhang, Xingliang Xu, Lianghui Li, Juntao Li and Gang Dai

***Abstract*—An edge termination technique, referred to as simple multistep etched junction termination extension (SME-JTE), is presented for 4H-silicon carbide gate turn-off thyristors (4H-SiC GTO). The proposed termination technique can form over ten steps in the termination region with only requiring a few of etching steps. Numerical simulations show that a high termination efficiency over 95% with broad process window for etching depth is obtained for the SME-JTE technique. In addition, a high breakdown voltage of 7500V has been experimentally demonstrated for the 4H-SiC GTO with 8-step JTE, and which is about 91% of the ideal breakdown voltage for the 50μm drift layer. The high termination efficiency and simple process of SME-JTE makes it applicable for fabrication of various high-voltage power devices.**

***Index Terms*—Junction termination extension, Gate turn-off thyristor, Silicon carbide, Breakdown voltage.**

I. Introduction

Silicon carbide (SiC) is considered as a promising material for next-generation power devices due to its unique intrinsic properties such as high electric breakdown field strength, wide bandgap and high thermal conductivity [1, 2]. And the 4H-SiC gate turn-off thyristor (4H-SiC GTO) is of specific interest for pulsed-power applications because of its great advantages over silicon counterparts, such as high-temperature, high-voltage, and high-current applications [3, 4].

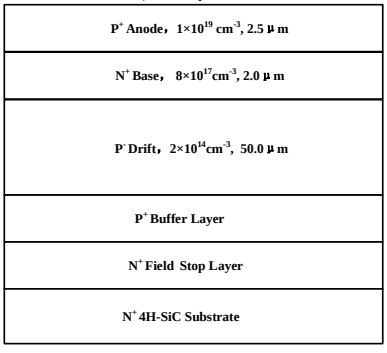
Edge termination is a critical technology for power devices. An effective edge-termination technique makes the electric field distribution more uniform at the edge of the device, and which makes the device approach the ideal breakdown voltage capability of the epitaxial layer used. And several specialized edge terminations have been developed to mitigate this effect, including floating guard rings [5], field plates [6], junction termination extensions (JTE) [7-8], and the JTE technique has become one of the preferred methods due to its simple design and high termination efficiency.

The JTE technique is usually formed by ion implantation, including multiple-floating-zone JTE, space-modulated JTE and multiple-ring-modulated JTE [9-11]. However, the activation of the implanted dopants is strongly dependent on annealing temperature and time. Moreover, the ion implantation and high temperature annealing process result in crystal damage and surface roughness, which usually affects the performance of power device. Recently, the etched termination has attracted wide attentions because of its simplicity in device design and implantation-free processing. And one of the etched terminations studied in SiC BJT and PiN devices is the single-step JTE, but its BV performance shows high sensitivity to etching depth [12, 13]. Therefore, the multistep JTE formed by etching are developed for wider tolerance of etching step variation [14, 15], and the highest BV of 22kV is achieved with over ten steps JTE in 4H-SiC GTO device [16], but the complexity and cost of device fabrication are significantly increased.

In order to realize multistep JTE in a cost-effective way, a method called simple multistep etched JTE (SME-JTE) is proposed in this letter. This method can effectively reduce etching process for realizing multistep JTE, and 16-step JTE only needs 5 etching process. Meanwhile, device simulations and experiments have been carried out to investigate the etching depth variation tolerance and termination efficiency of the SME-JTE technique, broad tolerance for etching depth variation and high termination efficiency have been demonstrated for the 4H-SiC GTO device with SME-JTE technique.

II. Epitaxial Stttucture and SME-JTE Design

Fig. 1 shows the schematic cross-section of the thyristors. The conventional asymmetric blocking p^+np^-pn structure is used for 4H-SiC GTO device. The five epitaxial layers were grown on an 8°-off n-type 4H-SiC wafer from Cree, Inc. The p^--doped drift layer has a thickness of 50μm and a doping concentration of about 2×10^{14} cm^{-3}, and the simulated forward breakdown voltage of the plane-parallel structure is 8270V. The highly doped anode layer (p^+ 1×10^{19} cm^{-3}) is 2.5μm and the gate layer (n ~8×10^{17} cm^{-3}) is 2μm thick.



This work was supported by Science Challenge Project, No. TZ2018003.

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Fig.1. The cross section of the five epitaxial layers of p+np−pn structure.

The design of SME-JTE is illustrated in Fig.2. The thickness of n-type base layer used for the edge termination fabrication is set as D. All the step lengths are equal. Except the first step depth d_1, all the left etching depths (d_i, i = 2…n) are equal, where n is the step number of JTE. The etching processes are implemented as following, the first etching is used to form the JTE region in Fig.1 (a), and the etching depth is d_1. The second etching is used to form 2-step JTE with etching depth of $(D-d_1)/2$ in Fig.1 (b). By increasing another etching step with etching depths of $(D-d_1)/4$ in Fig.1(c), a 4-step JTE is formed. As it expected, the number of JTE increases exponentially with the number of etching processes, and it is demonstrated that the 16-step JTE can be realized with another 2 etching processes in Fig.1 (d) ~Fig.1 (e). Thus this technique can achieve multistep JTE with requiring only a few of etching processes, which obviously reduces device fabrication complexity and cost. The final etching in Fig.1 (f) is used to form isolation in device fabrication.

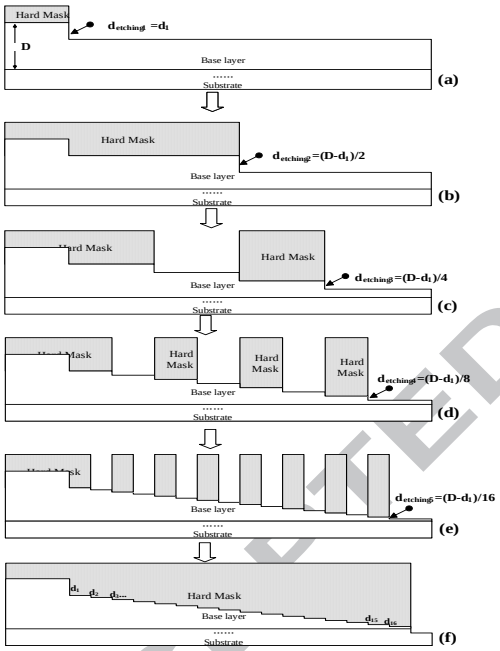


Fig.2. The design of SME-JTE technique.

III. DEVICE SIMULATION

2-D device simulations have been carried out using Synopsys Technology Computer-Aided Design program (TCAD) Sentaurus. The SME-JTEs have been investigated with different JTE step. All the simulated structures have the same total termination width of 400μm, and the step length of 2-step, 4-step, 8-step and 16-step JTE are 200μm, 100μm, 50μm and 25μm, respectively. The thickness of n-type base layer for the formation of JTE is set as 1.8μm. Excepting the first etching depth d_1, all the left JTE steps have the same etching depth, thus the thickness of JTE step is actually controlled by the first etching depth d_1.

And Fig.3 shows the simulated BV as a function of the first etching depth d_1. According to theory, the ideal BV of 50μm p-drift layer doped 2×10^{14} cm^{-3} in this letter is about 8270V [17], however, the simulated maximum BV for the 2-step JTE structure is 6700V with d_1 at 1.5μm, which is much lower than the ideal value due to the high electric filed in the periphery of main junction. As the JTE steps increasing from 4 to 16, the simulated maximum BV value is significantly increased and gradually saturated at 7950V, which is about 96% of the ideal value. Meanwhile, the tolerance for etching depth variation of d_1 is also obviously enhanced with increasing the JTE steps. As it shown in Fig.3, the BV is sharply reduced around the optimum value of d_1 (1.5μm) for the 2-step JTE, which is due to the high sensitivity to etching depth, and it presents a big obstacle in the real device fabrication. As increasing JTE step, the range of etching depth d_1 is obviously widened (>80% ideal breakdown voltage), and large etching window of d_1 ranging from 0.1μm to 1.4μm is obtained for the 16-step JTE, which is ascribed to the alleviated peak electric field at JTE region.

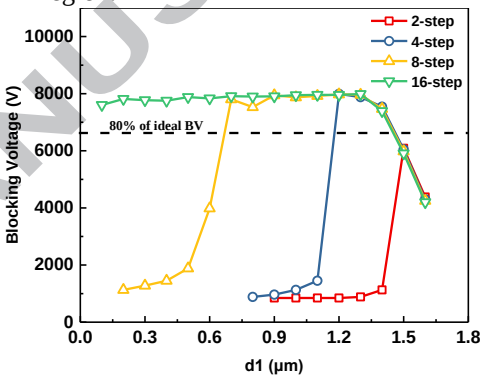
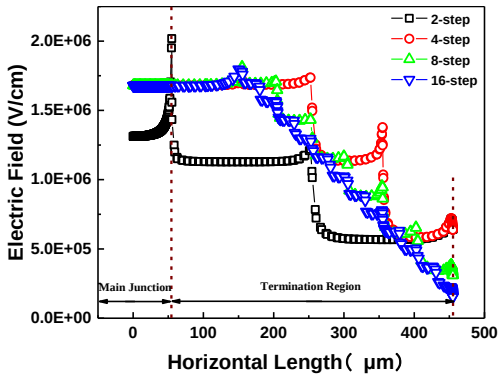
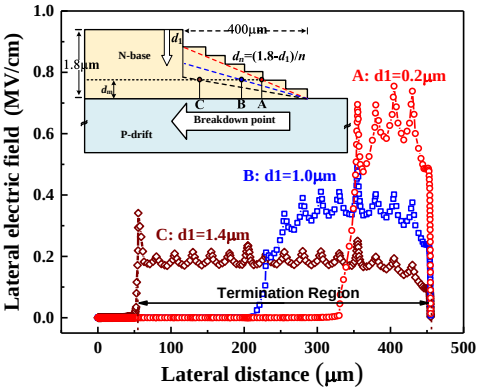


Fig.3. The simulated BVs as functions of extents on etching depth d1 with various JTE step

Fig.4 gives the electric field distribution for the SME-JTEs. As shown in Fig.4 (a), the maximum electric field is 2.02MV/cm near the main junction for the 2-step JTE. An obvious reduction of the peak electric fields (about 1.72MV/cm) is observed in the 4-step JTE, 8-step JTE and 16-step JTE, and thus the maximum BVs are increased to about 7950V. Besides, with increasing the JTE steps, the electric field at JTE region becomes more flat, and thus the etching depth window is also obviously widened. Fig.4 (b) gives the electric field component along the lateral direction at the PN contact interface for 16-step JTE with various d1 to further explanation for the broad etching tolerance. Due to the large number of JTE step, the change of d_1 induces small dose variation between the neighboring JTE steps, which is beneficial to suppress the electric field peak at the edge corner between the neighboring JTE steps. Hence, the increase of d_1 just leads to the lateral extension of the JTE depletion towards to the main junction while the BV remains around the optimum value due to the self-adaptive lateral field.



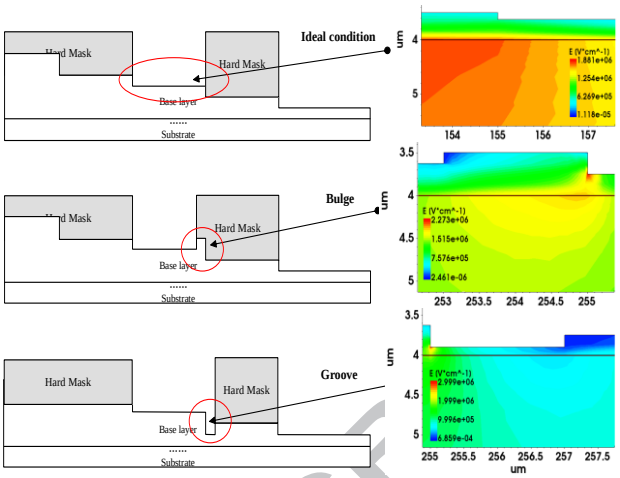
(a) Electric field at the PN contact interface with various JTE step.



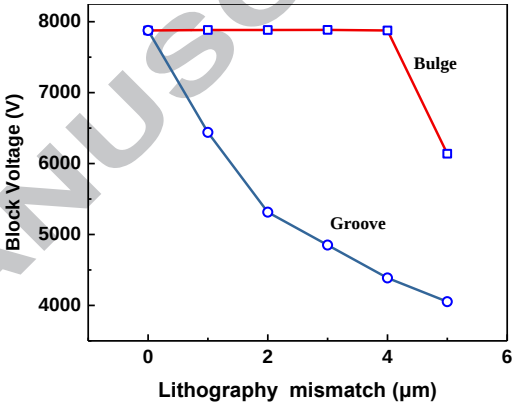
(b) Electric field component along the lateral direction at the PN contact interface for 16-step JTE with various d1.

Fig.4. The simulated electric field distribution for SME-JTEs.

The BV characteristic may be deviated from the ideal situation due to lithography mismatch, and which is also investigated in these letter. As it shown in Fig.5, there are two kinds of JTE morphology resulted by lithography mismatch for the 4-step JTE. One is a bulge formed after the two overlap etching steps, and the simulated BV is stabilized at 7880V with the etching error less than 4μm, and which is due to the small dose increased at the edge termination compared to the ideal condition. The bulge formed with the common lithography mismatch is usually smaller than 2μm, therefore, the bulge has little influence on the capacity of blocking voltage. The other is a groove formed after the two apart etching steps. The blocking voltage is obviously decreased to 6440V with 1μm etching error, and which is about 18% lower than that of the ideal condition. More serious BV characteristic degeneration occurred with larger etching error, which is due to the formed groove acting as a micro-trench in the etching region, and thus the electric filed crowding is occurred at the groove corner. The maximum electric fields of 4-step JTE with the ideal condition, 2μm-bulge and 2μm-groove etching error are separately 1.88MV/cm, 2.27MV/cm and 3.00MV/cm, which also verifies that the block voltage is more susceptible to the apart mismatch of lithography.



(a) The formed 4-step JTE with different lithography mismatch.



(b) the influence of lithography mismatch on BV characteristic.

Fig.5 the influence of lithography mismatch on JTE morphology and BV characteristic.

IV. Experimental Results and Discussion

The 4H-SiC GTO fabrication started with conventional lithography to define the anode, and it was etched with SiO_2 mask. And then, 4 steps dry etch were carried out to form 4-step and 8-step JTE. The 4H-SiC GTO devices with 4-step JTE were especially designed with the ideal condition, 2μm-bulge and 2μm-groove etching errors for the JTE etching steps. After JTE formation, the device isolation is done by etching the SiC down to the drift-layer. The gate contact implant was carried out next, using nitrogen with a box like profile. After the surface SiC was removed by sacrificial oxidation, the anode, gate and the backside ohmic contacts were formed using annealed Nickel-based metal system. The Al overlayer metal was patterned on the front and the Ag overlayer metal was deposited on the back. Finally, the polyimide layer was patterned on the front to open the bond pads for anode and gate terminals. The image of the fabricated 4H-SiC GTO is shown in Fig.6.

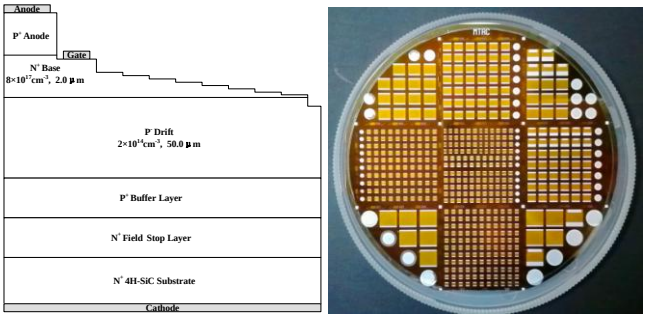


Fig.6. The cross section and image of 4H-SiC GTO with 8-step JTE.

On-wafer blocking characteristics are carried out with the Cascade Microtech probe and the Agilent B1505 semiconductor characterization system. The measurement was done at room temperature by immersing the GTO wafer in Fluorinert oil. As shown in Fig.7, the BV of the device with 8-step JTE is about 7500V, and the termination efficiency is as high as 91%, and the device with 4-step JTE give a similar BV value of 7200V, which demonstrates that the SME-JTE technique is very effective for blocking characteristic improvement.

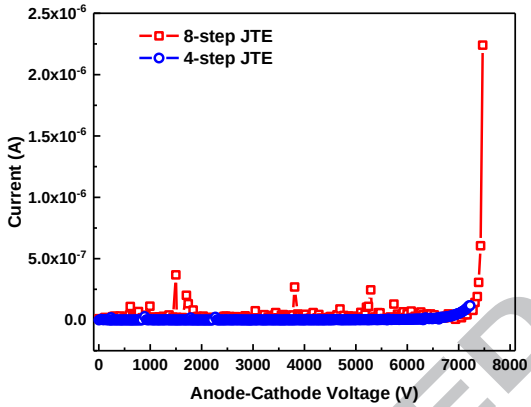


Fig.7. Breakdown capability of the fabricated 4H-SiC GTOs with 4-step and 8-step JTE.

The influence of lithography mismatch on BV characteristic is also experimentally investigated in these letter. As shown in Fig.8, the BV of the ideal condition device is about 7200V for the 4H-SiC GTO with 4-step JTE, and the measured BV is about 7000V for the 2μm-bulge device, approaching 97% of the ideal condition device, which demonstrates that the bulge has little influence on the capacity of blocking voltage. While for the 2μm-groove device, the measured BV is about 5600V, which verifies that the blocking voltage is obviously decreased compared with the ideal condition. Therefore, it can be concluded that the influence of groove etching error on BV characteristic is more serious than that of bulge.

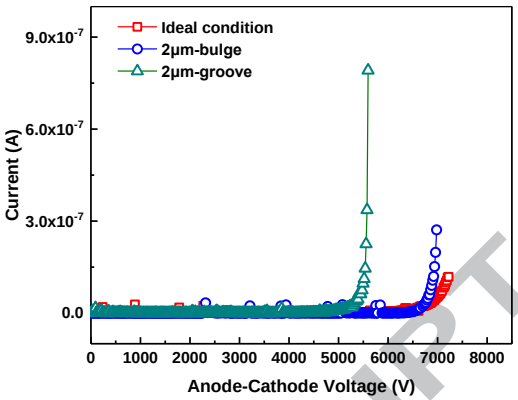


Fig.8. Breakdown capability of the fabricated 4H-SiC GTO with 4-step JTE under different lithography mismatch condition.

V. Conclusion

In conclusion, the SME-JTE technique is proposed for edge termination formation in 4H-SiC GTO device. The SME-JTE technique can form multistep edge termination with great reducing the processing complexity and cost, and the simulation results show that high efficiency of termination (over 95%) is achieved with broad etching window. Meanwhile, a high BV of 7500V is experimentally demonstrated with 50μm drift layer, which is about 91% of the ideal value. The excellent breakdown voltage characteristic of 4H-SiC GTO device indicates that the SME-JTE technique is well suited for application in 4H-SiC GTO and other high-voltage power devices.

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Gang Dai

Highlights:

- A simple multistep etched junction termination extension (SME-JTE) is presented and it only requires a few of etching steps to form over ten steps in the termination region.
- Numerical simulations show that a high termination efficiency over 95% with broad process window for etching depth is obtained for the SME-JTE.
- High breakdown voltage of 7500V with efficiency over 90% has been experimentally demonstrated for the 4H-SiC GTO with 8-step SME-JTE.
- The SME-JTE is very applicable for high-voltage power devices due to its high termination efficiency and simple process.