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**Low frequency noise investigation of n-MOSFET single cells for memory  
applications**

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**Abstract**

In this paper, we present a detailed investigation of low frequency noise (LFN) for different n-MOSFET devices dedicated for memory applications. We investigate the impact of the gate oxide thickness (GOX) on LFN. We analyzed how the position, the existence and the composition of Lightly Doped Dopant (LDD) implant in the source/drain region affect the LFN performance of the device. The results demonstrates that the thinner gate oxide and the device without LDD improved the noise performance compared the devices with thick GOX and with LDD implants. On the other hand, the absence of LDD implant on one side of the MOSFET didn't reveal a global trend for all measured devices. Finally, the different LDD implant composition resulted in different LFN performance which is gate area dependent. These results can be used from both process and design engineers to improve the LFN of n-MOSFET.

**Keywords:** low frequency noise, CMOS, n- MOSFET, logic NVM

## 1. Introduction

Today, it is well known that LFN can be used as a characterization tool for the quality and the reliability of the devices [1-2]. It is obvious that the level of noise has a direct impact on the device quality. In addition, LFN can influence the design of an electronic circuit since it can limit the overall performance and operation. Thus, the noise investigation of special architecture devices is of paramount importance for device and design engineers. Single transistors designed for logic NVM of SONOS type memory applications [3] can be used for LFN comprehension analysis due to the special architecture they have. In this experiment five single cell n-MOSFET devices were designed for memory applications and used for noise analysis.

In literature exists a number of publications referring to LFN characterization for logic NVM of SONOS type [4-7]. According to our knowledge, we could not find a prior work that used these type of devices for LFN improvement purposes and not for simple characterization. We tried not only to identify the main source of LFN in these devices but also to use this info for the improvement of LFN performance in CMOS technology.

In MOSFETs, it is generally accepted that the flicker ( $1/f$ -like) noise originates either from carrier number fluctuations (CNF) (Eqes 1, 2 Table 1) [1] or from Hooge mobility fluctuations [8]. The CNF noise is due to carrier exchange between the near-interface gate dielectric traps and the channel. The charge fluctuations in the gate dielectric could also induce fluctuations of the carrier mobility, giving rise to the so-called correlated mobility fluctuations (CMF) (Eqes 3, 4 Table 1) [9-11].

These devices show great interest for  $1/f$  noise analysis since they have special architecture in terms of LDD composition and gate oxide thickness. We are going to show how the different gate oxide thickness affects the noise performance when everything else in the device remains unchanged. We will see how the asymmetrical LDD implant or the lack of it (with/without LDD on Drain/Source side) can influence the LFN level. Finally, a comparison of two different LDD implants composition will give a better insight on the noise performance of the devices.

## 2. Experiment

Electrical measurements were carried out on n- MOSFET transistors issued from a bulk CMOS technology node. The channel material is Si. Different width devices for  $L=0.18\mu\text{m}$  measured:  $W=0.22, 0.44, 2, 5$  and  $10\mu\text{m}$ . Different length devices for  $W=1\mu\text{m}$  measured:  $L=0.25, 0.3$  and  $0.4\mu\text{m}$ . The gate stack consists of SiON-based oxide dielectric with equivalent oxide thickness given in Table 2.

In the following, we are going to present the different measured devices in more details. We are going to use a prefix number i.e 1, 2, 3, 4 and 5 in order to distinguish them. Tables 2 and 3 summarizes the most important differences. It can be seen that these devices have a “special” architecture with or without or different LDD implants in the Source/Drain region and GOX thickness. These “exotic” devices can reveal useful insights of the LFN behavior of n-MOSFET. We can better understand how the gate oxide thickness affects the LFN when everything else remains unchanged (devices D1 and D2). We can investigate how the different LDD implant composition and the asymmetry of Source/Drain architecture affects the LFN with devices D2,

D3, D4 and D5.

Static characterization was performed in order to obtain the transfer ( $I_D - V_G$ ) characteristics and then to extract typical MOSFET parameters. LFN measurements were performed using a Cascade Edge system [12] for low frequency noise measurements. Drain current noise measurements were carried out in linear region of operation. The drain voltage  $V_D$  was fixed to 0.1V and the gate voltage varied from weak to strong inversion. The experimental bandwidth is 1Hz to 10KHz. It should be noted that all the spectra presented in this work are the average of at least 10 dies, thus suppressing the impact of Random Telegraph Signal (RTS)-induced Lorentzian-like spectra in small area devices [13]. All noise parameters were extracted at  $f=10$ Hz.

Below we will describe the analysis procedure we followed. First, we analyzed the basic DC operation of the devices to verify any abnormalities. It is not the purpose of this paper the in-depth investigation of the DC performance. Then, we focused on the noise measurements and specifically we used the average noise spectrum for the analysis. It had  $1/f^\gamma$  shape with  $\gamma$  close to unity. We investigated which model better fits our experimental data. Then, we used the basic extracted parameter from this model to compare the noise performance.

This paper focus on the understanding of how the different architecture devices affects the LFN performance. Thus, we compared devices with special features in order to analyze how this affect the noise performance. We investigated the impact of (i) gate oxide thickness (devices D1 and D2) (ii) devices with and without LDD on Drain/Source side (devices D2 and D4) (iii) LDD asymmetry on Drain side (devices D2 and D3) (iv) LDD asymmetry on source side (devices D3

and D4) and (v) different LDD implant composition on Drain side (devices D2 and D5) on LFN. In addition, we analyzed the impact of both gate device width and length by measuring devices with  $L=0.18\mu\text{m}$  and various widths and devices with  $W=1\mu\text{m}$  and various gate lengths.

### 3. Results and discussion

Fig. 1 shows simple IDVG curves for different width and length devices. These transistors are showing different DC performance since their basic process features are not the same i.e. different gate oxide thickness and LDD composition. Nevertheless, the devices are working properly and they are not showing any abnormalities.

The drain current spectra of randomly selected devices are shown in Fig. 2 and various values of drain current. It is clear that the average noise spectra is  $1/f^\gamma$  like between 10 to 100Hz with  $\gamma$  close to 1. Similar results were obtained for all investigated bias conditions and devices. Fig. 3 shows the drain current spectrum for D3  $W/L=1/0.4\mu\text{m}$  for  $I_D=50\mu\text{A}$  and 10 sites. It can be seen from this graph the LFN dispersion. The average spectrum is showing  $1/f$ -like shape.

In order to verify which model better fits our experimental data we plotted the normalized drain current noise versus drain current in Fig. 4 for different area devices. The CNF model better describes our experimental data in all cases. According to this model, see Equ. 1-2 Table 1, the flat band voltage spectral density, SVFB, is the main parameter and the one we will use to compare the LFN performance. This parameter of each measured area and type of device is extracted according Equ. (1) and it is used for the comparison of the LFN performance.

According to [14], we used the statistical mean values of the linear noise data. The linear data

mean values are nearly constant with the device area, indicating that the quality of the gate oxide is maintained even at very small device area, showing no specific process-induced short or narrow channel effects.

The next step in our analysis procedure is the comparison of the extracted normalized SVFB values from all devices. We tried to divide the analysis in different parts because we wanted to focus on the impact of specific device features on LFN. Figs 5 and 6 are showing the normalized flat band voltage spectral density versus device width and length for all measured devices, respectively.

- **Impact of Gate Oxide thickness (Devices D1 and D2).** In all cases D2 is showing much higher noise compared to D1. This is attributed to the different gate oxide thickness that affects the noise level according to Equ. (2). D2 has thicker gate oxide thus smaller equivalent gate oxide capacitance which leads to higher flat band voltage spectral density assuming that the volumetric trap density is remaining unaffected since we are talking about the same process.
- **Impact of LDD in both sides (Devices D2 and D4).** D4 does not have any LDD implant in both Source and Drain side. In all cases, the normalized flat band voltage spectral density of D4 is smaller compared to D2. There are many studies of the impact of LDD in LFN [14-17] and all of them concludes that the LDD is increasing the LFN through the raise of source/drain resistance. We verified this tendency for all measured devices.
- **Impact of LDD in Drain side (Devices D2 and D3).** For devices 2 and 3, we investigated how the LDD implant in Drain side can influence the LFN performance of the



devices. D2 has the LDD implant on both sides compared to D3 that it has it only in Source side.

It can be seen that D3 has higher normalized flat band voltage spectral density values compared to

D2 for all measured devices for  $W=1\mu\text{m}$ . The situation is not clear for devices with  $L=0.18\mu\text{m}$ .

One could consider in this case that the lack of LDD in Drain side will directly lead to an

improvement of LFN in all cases. Apparently there is a different trend for devices with different

width and length. The asymmetry of drain/source side alters the LFN device performance in

respect to the device width and length.

- **Impact of LDD in Source side (Devices D3 and D4).** In this case, the device D3 with LDD on source side has higher noise compared to the one with no LDD implant.

- **Impact of different LDD composition in Drain side (Devices D2 and D5).** Finally, the devices D2 and D5 which are having different LDD composition in Drain side showed the following results. D5 is showing higher noise than D2 for all different gate lengths and constant gate width but not in the other case. For  $L=0.18\mu\text{m}$ , it is unclear which device shows higher noise since it depends on the device gate width.

One possible explanation for the results concerning devices 2,3,4 and 5 could be found in a previous work regarding the impact of LDD implants on LFN, Ref. [15]. Based on this work we

verified that the LDD composition can alter the carrier distribution for each device geometry

differently. Thus, the noise performance can be different for each device width and length leading

to different trend, which is verified from this study as well.

#### 4. Conclusions

In this manuscript, we investigated the LFN performance of special n-MOSFET transistors dedicated for logic NVM memory applications. The architecture of these devices can improve our understanding of the LFN behavior of n-MOSFET. Here we compared the impact of different gate oxide thickness on the LFN. The devices with thicker gate oxide thickness are noisier compared the thinner ones. Then, we investigated how the LDD implant on source/drain side can influence the noise level. The devices with no LDD in both sides are showing smaller noise. The analysis of the devices with LDD on drain/source side and with different LDD implant composition on drain side did not revealed a global trend. We have showed that the LFN of these devices is area dependent.

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**Tables and Figures captions**

Table 1. CNF and CMF low frequency model.

Table 2. LDD and GOX description

Table 3. Measured devices

Fig. 1. ID-VG curves for all type of devices for  $V_D=0.1V$  with (a)  $W/L=0.22/0.18\mu m$  and (b)  $W/L=10/0.18\mu m$ , respectively.

Fig. 2. Drain current spectra for device D3 with  $W/L=10/0.18\mu m$  at  $V_D=0.1V$ .

Fig. 3. Drain current spectra of 10 sites for device D3 with  $W/L=1/0.4\mu m$  at  $V_D=0.1V$  and  $I_D=50\mu A$ .

Fig. 4. Normalized drain current spectral density versus drain current for  $V_D=0.1V$  devices D1 with  $W/L=0.22/0.18\mu m$  and D3 with  $W/L=0.44/0.18\mu m$ .

Fig. 5. Normalized flat band voltage spectral density for  $V_D=0.1V$  and all device types versus various gate length for  $W=1\mu m$ .

Fig. 6. Normalized flat band voltage spectral density for  $V_D=0.1V$  and all device types versus various gate width for  $L=0.18\mu m$ .

**Table 1. CNF and CMF low frequency model**

CNF: $\frac{SID}{ID^2} = \left(\frac{GM}{ID}\right)^2 \cdot SVFB$ (1)	CNF: $SVFB = \frac{q^2 \cdot kT \cdot \lambda \cdot N_t}{W \cdot L \cdot C_{ox}^2 \cdot f^\gamma}$ (2)
CMF: $\sqrt{SVG} = \sqrt{SVFB} + \Omega \cdot \sqrt{SVFB} \cdot \frac{ID}{GM}$ (3)	
CMF: $\frac{SID}{ID^2} = \left(\frac{GM}{ID}\right)^2 \cdot SVFB \cdot \left(1 + \Omega \cdot \frac{ID}{GM}\right)^2$ (4)	
<p>Where <math>\Omega = a_{sc} \cdot \mu_{eff} \cdot C_{ox}</math>, <math>a_{sc}</math> is the Coulomb scattering coefficient, <math>\mu_{eff}</math> is the effective carrier mobility, <math>C_{ox}</math> is the gate dielectric capacitance per unit area, <math>SVFB</math> is the flat-band voltage spectral density, <math>SVG = f^\gamma \cdot SID / GM^2</math> the input voltage spectral density, <math>ID</math> is the drain current, <math>GM</math> is the transconductance, <math>SID</math> is the drain current noise spectrum, <math>kT</math> is the thermal energy, <math>\lambda</math> is the tunnel attenuation distance (<math>\approx 0.1</math>nm for <math>SiO_2</math>), <math>q</math> is the elementary charge, <math>f</math> is the frequency, <math>\gamma</math> is the slope of the drain current spectrum (close to 1) and <math>N_t</math> is the gate dielectric trap density in <math>cm^{-3} \cdot eV^{-1}</math>.</p>	

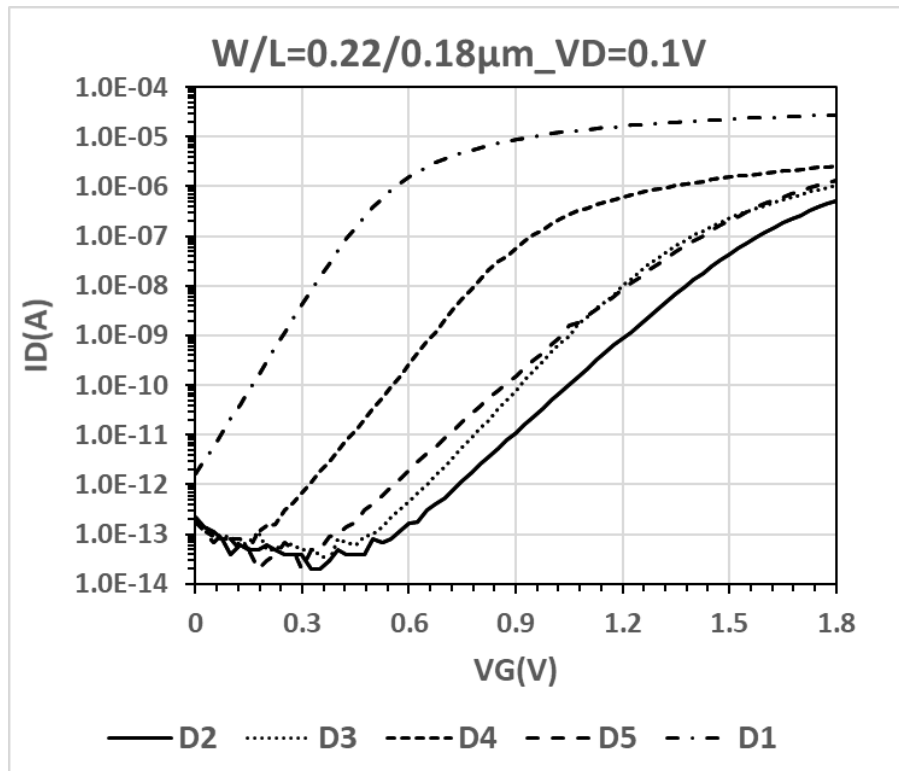
**Table 2. LDD and GOX description**

Parameter	Description
<b>LDD1</b>	B with X energy, Y dose and Z angle
<b>LDD2</b>	As with higher energy than LDD1 and the same dose and angle
<b>GOX1</b>	SiON-based oxide dielectric, EOT=4.45nm
<b>GOX2</b>	SiON-based oxide dielectric, EOT=12.6nm

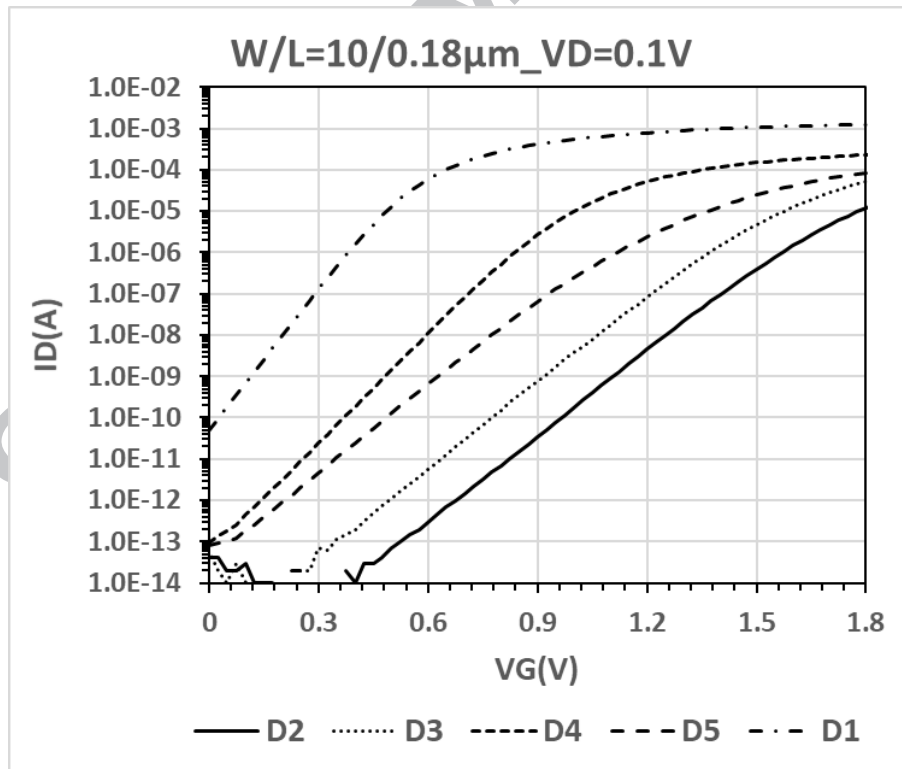
Table 3. Measured devices

Device	Oxide type	LDD type	
		Source	Drain
D1	GOX1	LDD1	LDD1
D2	GOX2	LDD1	LDD1
D3	GOX2	LDD1	-
D4	GOX2	-	-
D5	GOX2	LDD1	LDD2





(a)



(b)

Fig. 1

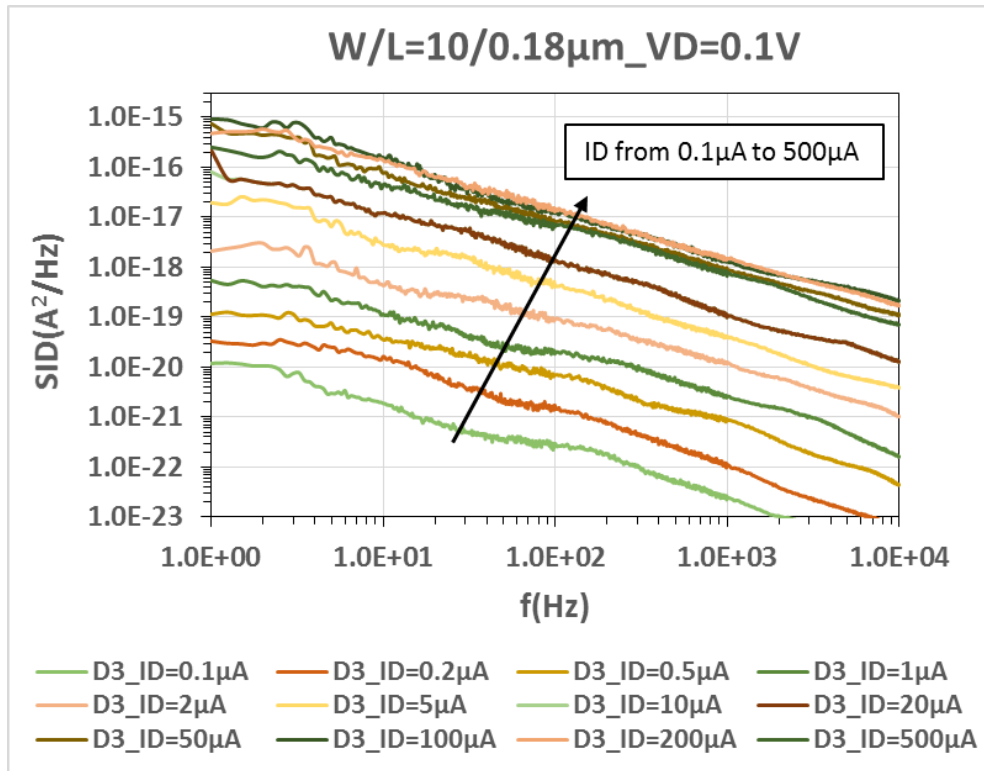


Fig. 2

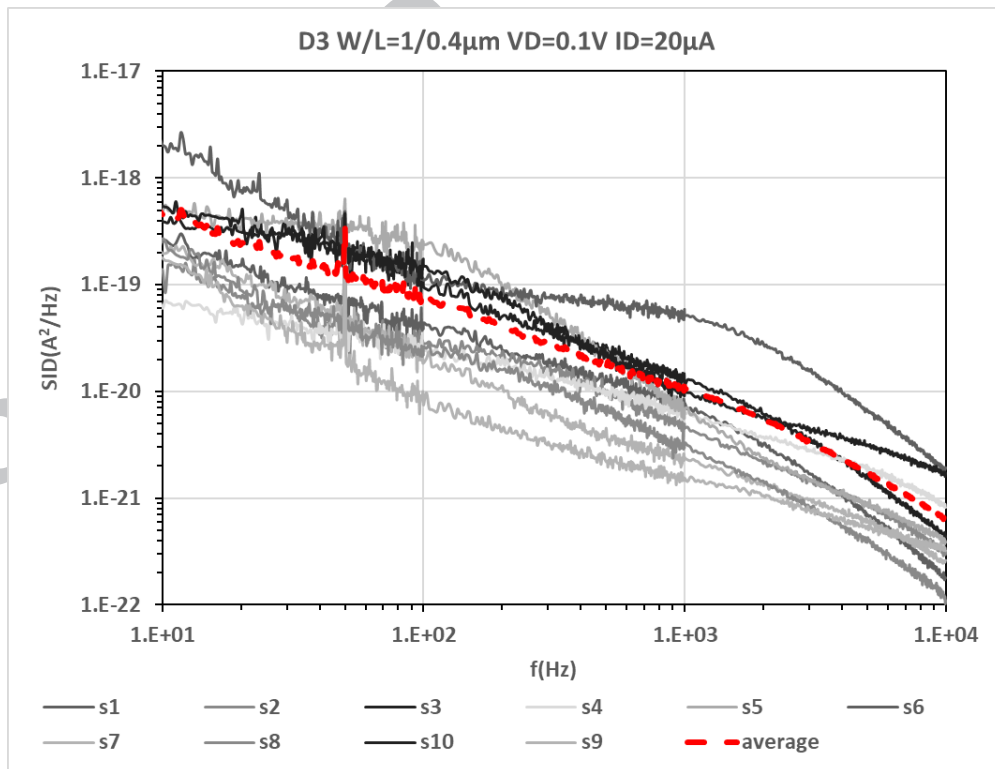


Fig. 3

(b)

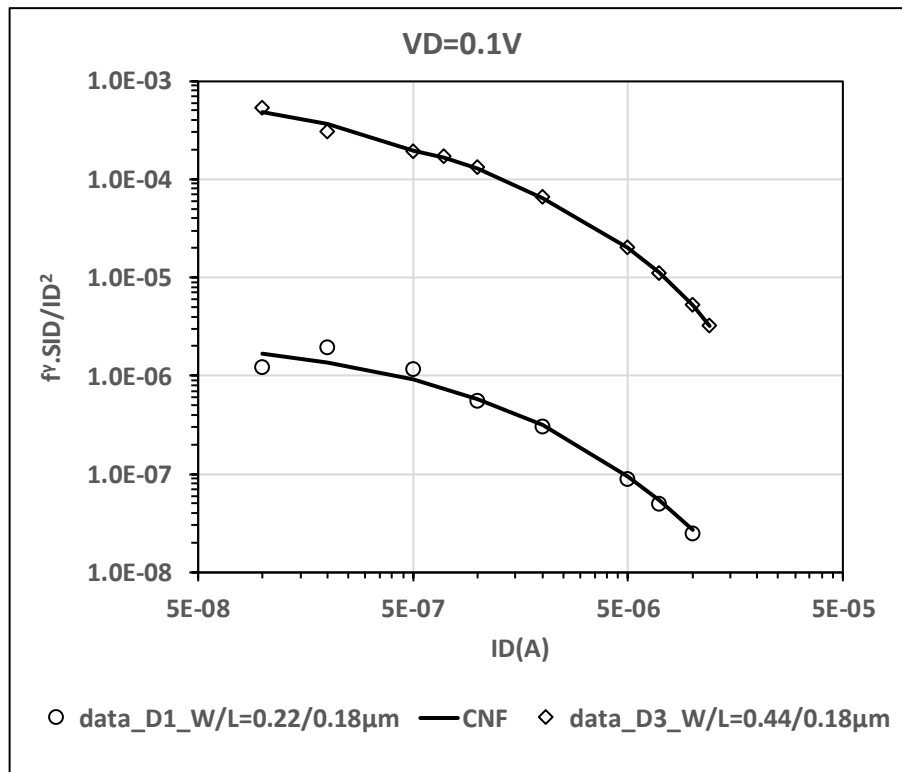


Fig. 4

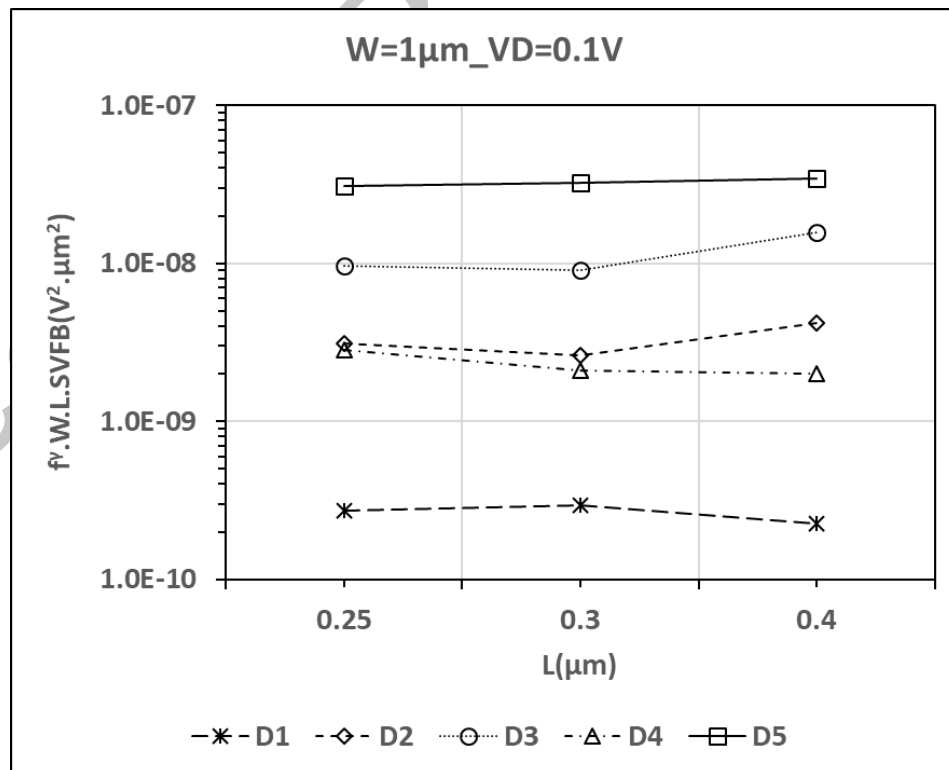


Fig. 5

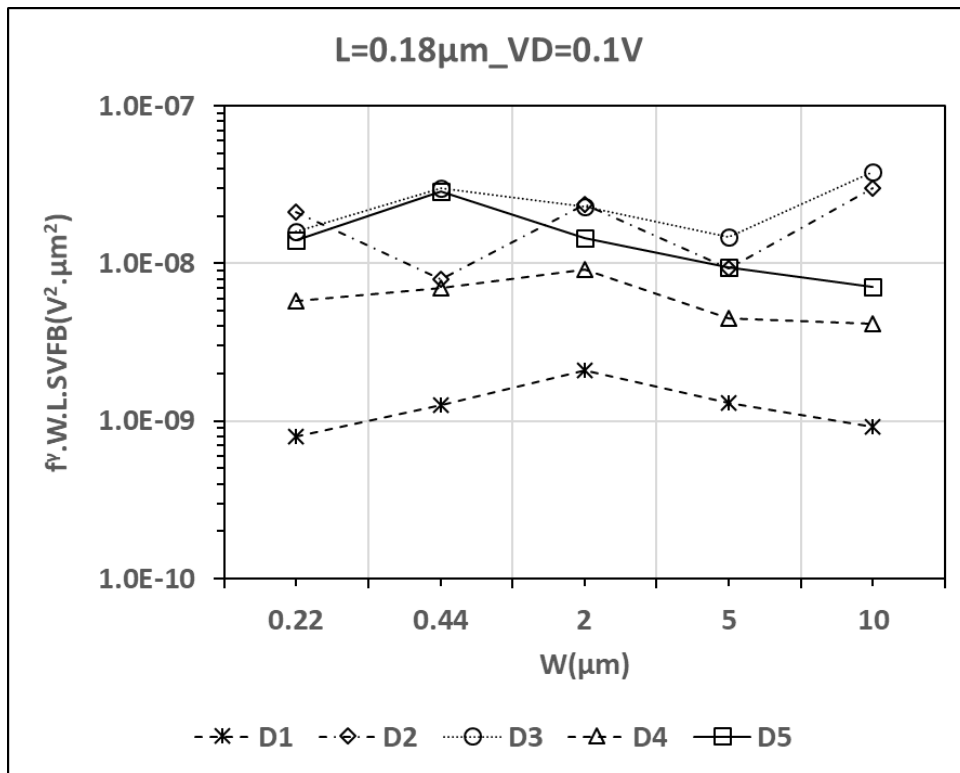


Fig. 6



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**Highlights:** This paper investigates the impact on low frequency noise of n-MOSFET dedicated for memory applications. We analyze the impact of different gate oxide thickness and LDD composition in source/drain side on LFN performance.

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