Solid State Electronics 146 (2018) 50–65

Contents lists available at ScienceDirect

Solid State Electronics

journal homepage: www.elsevier.com/locate/sse

Invited Review

Digital and analog TFET circuits: Design and benchmark

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ARTICLE INFO

The review of this paper was arranged by Prof. S. Cristoloveanu

Keywords:
Tunnel-FET
TCAD
Simulation
Digital circuits
Analog circuits

ABSTRACT

In this work, we investigate by means of simulations the performance of basic digital, analog, and mixed-signal circuits employing tunnel-FETs (TFETs). The analysis reviews and complements our previous papers on these topics. By considering the same devices for all the analysis, we are able to draw consistent conclusions for a wide variety of circuits. A virtual complementary TFET technology consisting of III-V heterojunction nanowires is considered. Technology Computer Aided Design (TCAD) models are calibrated against the results of advanced full-quantum simulation tools and then used to generate look-up-tables suited for circuit simulations. The virtual complementary TFET technology is benchmarked against predictive technology models (PTM) of complementary silicon FinFETs for the 10 nm node over a wide range of supply voltages (V_{DD}) in the sub-threshold voltage domain considering the same footprint between the vertical TFETs and the lateral FinFETs and the same static power. In spite of the asymmetry between *p*- and *n*-type transistors, the results show clear advantages of TFET technology over FinFET for V_{DD} lower than 0.4 V. Moreover, we highlight how differences in the I-V characteristics of FinFETs and TFETs suggest to adapt the circuit topologies used to implement basic digital and analog blocks with respect to the most common CMOS solutions.

1. Introduction

After the initial report in [1], complementary-metal-oxide-semiconductor (CMOS) transistors based on band-to-band-tunneling (BtBT), usually referred to as Tunnel-FETs (TFETs), have been extensively explored as possible replacements of, or complements to, conventional MOSFETs for low-power/low-energy electronic circuits targeting a supply voltage V_{DD} below 0.5 V [2–5]. TFETs embody a promising small slope FET concept able to achieve a subthreshold swing (SS) below the 60 mV/dec room temperature limit of conventional MOSFETs, as demonstrated by many theoretical works based on simulations (see [5] and references therein), and by some recent encouraging experimental results [6,7]. The lower SS compared to a conventional MOSFET can be exploited in two ways: if the threshold voltage is the same as in the MOSFET, the TFET will have a lower off-current (and thus lower static energy dissipation); if instead the same off-current is set in both devices, the TFET will be able to deliver a similar on-current as the MOSFET at a lower supply voltage V_{DD}, thus reducing both static and dynamic energy dissipations (which are proportional to V_{DD} and V_{DD}^2, respectively). In this respect, circuit simulations have attributed to TFETs the potential to outperform conventional MOSFETs in the ultra-low voltage domain ($V_{DD} < 0.4$ V) in both analog [8–10] and digital [11–17] applications. At higher supply voltages, however, the drive current of TFETs is significantly lower than the one of conventional MOSFETs. It is thus clear that TFETs can outperform MOSFETs only if they can deliver an SS significantly smaller than 60 mV/dec over a large current range in the subthreshold region. In many experiments this target has not been achieved, which may be due to fundamental as well as to material and device design issues [18–24]. As a result, the performance of the fabricated TFETs lags behind the optimistic figures reported in simulation studies, but experimental results have been steadily improving along the years. Another intrinsic advantage of TFETs over conventional MOSFETs stems from the lower temperature dependence of BtBT compared to thermionic emission [56], which may directly translate in less temperature sensitivity of TFET circuits. This has not been observed in early experimental reports about TFETs mainly because the conduction at very low current levels was often dominated by *Trap-Assisted-Tunneling* (TAT) and *Shockley-Read-Hall* (SRH) recombination processes [25]. Nevertheless, the fabrication process for TFETs is also getting more and more controlled and encouraging variability analysis are being reported both for statistically meaningful experimental samples [26], and for simulation based studies [27,28].

Among the possible technological platforms, silicon/silicon-

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https://doi.org/10.1016/j.sse.2018.05.003
Received 24 April 2018; Accepted 21 May 2018
Available online 26 May 2018
0038-1101/

germanium TFETs have the advantage of easy integration with mainstream CMOS [25,26,29,30]. However, the achieved performance is not very rewarding, especially for *n*-type TFETs, due to fundamental limit set by the indirect band-gap. As opposite to Si-based devices, TFETs based on heterojunction III-V structures are more promising [6,7,31,32] since they take advantage on their direct (and smaller) energy gap, and in fact they have shown higher on-current as well as SS below 60 mV/dec in the low current range. In addition, III-Vs provide more degrees of freedom for creating hetero-junctions and reduce ambipolar behavior.

The on-current and SS value are not the only important parameters to assess the possible advantages of TFETs against MOSFETs. TFETs are known to have a higher gate-drain capacitance [33], which can result in a switching time penalty compared to MOSFETs due to the Miller effect. On the other hand, the output conductance is lower due to the different electrostatics compared to MOSFETs [8]. Consequently, it is very important and timely to analyze the possible employment of TFETs in relevant benchmarking circuits. The fabrication processes for TFETs are however not as mature as for conventional CMOS transistors, and there exist very few reports about fabrication of TFET circuits (inverters in [25,34], current mirrors in [35], half-SRAM cell in [36]), in many cases employing transistors that are not at the state-of-the-art of TFETs and that are based on silicon platforms.

To assess the possible advantages of TFETs versus advanced CMOS transistors in realistic circuits, many simulation works have been presented. Most of such efforts have been devoted to digital circuits. SRAMs, for example, have been analyzed by various authors using different models for the TFETs either calibrated against experimental silicon devices [37] or obtained from full-quantum simulations [38]. Various SRAM topologies to circumvent the unidirectional conduction and/or to improve the cell stability have been also proposed [39–46]. Full-adders have been analyzed in [47–49] using look-up-tables (LUTs) obtained from TCAD simulations and calibrated against full-quantum results for hetero-junction complementary TFETs [50]. Level shifters have been also recently addressed in [50,51].

As for analog circuits, an operational transconductance amplifier (OTA) has been studied in [52], while a 6-bit successive approximation register (SAR) analog-to-digital-converter (ADC) has been simulated in [53] considering complementary double-gate GaSb-InAs hetero-junction TFETs. A thorough investigation in [54] analyzed mm-wave low noise amplifiers, oscillators, mixers, rectifiers and detectors using Verilog-A models for the hetero-junction GaSb-InAs TFETs presented in [55]. OTAs, current mirrors and track-and-old circuits based on InAs and GaSb/InAs TFETs have been analyzed in [8] using LUTs built from TCAD simulations calibrated on the device characteristics of [28,32]. Basic analog building blocks (current mirrors, differential pairs, diode-connected transistors) have been simulated in [56] using compact models calibrated on experimental strained silicon TFETs, proposing the deployment of TFETs in niche applications exploiting the lower temperature sensitivity. The performance of track and hold and comparators based on complementary heterojunction TFETs has been assessed in [9]. Different topologies of TFET-based power management circuits for energy harvesting applications have been proposed in [10,57]. Low-dropout linear voltage regulators with III-V TFETs have been analyzed in [58]. In most of these works, the characteristics of the *p*-TFETs are obtained by mirroring the ones of the *n*-TFETs.

In this paper, we present a comparison between aggressively scaled template heterojunction TFETs and FinFETs considering a wide variety of digital and analog/mixed-signal building blocks. The characteristics of the TFETs have been derived from full-quantum simulations [59], where *n*-TFETs and *p*-TFETs have been separately designed and have their own individual characteristics. This work reviews and extends previous publications from our group [9,37,47,48,51] by using the same set of devices for a large variety of circuits and supply voltages, and drawing more general conclusions. Furthermore, differently from the previous papers, the comparison with silicon FinFETs is carried-out at fixed occupied area and absolute off-current, hence essentially at the same static power.

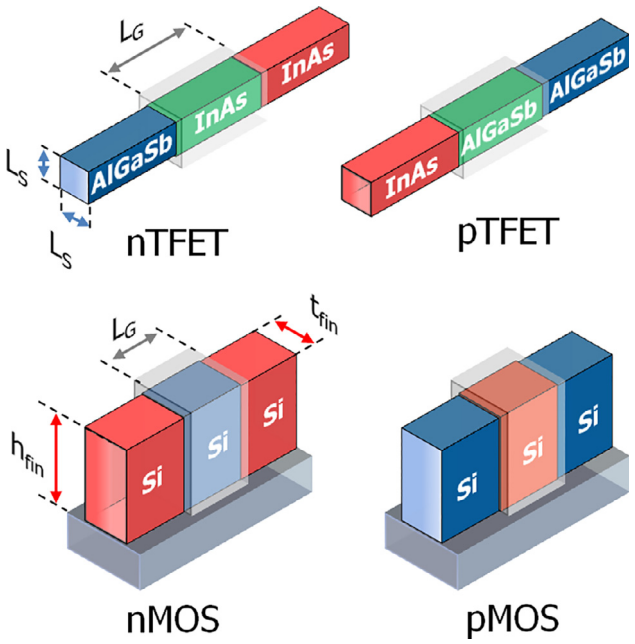

Fig. 1. Sketch of *n*- and *p*-type TFET and FinFET device architectures. The red and blue colors indicate the n- and p-doping types, respectively (green: intrinsic semiconductor, transparent-grey: oxide). TFET dimensions are: L_G = 20 nm, nanowire cross section (L_S) = 7 nm, EOT = 1 nm. FinFET dimensions are: L_G = 14 nm, t_{fin} = 8 nm, h_{fin} = 21 nm, EOT = 0.88 nm. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

The paper proceeds as follows. The devices and the simulation methodology are described in Section 2. Simulation results for digital building blocks such as inverters, full-adders, SRAM cells and level shifters are reported in Section 3. Analog/mixed-signal building blocks (op-amps, current mirrors and comparators) are analyzed in Section 4. Conclusions are drawn in Section 5.

2. Virtual technology platforms and methodology for simulation and benchmarking

The geometric structures of the *p*/*n*-type nanowire (NW) TFETs and silicon FinFETs considered in the following of this work are shown in Fig. 1. The considered TFETs belong to the complementary virtual technology in [59], designed and characterized by means of full-quantum simulations. In particular, the AlGaSb/InAs NWs TFETs have a square cross section with a side L_S = 7 nm, a gate length L_G = 20 nm, and an equivalent oxide thickness EOT = 1 nm (with a physical oxide thickness of 2.3 nm by considering Al_2O_3 gate oxide [59]). The FinFET technology used as a benchmark was obtained via the PTM for 10 nm node FinFETs, available at [60]. There are two flavors of such a 10 nm node PTM-FinFETs targeting two different application domains: high-performance (HP) and low-standby-power (LSTP), the latter being the one selected for our analysis. FinFETs have fin height h_{fin} = 21 nm, fin width t_{fin} = 8 nm, L_G = 14 nm and EOT = 0.88 nm (physical oxide thickness of 1.2 nm [60]). As for the electrical characteristics, at the nominal V_{DD} of 750 mV, the n- and the p-FinFET feature a threshold voltage V_{th} of 425 mV and −428 mV, a saturation on-current I_{ON} of 44 μA and −39.5 μA, and an off-current I_{OFF} of 5.13 pA and −5.08 pA, respectively. Despite the different geometry, the benchmark is fair since the two architectures occupy almost the same area on the wafer under the assumption of having vertical TFET NWs (see for example [7]) and conventional lateral FinFETs. In fact, the physical footprint of a vertical TFET is a square with a total side of 11.6 nm (area ~135 nm^2), considering the semiconductor wire and the surrounding Al_2O_3 gate oxide.

Table 1
Calibrated parameters used in the TCAD simulations of the AlGaSb/InAs TFET templates.

Parameter	$Al_{0.05}Ga_{0.95}Sb$	InAs
Band-gap parameters (including quantization effects)		
Energy gap E_G (eV)	1.04	0.59
Electron affinity χ (eV)	4.01	4.9
Dynamic non-local BtBT model parameters		
A_{path} ($cm^{-3}\,s^{-1}$)	$1.51{\cdot}10^{20}$	$1.44{\cdot}10^{20}$
B_{path} (V/cm)	$9.54{\cdot}10^{6}$	$2.94{\cdot}10^{6}$
Effective conduction and valence band density of states		
N_C (cm^{-3})	$1.26{\cdot}10^{18}$	$5.22{\cdot}10^{17}$
N_V (cm^{-3})	$1.8{\cdot}10^{19}$	$6.6{\cdot}10^{18}$

As for a FinFET, the resulting footprint area is $\sim 145\,nm^2$, by considering the fin cross section side of 10.4 nm (represented by the channel thickness and the wrapped gate oxide) and $L_G = 14$ nm.

As extensively described in [47,48], the TFETs have been simulated using the TCAD tool Sdevice [61], where the model parameters have been adjusted to reproduce the full-quantum results in [59], which were performed at room temperature. In fact, due to over-simplified models available in commercial TCAD to account for the effects of quantum confinement, the default model parameters are not adequate. Thus, the band-gap parameters for the InAs/AlGaSb heterostructure, i.e. the energy-gap (E_G) and the electron affinity (χ), have been chosen so as to reproduce the same band alignment as in [59]. Then, the dynamic nonlocal-path BtBT model parameters for the direct tunneling process ($A_{path,dir}$ and $B_{path,dir}$, see [61]) were recalculated by using the effective masses from bulk GaSb and InAs. Finally, the effective valence and conduction band density of states (N_V and N_C) have been increased compared to the default value for bulk crystals to improve the matching of the I-V curves between TCAD and full-quantum results. The calibrated parameters are summarized in Table 1; one should note that these parameters may be interpreted as a fitting deck allowing to reproduce room temperature full-quantum results, while the TCAD predictivity at different temperatures has not been proved due to lack of high temperature simulations in [59]. Our analysis is thus limited to room temperature and does not explore possible advantages of TFETs due to better temperature stability.

Fig. 2 shows the device I_D-V_{GS} characteristics. The comparison has been performed by aligning both *n*- and *p*-type TFETs transfer-characteristics at the same off-current ($I_{OFF} \sim 2$ pA) as for the FinFETs at $|V_{DS}| = 0.3$ V (note that all the forthcoming figures will be consistent with this shift, if not otherwise stated). This threshold-voltage alignment is possible by assuming a metal gate work-function of 4.86 eV and 5.03 eV for the p- and n-TFET, respectively. In real devices, both work-functions might be achieved by using a TiN metal gate. This would be possible thanks to the tunability of the TiN work-function [62,63], and considering that the tunable range is between 4.85 and 5.2 eV for a TiN/Al_2O_3 gate stack [64]. Note that we considered the same absolute I_{OFF} without normalization because the two architectures have very similar footprint. This ensures similar static power for TFETs and FinFETs, although likely different cell layouts when considering lateral and vertical devices may result in different circuit areas.

While the I_D-V_{GS} characteristics of *p*- and *n*-type FinFET in Fig. 2 are essentially symmetric at low voltage levels due to similar electrostatics (and SS) and matched I_{OFF} (the electron/hole mobility difference does not imply a mismatch between the n-/p-type I_D in the subthreshold region), the I_D-V_{GS} curves of TFETs are strongly asymmetric. In fact, the design of both p- and n-type TFETs encounters significant criticalities. Due to low density of states (DOS) in the conduction band of III-V materials leading to a degeneracy at relatively low doping levels, the source of the p-TFET cannot be heavily doped in order to preserve a steep SS, but this tends to limit the corresponding maximum on-current [65]: as a result, the *p*-type TFET has four times smaller on-current compared to the *n*-type device. As regards to the *n*-TFET, it suffers from a larger ambipolarity compared to the *p*-TFET. This is due to smaller band-gap of the channel/drain material of the n-TFET (InAs) than the one of the p-TFET (AlGaSb), see Table 1, which is more prone to unwanted BtBT at the drain side. Furthermore, this also favors the kink at low V_{GS} in the n-TFET that is due to a direct tunneling path between the source and the drain. This tunneling path is weakly controlled by the gate and dominates the current until the source-to-channel tunneling starts to dominate.

Fig. 3 compares the I_D-V_{DS} characteristics of the devices (with the same threshold-voltage), showing that both *p*/*n*-type TFETs have a better saturation compared to FinFETs. This conduction is shown only for $V_{DS} > 0$ ($V_{DS} < 0$), while for the opposite polarization a forward biased p-i-n diode-like behaviour takes place (see [36,37] for further details). Fig. 4 reports the total gate capacitance (C_{GG}), which is the sum of the gate-to-source (C_{GS}) and gate-to-drain (C_{GD}) capacitances. Note that the PTM-FinFET models include an extrinsic capacitance of about 30 aF equally split between the C_{GS} and C_{GD} contributions. For a fair comparison, the same absolute extrinsic capacitances have been added to the C_{GS} and C_{GD} extracted from TCAD simulations of the TFETs. It should be noted that the real parasitic capacitance – which can be estimated only after assuming a circuit layout – might be much larger. However, this estimation is beyond the scope of this work since it would require technology parameters and design-rules to be predicted (some effort in this sense has been done in [66,67]). Rather, our main aim is to consider intrinsic devices to focus on more fundamental aspects. In any case, we believe that including at least the contribution already present in the PTM is needed to get not excessively optimistic results.

The I-V and C-V curves for the TFETs simulated with the calibrated TCAD simulation deck are then used to generate dense LUTs for I_D, C_{GS},

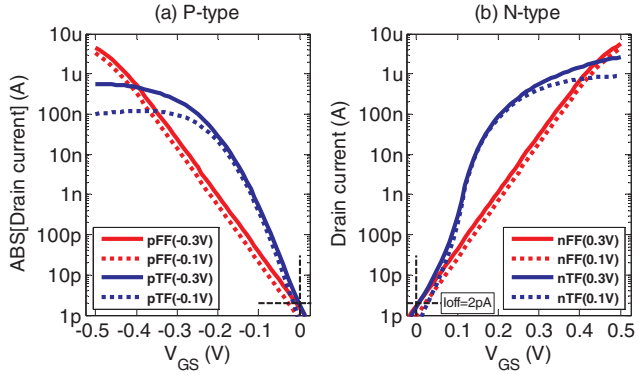

Fig. 2. (a) *p*-type and (b) *n*-type transfer-characteristics (I_D-V_{GS}) at $|V_{DS}| = 0.1$ V and 0.3 V of single FinFET (FF) and TFET (TF) devices, aligned at $I_{off} \sim 2$ pA at $V_{DD} = 300$ mV.

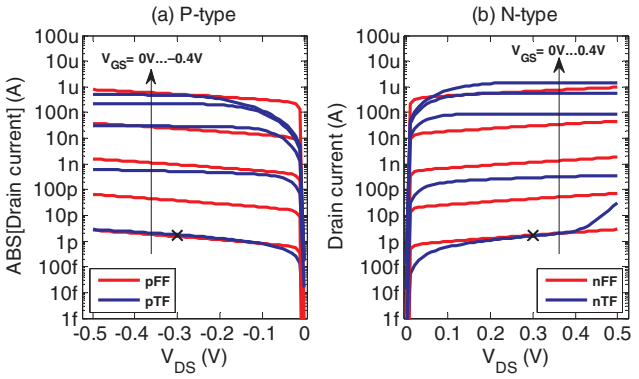

Fig. 3. (a) *p*-type and (b) *n*-type device output-characteristics (I_D-V_{DS}) at $|V_{GS}| = 0$ V, 0.1 V, 0.2 V, 0.3 V, 0.4 V.

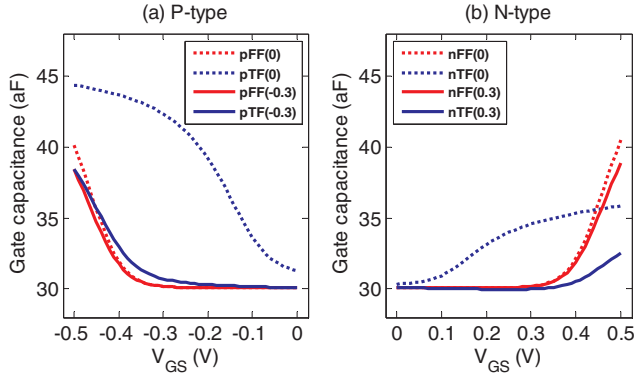

Fig. 4. (a) *p*-type and (b) *n*-type device gate-capacitance characteristics (C_{GG}) as a function of V_{GS} at $|V_{DS}| = 0$ V and 0.3 V.

and C_{GD} as a function of V_{GS} and V_{DS}. These LUTs are then imported in the Cadence Virtuoso environment by means of the Verilog-A description language thus enabling circuit simulations. For the FinFETs instead, we used directly the SPICE models in [60].

As a general remark, we want to point out that the device models used in this work do not include traps and other defects related to immature fabrication processes, and this means that we are considering a "virtual" technology where small SS can be achieved. On the other hand, NEGF simulations in [59] are quite accurate to describe the tunneling mechanisms at the base of the TFET behavior. This means that the virtual technology considered here is representative of something that is not available today, but that is not unrealistic because it requires an evolutionary improvement to devices which can be fabricated today. Thus, we would like to stress that the results reported in the following of this paper are not restricted to the specific template devices employed here. In this regard, Fig. 5 compares the IV characteristics of the template TFETs used in this work (taken from [59]) and the ones used for other benchmarking activities based on simulations [14,65,68]. We see that all nTFETs feature quite similar characteristics. The same applies to the pTFETs, except for the one in [68] that appears to be the mirrored version of the nTFET. One should also note that the small differences among the reported devices depend on how the normalization of the current is performed (e.g. the I_D of our devices has been normalized by the nanowire perimeter, while the current of the other devices is already normalized since they are obtained by 2D simulations). Furthermore, the I_D-V_{GS} for the InAs homojunction device in [65] is reported for a lower V_{DS} than the others ($|V_{DS}| = 100$ mV against 300 mV).

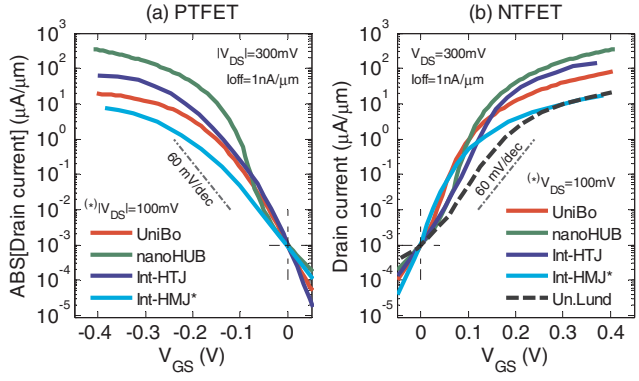

Fig. 5. (a) *p*-type and (b) *n*-type transfer-characteristics (I_D-V_{GS}) at $|V_{DS}| = 300$ mV of virtual *p*-/*n*-TFETs presented in [59] (UniBo, devices used in this work), of the template used in [68] (nanoHUB), the templates in [14] (Intel-HTJ), [65] (Intel-HMJ, at $|V_{DS}| = 100$ mV) and of the experimental *n*-TFET in [7] (Un.Lund). For a fair comparison, the I_D-V_{GS} characteristics have been normalized by the gate perimeter and aligned at the same $I_{off} = 1$nA/μm.

In addition, Fig. 5 reports also the experimental IV of the nTFET presented in [7]: the SS and on-current are worse than in the idealized TFETs used in this work and in [14,68]. However, a detailed TCAD-based analysis of these experimental results has shown that there is still room for material and device optimization [69], which may improve SS and enable a ten times improvement of the on-current, that would make it close to the current of our template devices. This is an indication that TFETs with performance similar to the simulated devices of this work may be manufacturable within a reasonable time frame.

3. Analysis of digital circuits

The circuit-level benchmarking analysis reported in this section focuses on basic digital building blocks implemented with TFETs. Starting from simple inverter logic-gates, we delve into the details of the design of TFET digital circuits, with emphasis on how the TFET specific characteristics influence the operation and performance of some relevant building blocks. These include complementary arithmetic circuits such as the standard *28 T full-adder* in Section 3.1, access-transistor based memory cells, such as the *Static-RAM* (SRAM) in Section 3.2, and hybrid (i.e. comprising both FinFET and TFET devices) digital voltage conversion blocks such as the level shifters in Section 3.3.

Independent *inverter* gates, together with *fan-out* 4 (FO4) inverters and *5-stage ring oscillators* (RO5), are conventionally representative benchmarks to assess the static and dynamic performance of emerging device technologies for digital applications. In Fig. 6a, the voltage transfer characteristics have been reported for both minimum size TFET and FinFET inverters at $V_{DD} = 300$ mV. As suggested by the drain current characteristics of *n*/*p*-type devices in Fig. 2 and Fig. 3, the asymmetry is more pronounced for the TFETs, whose inverter logic threshold is below $V_{DD}/2$ (i.e. 150 mV in this case), because the *p*-TFET is weaker than the *n*-TFET. This fact is further illustrated by Fig. 6b that reports the inverter static noise margins as a function of the *p*-type to *n*-type device ratio, considering that a ratio close to 4/1 is needed to compensate for the resulting asymmetry between the NML and NMH (Noise Margins at the Low and High digital levels, respectively) of the TFET inverter, in agreement with the factor of 4 in on-current between *n*-TFETs and *p*-TFETs (Fig. 2). In any case, the unbalance between the on-current in n- and p-type TFETs leads to a much reduced effect in the NML and NMH than in our previous report [47] since we consider here $V_{DD} = 300$ mV instead of 400 mV. At this bias, the current of the *p*-TFET is closer to the one of the *n*-TFET than at 400 mV. In Fig. 5a we see that the voltage gain at the logic threshold is larger in TFET inverters thanks to the higher output resistance (Fig. 3).

Low-to-high (L → H) and high-to-low (H → L) FO4 delays are plotted as a function of V_{DD} in Fig. 7. Unlike FinFETs, which have essentially symmetric I-V electrical characteristics for *n*- and *p*-type

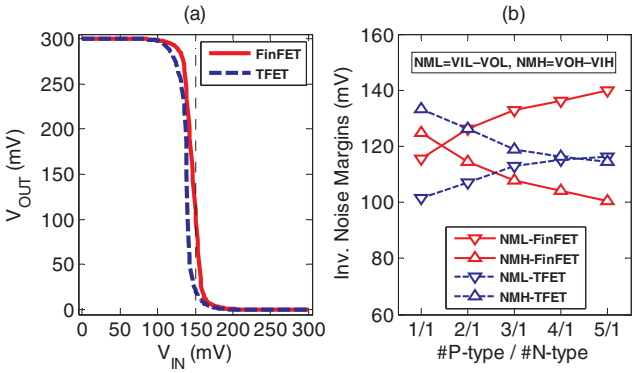

Fig. 6. (a) Voltage-transfer-characteristics (VTC) for minimum size FinFET and TFET inverters. (b) Inverter static noise margins (NML and NMH) as a function of the inverter *p*-type/*n*-type device ratio.

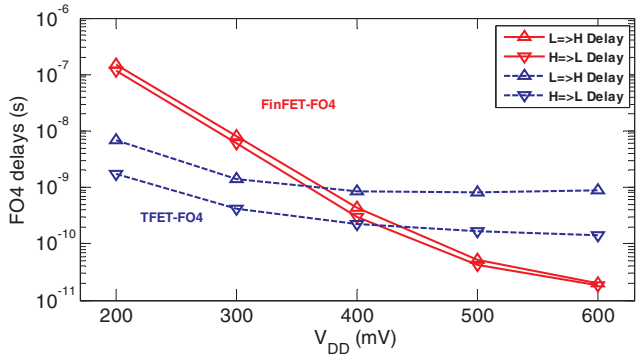

Fig. 7. Low-to-high and high-to-low delays as a function of V_{DD} for FinFET and TFET Fan-Out 4 (FO4) minimum-size inverters.

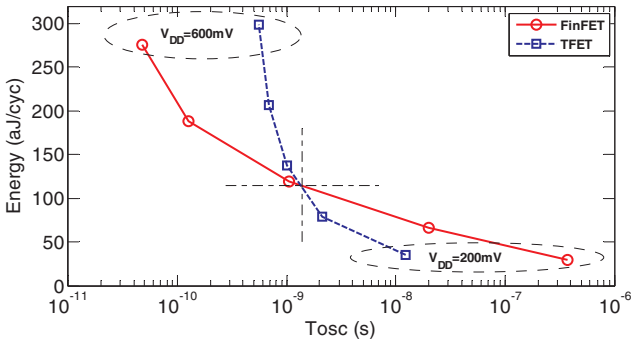

Fig. 9. FinFET vs TFET benchmark based on the Energy vs. T_{osc} plot for minimum size 5-stages Ring Oscillators (with *fan-out* 1). The single points on the curves are obtained for different V_{DD}s (steps of 100 mV).

devices and thus symmetric voltage-transfer-characteristics (VTC), asymmetric electrical characteristics of TFETs result in asymmetric rise and fall transitions. Despite such asymmetry, the TFET FO4 delay is shorter than for the FinFET case for V_{DD} below ~370 mV (~410 mV) if we consider the rise (fall) edge. Furthermore, one should consider that TFET FO4 suffers from Miller effect due to large C_{GD}, but this does not impede the TFETs to become faster than FinFETs at reduced V_{DD}s, in accordance with their larger on-current and to the fact that the average gain of a logic gate is ~2. Note that C_{GD} also produces significant overshoots in the voltage waveforms [48].

As for the ring-oscillator, we have extracted and examined the oscillation frequency (T_{osc}^{-1}) and the energy per cycle. T_{osc} is correlated with the critical path delay of a generic logic circuit, representing a limit for its maximum operating frequency, whereas the energy per cycle is in turn correlated with the energy per operation (E_{op}) when the same digital circuit is operated at the maximum frequency. In Fig. 8, we show in (a) the oscillation period (T_{osc}) and in (b) the energy per cycle, as a function of the inverter *p*-type/*n*-type device ratio. From this plot it is clear that, although symmetric TFET drive-currents improve noise margins, having a small total capacitance (hence a 1/1 ratio) is preferable from a performance and energy consumption perspective. In Fig. 9, energy versus T_{osc} points, as extracted for various V_{DD} in the range 200–600 mV (step 100 mV), are plotted for both TFET and FinFET ring-oscillators, showing that for time-relaxed applications, the TFETs offer an energy budget saving, which in this case occurs for $T_{osc} > 1.5$ ns and for energy below 100 aJ/cycle. If we focus on the ultra-low V_{DD} (e.g. close to 200 mV), there is a very large gain in T_{osc} for a fixed energy (with a factor > 20 at 30 aJ/cycle energy), while the advantage in terms on energy per cycle for a given T_{osc} is less relevant (with a factor of ~2 for a T_{osc} = 1 ns). The larger current of TFET at low V_{DD} explains the much smaller propagation delay. On the other hand, the capacitances are quite similar in TFETs and FinFETs (slightly larger for TFETs). As a result, the dynamic energy is almost the same for a given V_{DD}, with second order differences due to different capacitance and static energy (the same static power gets integrated over different T_{osc}).

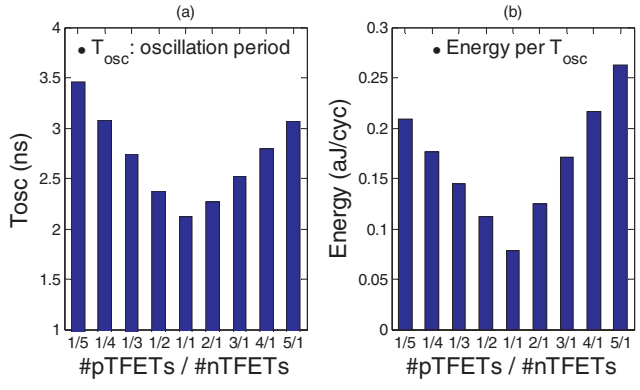

Fig. 8. TFET 5-stages Ring-Oscillator (RO5) with *fan-out* = 1 (i.e. all the inverters in the chain are the same): (a) oscillation period (T_{osc}) and (b) Energy per cycle as a function of the inverter *p*-type/*n*-type device ratio.

When considering the maximum clock frequency at which a logic-chip can operate, it should be noted that this could be up to 100 times slower than the one extracted for the RO ($f_{osc} = T_{osc}^{-1}$). This means that the frequency range where it would be convenient to use TFETs in place of FinFETs is limited to ~MHz levels and below, as it will be discussed in the next sections. In conclusion, considering that the low SS of TFETs makes them advantageous in the sub-threshold regime, the target applications are the ultra-low-voltage circuits, typical in Internet-of-Things end-nodes [70], which indeed trade the very low power dissipation with low speed.

3.1. Full-Adder circuits

Full-adders are fundamental building blocks of many digital systems. To analyze such circuits, transient simulations were performed with a dedicated test-bench on both TFET and FinFET single-bit full adder solutions. To provide a simulation environment with realistic driving signal and loads, the full-adder under test has been placed in a framework including other full-adders and inverters as circuital periphery, as extensively discussed in our previous paper [48]. The extracted delays and energy characteristics are post-processed and translated into figures-of-merit for multi-bit ripple-carry-adders. Trends related to the FinFET and TFET designs are presented and discussed in this section.

The transistor level schematic of the standard and mirror 28T full-adder topologies are reported in Fig. 10 (TFET implementations only). In the mirror topology, the pull-up and pull-down networks are identical rather than complementary [71]. This reduces the current path from 3 to 2 p-type transistors in the carry, and from 4 to 3 p-type transistors in the sum circuit. In particular, due to the asymmetric current conduction of the TFETs, in complementary logic circuits the TFETs are connected so that *n*-type and *p*-type devices have respectively a positive and negative V_{DS}. This configuration prevents the forward biasing of the p-i-n junctions for both *n*- and *p*-TFETs.

Fig. 11 reports the propagation delays of the TFET and FinFET full-adders. The TFET adder shows less speed degradation when V_{DD} is reduced compared to the FinFET design; this allows the TFET solutions to become faster than its FinFET counterparts for V_{DD} below ~400 mV. Furthermore, by comparing the results for the mirror topology against the standard one, we see more advantage in terms of propagation delay for the TFET implementation (around 3.5% improvement), while for FinFETs the improvement is around 0.6%. This can be explained considering that the dominant delay is associated to the pull-up chain generating $\overline{Co}$, with a higher performance benefit for the TFET adder

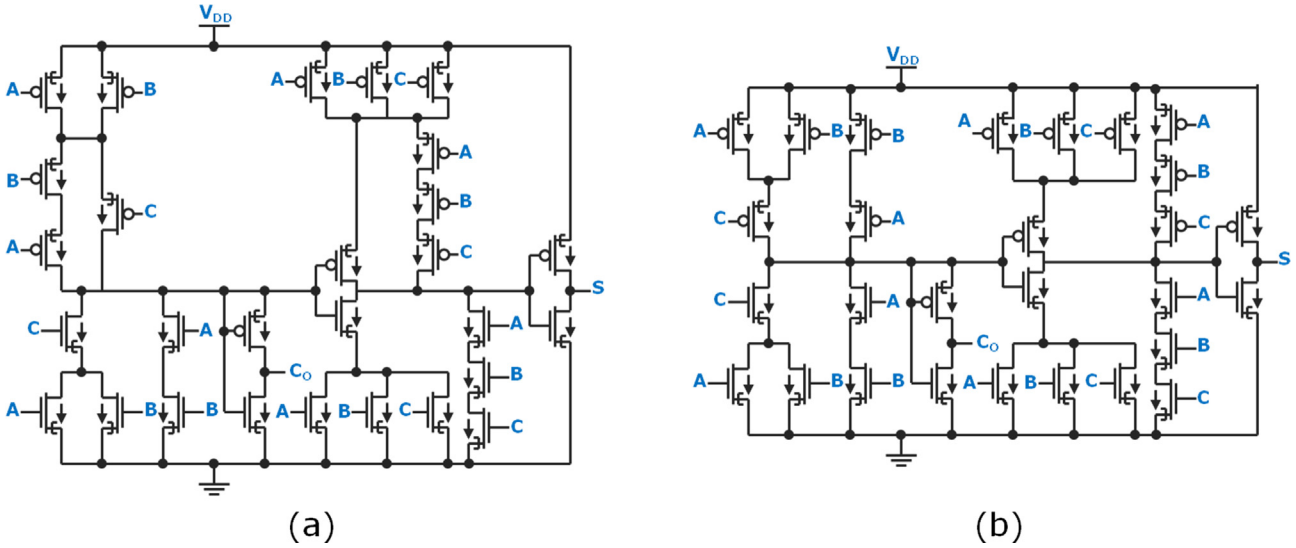

Fig. 10. Schematic of a standard (a) and mirror (b) 28 T full adder circuits. Source of the TFETs are marked.

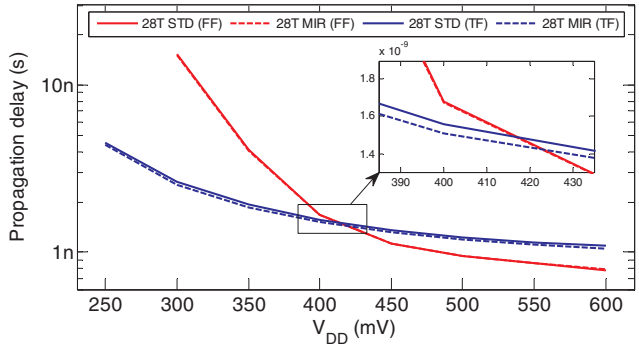

Fig. 11. Propagation delay of 28 T (standard, STD, and mirror, MIR) single-bit full-adders.

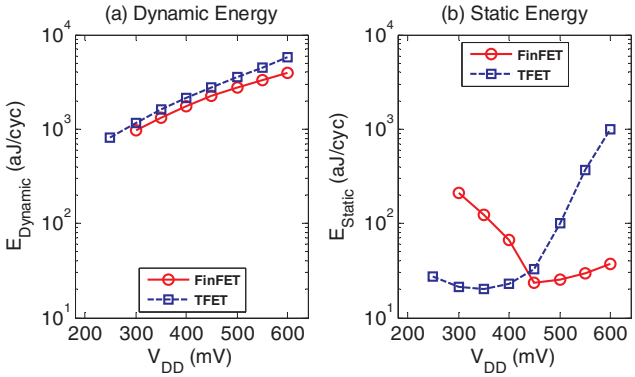

Fig. 12. (a) Dynamic and (b) Static Energies per minimum clock cycle ad a function of V_{DD} for 32-bit Ripple-Carry-Adders.

due to p-/n-device asymmetry.

Besides the obvious consequence that TFET circuits can operate at a higher clock frequency for such reduced V_{DD}, the smaller speed degradation with V_{DD} scaling with respect to FinFETs has also implications from the energy point of view. In fact, in the energy balance of a circuit, both static and dynamic energy components can be relevant. In particular, at high V_{DD} values, the dynamic energy per cycle ($E_{dynamic} = \alpha \cdot C_{L,eq} \cdot V_{DD}^2$, where α is the activity and $C_{L,eq}$ is the equivalent capacitive load of the circuit) is dominant. On the other hand, when the V_{DD} is scaled down, a longer T_{CLK} is needed to accommodate the larger delays, so that the static energy component ($E_{Static\ per\ cycle} = T_{CLK} \cdot V_{DD} \cdot I_{leak}$) can become dominant at lower switching activity. In this regard, it appears clear that having a reduced delay degradation with V_{DD} scaling would result in reduced static energy consumed per each operation, for the same static power.

Fig. 12 reports the estimated (a) dynamic and (b) static energy per cycle for 32-bit ripple-carry-adders (RCA), each corresponding to 32 blocks of the 28 T standard topology in Fig. 10a, with either TFETs or FinFETs. The total energy per cycle for TFET and FinFET 32-bit RCAs is reported in Fig. 13, by considering various conditions for the activity factor, which is defined as the ratio between the effective input/output switching events and the total clock cycles. When a switching activity close to 1 is considered, the dynamic energy dominates over the static one. Thus, irrespective of the operating voltage, the energy consumption of the FinFET circuit is slightly lower than the one needed for the TFET one. This is due to larger gate capacitance of TFET devices (see Fig. 4): in fact, although the same extrinsic capacitance has been

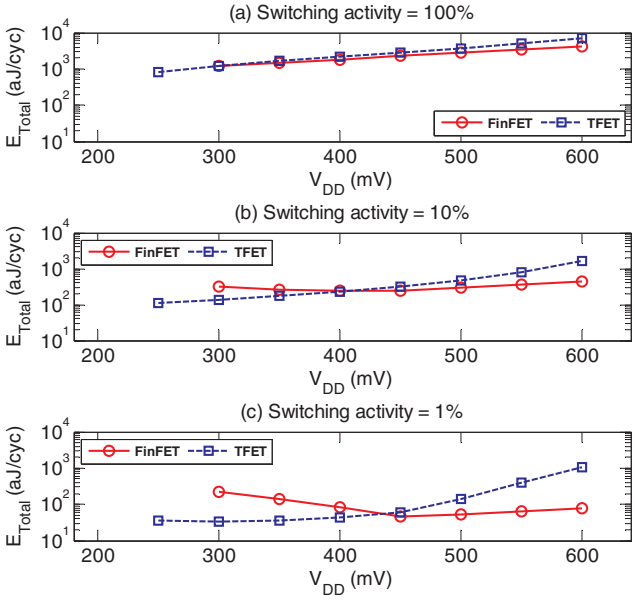

Fig. 13. Total Energy (Static + Dynamic contributions) as a function of V_{DD} for 32-bit Ripple-Carry-Adders, considering a switching activity equal to (a) 100%, (b) 10% and (c) 1%.

assumed in this study and the TFET has a lower C_{ox} (due to slightly larger EOT), the TFETs have to cope with the intrinsic increase due to Miller effect [33]. On the other hand, when we move toward applications requiring a lower activity (i.e. 10% or below), the static energy contribution becomes more and more relevant in the balance against the dynamic energy. This means that the reduced static energy at lower V_{DD} for the TFET topology, as reported in Fig. 12b, directly translates into a better energy efficiency of the TFETs when low activity applications are considered.

3.2. 6T SRAM cells

The SRAM cell is widely deployed as on-chip cache in processors, due to its better read and write access times compared to other memory types. As a result, a SRAM array can occupy more than 50% of the processor area. From a topology point of view, the 6T SRAM cell contains two cross-coupled inverters to store the data, and two access-transistors (ATs), to access the data. Thus, the importance of investigating the TFET SRAM cell is twofold: (1) it allows us to benchmark the possible TFET deployment in advanced digital circuits; (2) it is an important case-study to investigate the possible shortcoming of TFET due to their unidirectional conduction.

In recent years, many groups have investigated the impact of the TFET drain current unidirectionality, by assuming conventional 6-transistor (6T) cells with either inward-faced or outward-faced ATs (the outward configuration is sketched in Fig. 14), as well as possible alternative topologies. One of the first proposal has been the asymmetric 6T cell based on one inward-AT and one outward-AT [39], which uses a kind of write-assist technique to improve the write stability. Various conditions for read and write assist protocols have been investigated in [40], with emphasis on a symmetric 6T cell with p-type inward-ATs and read-assist. Afterwards, a 7T cell based on a conventional outward-AT 6T cell and one additional transistor for the read has been proposed in [41] (the same topology has been recently re-considered in [46] by simulating a different set of TFET templates). Robust topologies with more than 6 transistors have been proposed to improve the cell stability against device variations, such as the 10T Schmitt-Trigger cells in [42,43], the 7T driverless cell in [44] and the 8T hybrid TFET/CMOS cell in [45]. The most recent proposal is the 7T cell based on unconventional connections of the ATs to the bit-lines (BLs) and word-line (WL) in [38] (source and drain of the AT connected to the WL and BL, respectively), with the purpose to improve the cell stability and reduce the minimum operating V_{DD}. In our previous report [37], we have demonstrated that the simple 6T SRAM cell can work without severe performance penalty with respect to more complex cells (e.g. the 8T cell), provided that (1) outward-ATs are used and (2) the bit-lines (BLs) are pre-charged to $V_{DD}/2$ for the read operation.

The static performance of the 6T SRAM cell is analyzed in Fig. 15, which reports the static noise margins in both read (RSNM) and write (WSNM) operations, for (a and b) FinFET and (c and d) outward-AT TFET 6T SRAM cells. These static noise margins are plotted as a function of the effective width of the AT (x-axis), of the pull-up transistor

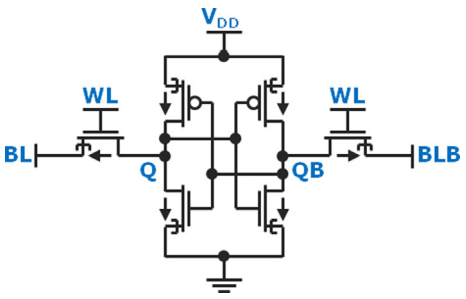

Fig. 14. Simulated 6 T SRAM cell with outward-facing TFET access transistor (TFET implementation only).

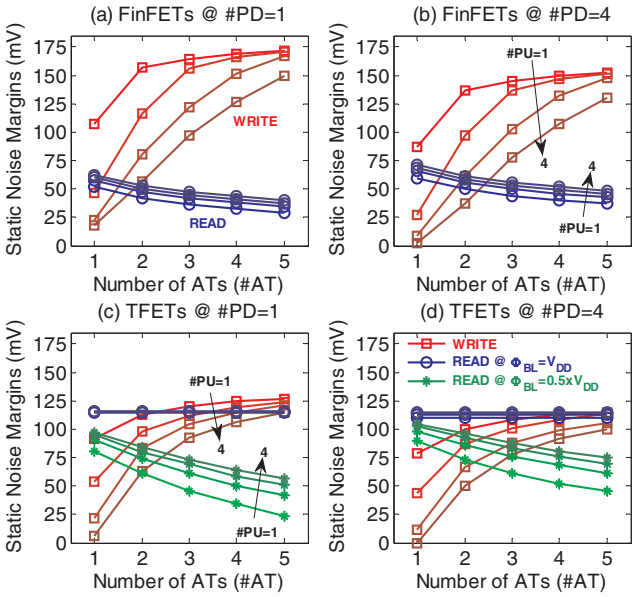

Fig. 15. Read and Write Static-Noise-Margins for (a and b) FinFET and (c and d) outward-AT TFET 6 T Static-RAM cells, as a function of the number of AT and PU devices, for #PD = 1 (a and c) and for #PD = 4 (b and d). The read is performed with a pre-charge of the BLs at either V_{DD} or $V_{DD}/2$ for the TFET cell, while for the read of the FinFET cell the BLS are at V_{DD}. The write is performed with differential voltage levels applied at the BLs (i.e. either 0 V and V_{DD} or V_{DD} and 0V applied at BL and BLB, respectively). V_{DD} = 300 mV.

(different curves in the same plot) and of the pull-down transistor (plots on the left against the ones on the right), obtained by assuming multiple parallel transistors. When considering symmetric transistors as the FinFETs (Fig. 15, a and b), the write-ability of a cell mainly improves by decreasing the pull-up ratio, defined as the ratio between the effective width of pull-up transistors and the width of the ATs. As for the read-ability, this can be mainly improved by increasing the cell ratio, which is defined as the ratio between the effective width of pull-down transistors and the width of the ATs. In a few words, a trade-off between read and write operations is required to achieve a correct sizing of an SRAM cell: the larger the ATs, the lower is the RSNM and the larger is the WSNM (see for example Fig. 15a). On the other hand, when considering unidirectional transistors as the TFETs (Fig. 15, c and d), RSNM results to be independent on the overall AT size. This fact has been already discussed in [37], with the conclusion that the read is in fact forbidden due to unidirectional conduction of outward-faced ATs, which prevents the access to the cell in read-mode (i.e. despite quite large RSNM, the corresponding read operation is too slow). For this reason, we report also the case when read is performed with a pre-charge of the BLs to $V_{DD}/2$, while keeping the standard write protocol with differential voltage levels to 0 V and V_{DD} at the two BLs. In this case, at the beginning of the read operation, the BL voltage levels are between 0 and V_{DD}, and thus at least one of the AT is operated at positive V_{DS} (i.e. the one at the side where the '1' logic value is stored), so that the BL capacitance is charged toward V_{DD} in a reasonable time. In Fig. 16, we report the (a) write and (b) read delays for both FinFET and TFET SRAM cells as a function of V_{DD}. As regards the write delay, the TFET SRAM cell becomes faster than the corresponding FinFET cell at V_{DD} below ~360 mV. A similar trend is also obtained for the read delay, where the TFET SRAM cell becomes faster at V_{DD} below ~400 mV. It is important to remark that the read of the TFET cell has been performed by pre-charging the BLs to half V_{DD}, and this makes the TFETs competitive with FinFETs at such ultra-scaled V_{DD} values, despite the unidirectionality of TFETs. As for the FinFET cell, this pre-charge scheme does not bring any significant improvement to the read delay because FinFETs are bidirectional. Read and write delay transient

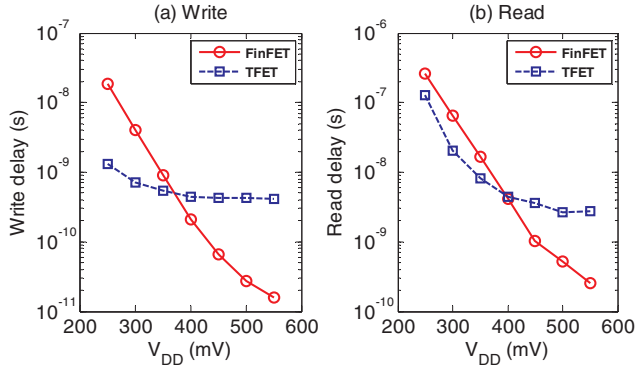

Fig. 16. (a) Write and (b) Read delays as a function of V_{DD} for FinFET and TFET SRAM cells. The read of the TFET cell is performed by assuming a BL precharge at $V_{DD}/2$. #PD = #PU = 1. #AT = 1 for FinFETs, #AT = 3 for TFETs.

simulations have been performed by assuming a BL parasitic capacitance of 20 fF, to account for interconnect parasitic capacitance as well as for input capacitances of ATs belonging to other cells in the same array.

3.3. Level shifters

Level shifter (LS) circuits are required in multi-supply voltage designs to up-convert digital signals from the lower (V_{DDL}) to the higher (V_{DDH}) power supply domain. A key requirement of this class of circuits is to perform fast and energy efficient conversion for a wide range of input voltages. In this context, a hybrid MOSFET/TFET approach has been proposed in [51] showing significant improvement over pure MOSFET and TFET designs. The same hybrid MOSFET/TFET LS application has been investigated in [50], with more focus on the layout density reduction (e.g. by using single non complementary input data signal, i.e. with a single input-stage inverter). Although the co-integration of such two technologies in the same chip would be challenging, due to different device concepts (TFET and CMOS) and different material schemes (III-V materials and silicon), some encouraging result has been already shown in the literature, such as the TFET and CMOS devices co-integrated with the same process flow in [30], as well as the hybrid integration of III–V and Si(Ge) CMOS devices in [72]. In this context, a lot of effort is being devoted to enable heterogeneous integration of very different technologies [73,74], and we may consider the further challenge to integrate vertical and lateral device architectures.

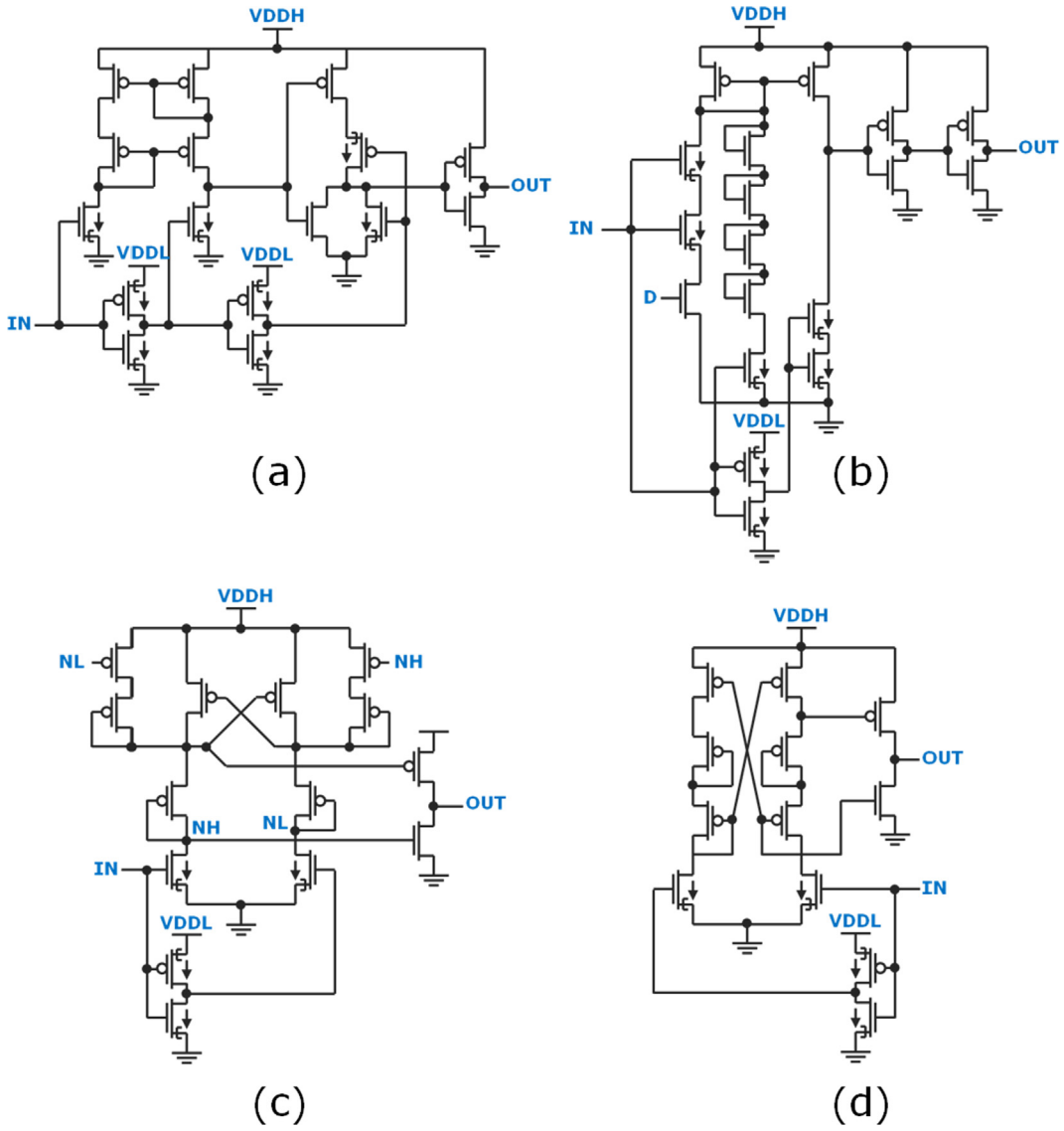

Fig. 17. Hybrid FinFET/TFET design of the level shifter topologies reported in (a) [75], (b) [76], (c) [77] and (d) [78].

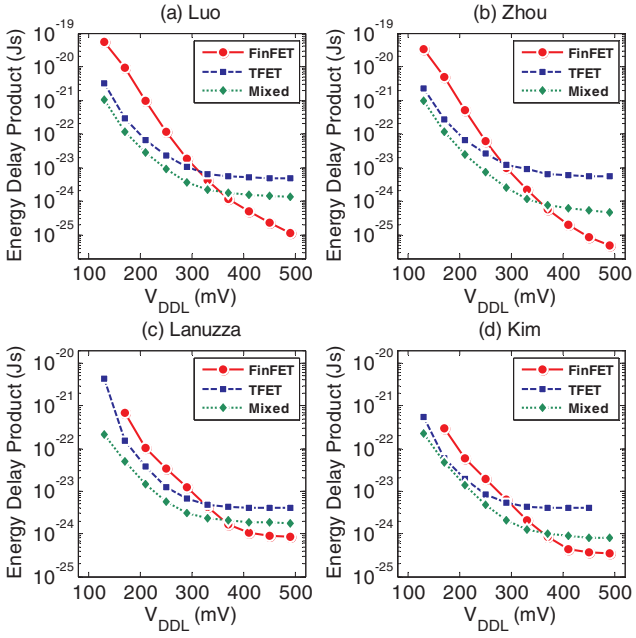

Fig. 18. Energy Delay Product comparison between pure FinFET/TFET design and hybrid solution as a function of V_{DDL}, considering the level shifter topologies depicted in Fig. 17. Plots a-b-c-d correspond to the topologies in [75–77] and [78] respectively.

The four LS topologies depicted in Fig. 17 (only hybrid FinFET/TFET designs), as proposed in [75–78], are analyzed in terms of energy delay product (EDP) considering different $V_{DDL} \rightarrow V_{DDH}$ signal up-conversions. In particular, the pure FinFET LS designs have been sized in order to achieve the minimum EDP for the target conversion 0.25 V → 0.75 V (note that 0.75 V is the nominal operating voltage of the considered FinFET technology), for 1 MHz input waveform. As regards the pure TFET and hybrid designs, similar leakage currents per circuit block are ensured by employing the same number of devices. The simulated EDP results as a function of V_{DDL}, for up-conversion to V_{DDH} = 0.75 V, are reported in Fig. 18 showing that for V_{DDL} below 0.4 V the hybrid FinFET/TFET approach outperforms both pure FinFET and TFET implementations, regardless of the considered circuit configuration. Thus, by employing TFETs as the transistors operating at V_{DDL} while keeping the FinFETs for the V_{DDH} operation, one can guarantee a sufficient pull-down network strength even at relatively low voltage input signals. This allows reduced current contention among pull-up (p-FinFETs) and pull-down (n-TFETs) devices in critical up-conversion operations (i.e. when V_{DDL} is extremely low) with a positive impact on the low-to-high delay, on the corresponding short circuit current and thus on the energy consumption. This twofold advantage in terms of delay and energy is well highlighted in Fig. 19, which shows the EDP ratio between FinFET and hybrid implementations for V_{DDL} ranging from 0.15 to 0.4 V and V_{DDH} in the range from 0.45 to 0.75 V. Similar trends are observed for all the hybrid designs, pointing out that the larger is the voltage up-conversion ratio the larger is the EDP improvement compared to the corresponding FinFET counterparts.

4. Analog/mixed-signal applications

This section focuses on benchmarking the same TFET and FinFET technology platforms described above, by moving to analog and mixed-signal domains. In fact, it is the most common situation in system-on-chips (SoCs) that the dominant digital part dictates the device specs and the analog circuit design simply adopts them and tries to use the existing devices at best. The circuit-level performances are dictated by the device-level figures-of-merit (FOM), such as the transconductance efficiency (g_m/I_D), output resistance (r_0), intrinsic gain (A_v) and cut-off frequency and maximum oscillation frequency (f_T and f_{MAX}). The comparison for *n*-type devices is reported in Fig. 20, the one for *p*-type devices in Fig. 21. TFETs exhibit significant advantages over FinFETs for low current level (below ~1 μA) in terms of g_m/I_D with a peak value around I_D = 1 nA for *n*-TFET and around 10 pA for *p*-TFET. The better saturation behavior of TFET devices (Fig. 3) results in a significantly higher r_0 compared to FinFETs in the current range 1n ~ 1 μA for *n*-TFET and 10p ~ 100 nA for *p*-TFET. The output resistance affects also the intrinsic gain, which is 100 times or 10 times larger for respectively the *n*-TFET or *p*-TFET compared to the corresponding FinFET at I_D of about 100 nA. TFETs outperform FinFETs also in terms of f_T with an improvement of approximately a factor 2 occurring around 1 nA for *n*-TFET and around 10 pA for *p*-TFET. On the other hand, for current levels larger than 80 nA (20 nA) for the n-type (p-type) devices, the FinFETs reach larger f_T peaks, e.g. 100 GHz in the 1μA range. One should however consider that these values have been computed for intrinsic devices, while the inclusion of layout parasitics would likely result in lower f_T peaks. In the same figure, the maximum oscillation frequency f_{MAX} is also reported, with similar trends as for the f_T (but different absolute values).

Overall, because of the asymmetric characteristics of TFETs, the *n*-type device exhibits larger improvements in terms of r_0 and A_v (about a factor 10) with respect to the *p*-type one when compared to FinFET counterpart, with the peak values of the g_m/I_D and f_T (and f_{MAX}) curves being shifted at lower current levels for *p*-type TFET. Based on these key FOMs, the potential of conventional topologies for TFET design is investigated and discussed in comparison to more complex CMOS low-voltage design topologies, considering some relevant analog/mixed signal building blocks such as *Current Mirrors* in Section 4.1, *Operational Amplifiers* in Section 4.2 and *Comparators* in Section 4.3.

A similar benchmarking study for the main analog FOMs of several building blocks (such as operational transconductance amplifier, track-and-hold, current mirror, differential pair, diode connected transistor) has been presented in two recent works [8,56]. In [8] two 14-nm node III–V TFETs (homo-junction InAs and hetero-junction GaSb-InAs) with a gate-length of 20 nm are compared with a Si MOSFET, while in [56] the 28-nm homo-junction strained-silicon (sSi) double-gate (DG) TFET is systematically benchmarked against the 28-nm low-power Fully Depleted Silicon on Insulator (FD-SOI) CMOS node. Significant advantages have been shown for low-to-moderate current densities both at device and circuit levels, highlighting the potential of conventional topology for TFET design compared to CMOS design which instead requires more complex topologies to achieve similar performance in low-voltage design.

4.1. Current mirrors

In the context of analog design, current mirrors are required to generate a replica of a given current reference, that corresponds to the implementation of a current controlled current source. Their most important figure-of-merit is the output resistance, which is required to be sufficiently high to deliver an almost constant output current over a wide range of output voltages. Several topologies of current mirrors have been proposed and the selection of the most appropriate topology depends on the adopted technology [79]. An experimental comparison of TFET and FinFET current mirrors is reported in [35] in which the ability of the simple topology in mirroring the reference current is analyzed, showing a reduced sensitivity of TFET design to channel length variation compared to FinFET implementation. In the following, we have analysed the simple, the cascode and the high-compliance mirror topologies sketched in Fig. 22, by considering a reference current (I_{REF}) of 100 nA where the TFET r_0 is close to highest compared to the FinFET one. Fig. 23 reports the ratio between the output current (I_{OUT}) and I_{REF} as a function of the output voltage (V_{OUT}). As for the FinFET designs, it can be seen that: (i) the simple circuit has a strong

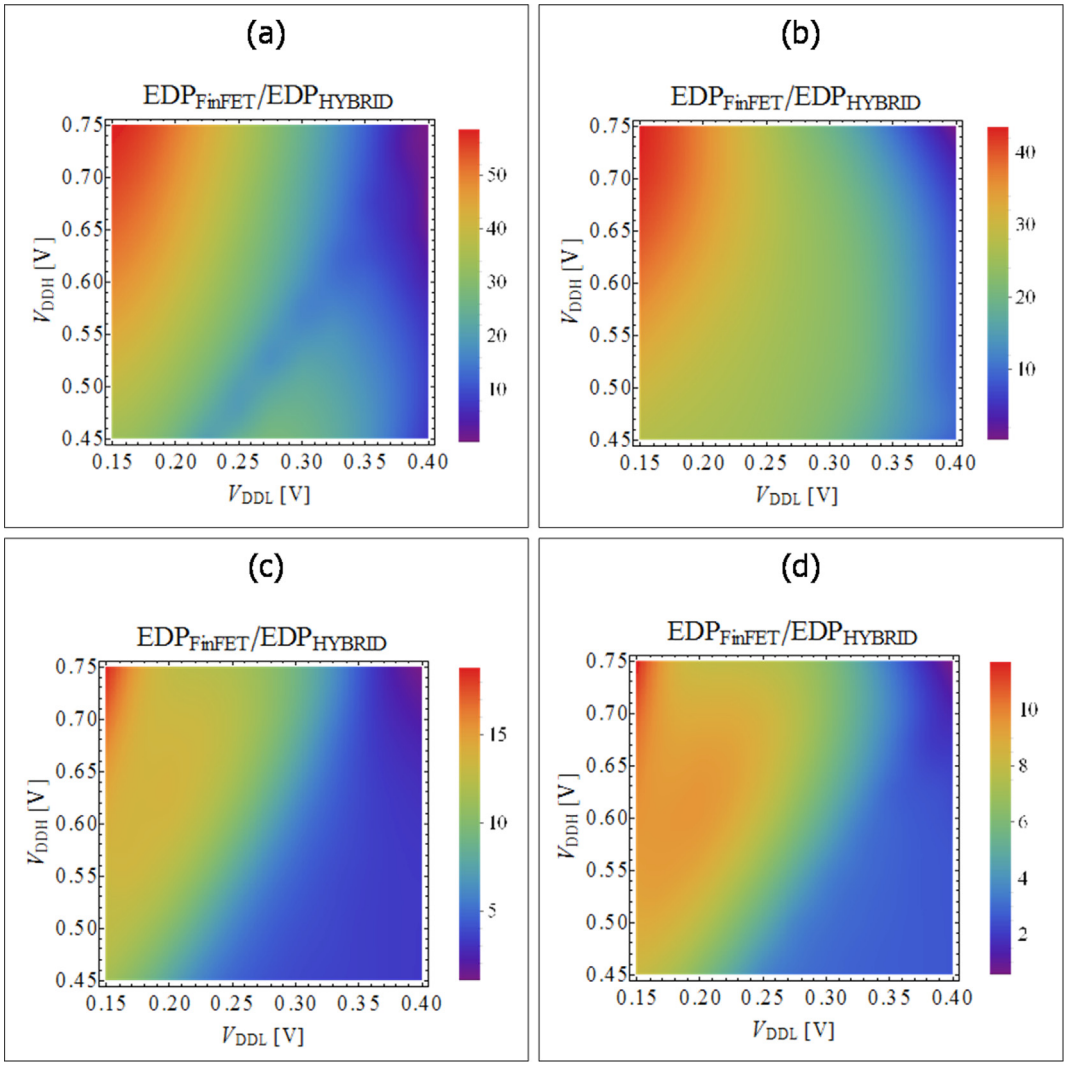

Fig. 19. EDP ratio between pure FinFET design and hybrid solution as a function of V_{DDH} and V_{DDL}, considering the level shifter topologies reported in Fig. 17. Plots a-b-c-d correspond to the topologies in [75–77] and [78] respectively.

sensitivity to V_{OUT}, which practically impedes the proper operation of the mirror; (ii) the cascode solution shows the drawback of a high minimum output voltage (V_{OUTmin}); the FinFET high-compliance topology allows to achieve a good performance in terms of low sensitivity to V_{OUT} and low V_{OUTmin}, but it requires additional biasing circuitry, resulting in a significant area penalty. As for the TFET designs, the significantly higher output resistance makes the simple current mirror have similar mirroring performance compared to the FinFET high-compliance architecture. The TFET cascode implementation allows for a slight improvement in keeping the I_{OUT}/I_{REF} ratio close to one, but at the expenses of higher V_{OUTmin} because of the delayed onset of the saturation region in TFETs compared to FinFETs. The important conclusion is thus that the TFET-based design has the potential to significantly reduce the circuit complexity of a low-voltage current mirror, without significantly affecting the performance.

4.2. Operational amplifiers

The design of operational amplifiers with sub-1 V operation poses several challenges, mainly due to the speed-limiting factor associated to the reduced current level in sub-threshold operation [80,81]. The circuit performance can be predicted by applying the g_m/I_D design methodology [82] which has been extensively reviewed in [83] for TFET designs. The results obtained from current mirrors hint to the potential of TFET implementation for low voltage operational amplifiers. The simple, the telescopic cascode and the folded cascode operational amplifier topologies (see Fig. 24), implemented with TFETs and FinFETs, are compared in terms of DC gain and of the figure-of-merit FOM_{GBW} (defined as $\frac{GBW \times C_{load}}{I_{BIAS}}$) [80], which provides a fair comparative evaluation of the bandwidth-power consumption trade-off. The circuits are designed for the target unity gain frequency of 50 MHz at V_{DD} = 0.5 V and under the same load condition, C_{load} = 1 fF. Table 2 reports the DC gain as well as the FOM_{GBW} values, which are basically a measure of the power consumption because the circuits are compared for the same GBW and C_{load}. As a consequence of the combined effect of higher output resistance of the active load and higher g_m/I_d at lower current level, for the simplest topology the TFETs implementation allows to achieve significantly higher performance compared to its FinFET counterpart in terms of DC gain and at a lower power consumption. The cascode solutions (folded or telescopic cascode) are required for FinFET design in order to compete with the gain of the TFET simple circuit, but at the expense of reduced output swing, higher power consumption and increased silicon area. For the same circuit topology, TFETs show improvements over FinFETs in the order of a factor of 2 in terms of both performance and power.

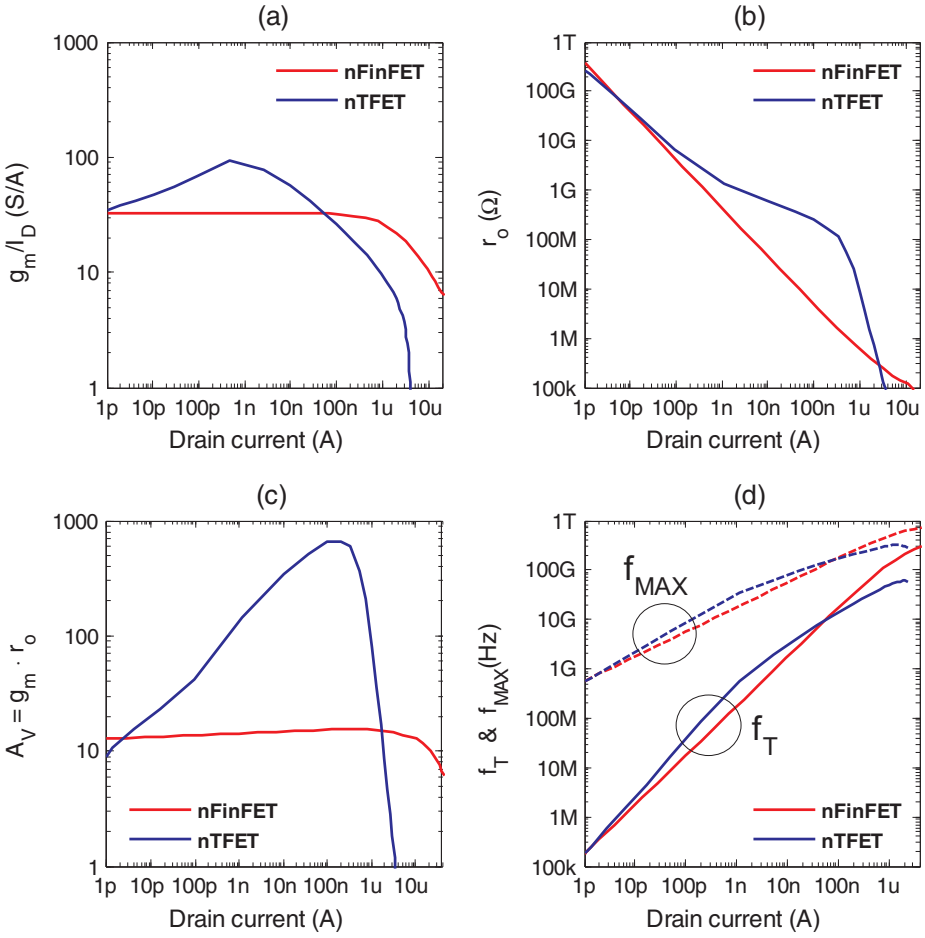

Fig. 20. *n*-type devices: (a) transconductance efficiency (g_m/I_D), (b) output resistance (r_o), (c) intrinsic gain ($A_{vi} = g_m r_o$) and (d) cut-off frequency and max oscillation frequency (f_T and f_{MAX}) as a function of I_D at $|V_{DS}| = 0.3$ V. In order to estimate f_{MAX} for the TFETs, we have considered the same source/drain series resistance as in the FinFET models (i.e. 1.28 kΩ).

4.3. Comparators

In the context of analog-to-digital conversion, dynamic regenerative comparators are required for fast and energy efficient operation. Thanks to the higher transconductance efficiency at lower current level, TFET designs could enable significant power saving compared to FinFET ones. The conventional and double tail [84] architectures sketched in Fig. 25 are compared in terms of energy and delay. The FinFET designs have been sized according to a progressive sizing methodology for stacked transistors, while TFET designs have been sized in order to keep approximately the same static current consumption as their FinFET counterparts. The simulation setup consists of 5 mV differential input (V_d) with an input common mode (V_{CM}) of 70% V_{DD} and a load capacitance (C_L) of 1 fF, which corresponds approximately to the effective input capacitance of 10 parallel minimum-size FinFET inverters. The FinFET-based double tail topology enables a significant boost of the speed in comparison to the conventional design at the expense of higher energy per operation (obtained considering the minimum clock period at each V_{DD}), as depicted in Fig. 26. As for the TFET designs, the conventional architecture has comparable performance to the double tail in terms of speed while keeping lower energy per operation (E_{op}), because of the asymmetric characteristic of *p*- and *n*-type TFETs. Thus, the TFET-based conventional structure appears to be the best option compared to both the FinFET-based designs, also due to the reduced number of devices compared to the more complex double tail structure. Furthermore, considering a TFET-based design, a reduced V_{CM} value allows for an extended range of V_{DD} where TFET-based comparators outperform their FinFET counterparts as reported in Fig. 27, in which the EDP is plotted as a function of V_{DD} for different values of V_{CM} ranging from 50% to 90% of V_{DD}.

5. Conclusions

This work has provided an overview of TFET circuit applications, along with a detailed benchmark against aggressively scaled FinFETs, carried out by touching a large variety of circuit domains including digital, analog and mixed-signal building blocks. The virtual TFET technology platform consists of III-V heterojunction NWs, designed through advanced full-quantum simulators in [59], while the predictive technology model (PTM) platform of 10 nm node FinFETs was used as representative of the CMOS counterpart [60]. For a fair comparison, TFET and FinFET blocks have been operated at approximately the same static power density consumption that is at fixed area occupation and off-current. Unlike FinFETs, the considered TFETs feature asymmetric *p*- versus *n*-type transistors drain current characteristics, as actually the case in several experimental reports.

Highlights related to the **digital domain**:

- **Basic blocks (inverters, FO4 and ring-oscillators)**. Symmetric VTC can be achieved with TFETs at the cost of using ~4 p-type parallel devices for each n-type, to implement the pull-up and pull-down network, respectively. This is not the case for FinFET inverters, whose VTC is almost symmetric even considering a 1/1 p/n ratio. The large capacitance and area occupation compared to FinFETs due to the number of pull-up TFET devices, leads to larger energy consumption without providing a real performance

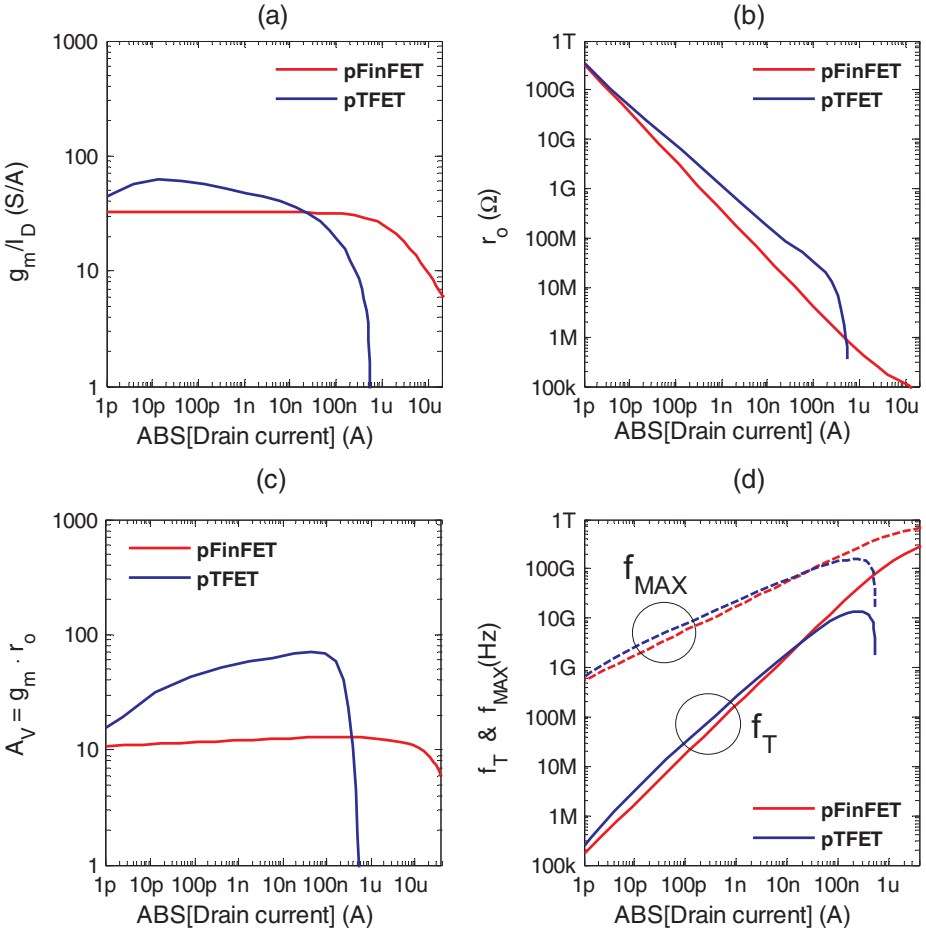

Fig. 21. *p*-type devices: (a) transconductance efficiency (g_m/I_D), (b) output resistance (r_o), (c) intrinsic gain ($A_{vi} = g_m r_o$) and (d) cut-off frequency and max oscillation frequency (f_T and f_{MAX}) as a function of I_D at $|V_{DS}| = 0.3$ V. In order to estimate f_{MAX} for the TFETs, we have considered the same source/drain series resistance as in the FinFET models (i.e. 1.28 kΩ).

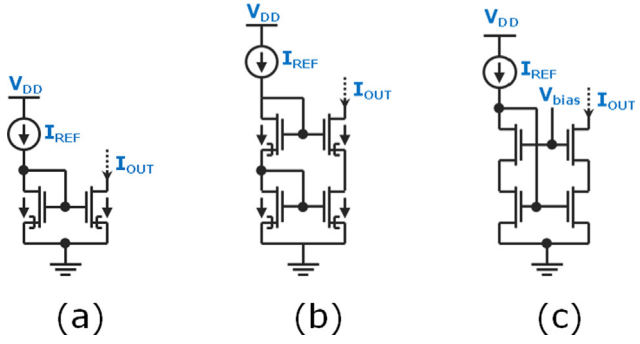

Fig. 22. Schematic of the current mirrors considered in this work: (a) simple, (b) cascode and (c) high-compliance.

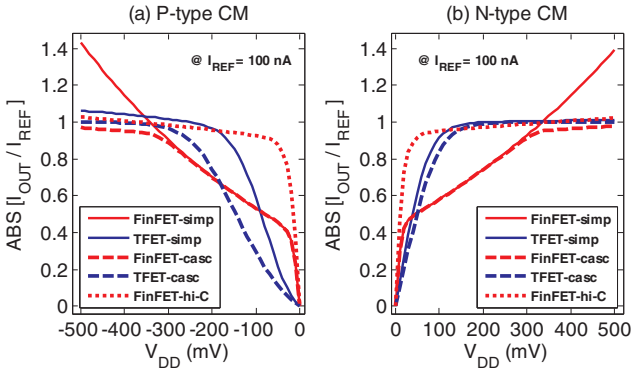

Fig. 23. I_{OUT}/I_{REF} ratio for (a) *p*-type and (b) *n*-type version of current mirrors reported in Fig. 22. The circuits are compared for the same reference current of 100 nA.

advantage. Thus, by considering minimum size inverters, 5-stages ring-oscillator benchmark-vehicle demonstrated a better energy efficiency of TFETs only in applications with time constants below ~1 ns, e.g.: if FinFETs are replaced by TFETs, the energy per cycle is approximately halved for a T_{osc} of ~10 ns.

- **Arithmetic circuits (full-adders).** The standard 28 transistors implementation of 1-bit full-adder has been used as a benchmark for the logic/arithmetic domain. The carry-in to carry-out propagation delay has been selected as the main performance figure-of-merit: TFET full-adder turned out to be faster than the corresponding FinFET implementation for V_{DD} below ~400 mV. When considering multi-bit adders such as the 32-bit ripple carry adder implemented with a chain of 32 1-bit full-adder blocks, similar energy consumption is found when TFET and FinFET solutions are operated at the same V_{DD}, if a 100% switching activity is assumed. However, when moving toward applications featuring a limited switching activity (e.g. < 10%), the TFET circuits allow energy saving at low V_{DD} (i.e. below 400 mV), which corresponds to the regime where the static energy becomes relevant, and moreover they can be operated at a lower minimum energy point. In fact, irrespective of similar active power, in that regime the same operation can be performed in a reduced time if TFETs are employed.
- **Memory cells (SRAM).** We have considered a standard 6T Static-RAM memory block as a test vehicle for memory cells based on TFETs. Due to unidirectional conduction, the TFET access-transistors have been oriented in the outward configuration by connecting the source to the BLs. The sizing of the cell transistors has been optimized for each V_{DD} in order to enable functional hold, read and

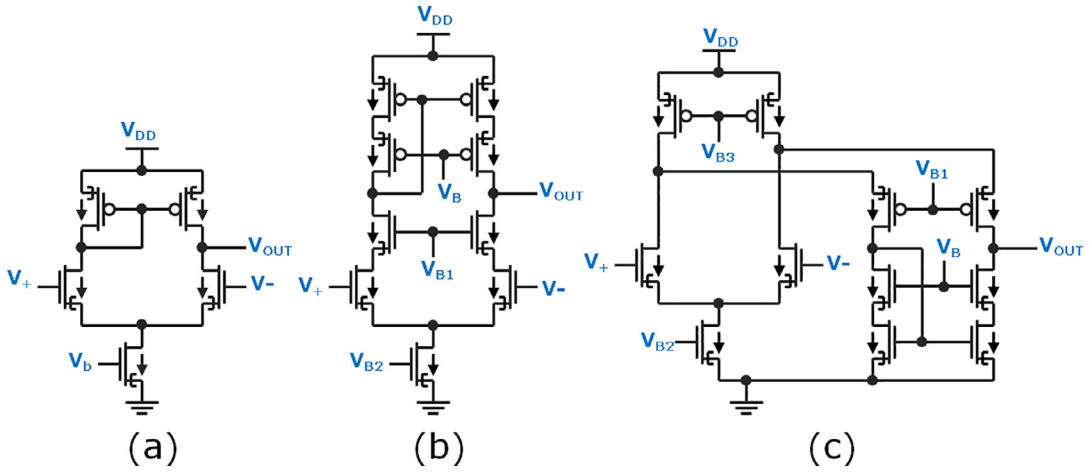

Fig. 24. Schematic of the operational amplifiers considered in this work: (a) simple, (b) telescopic cascode and (c) folded cascode.

Table 2
Performance comparison of the operational amplifiers reported in Fig. 24 considering a minimum size design.

	TFET design			FinFET design		
	Simple	Telescopic cascode	Folded cascode	Simple	Telescopic cascode	Folded cascode
DC gain [dB]	33	50	58	16	36	34
FOM_{GBW}* [MHz·p-F/μA]	6.3	6.3	2.6	2.2	2.3	1.2
I_{DD} [nA]	7.9	7.9	19.2	22.7	21.7	41.7

* V_{DD} = 500 mV, GBW = 50 MHz, C_L = 1fF.

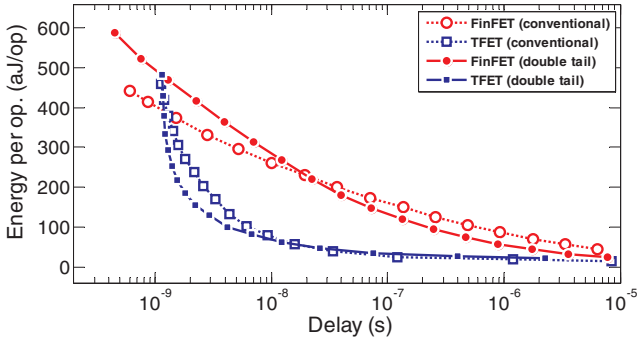

Fig. 26. Energy per operation as a function of the delay for the comparators reported in Fig. 25. The different points correspond to different V_{DD} values ranging from 100 mV to 600 mV (step 10 mV).

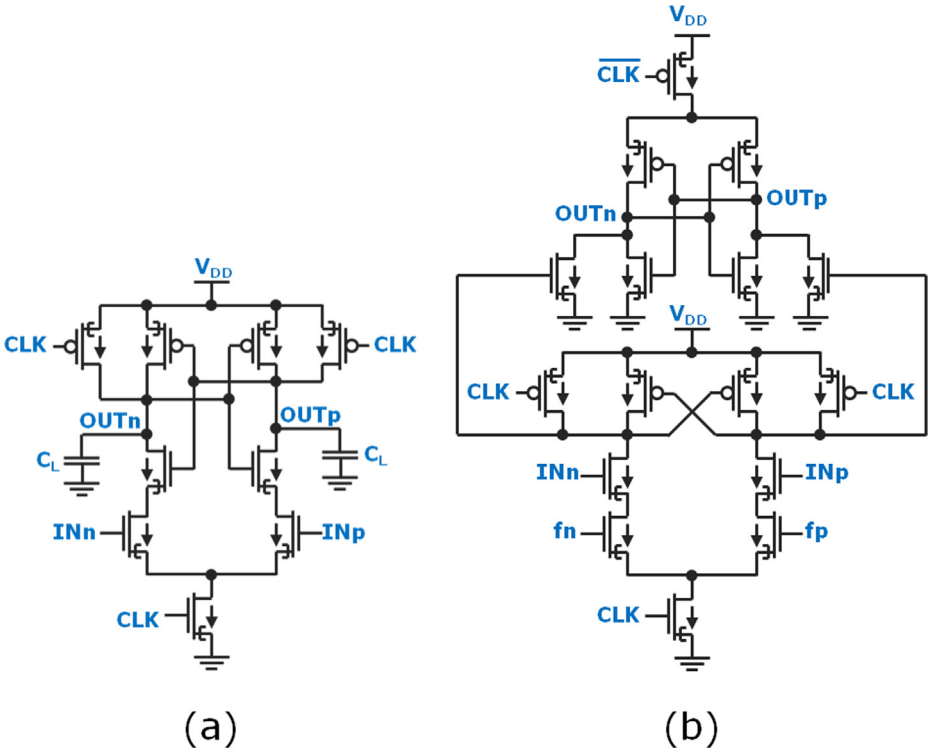

Fig. 25. Schematic of (a) conventional and (b) double tail comparators.

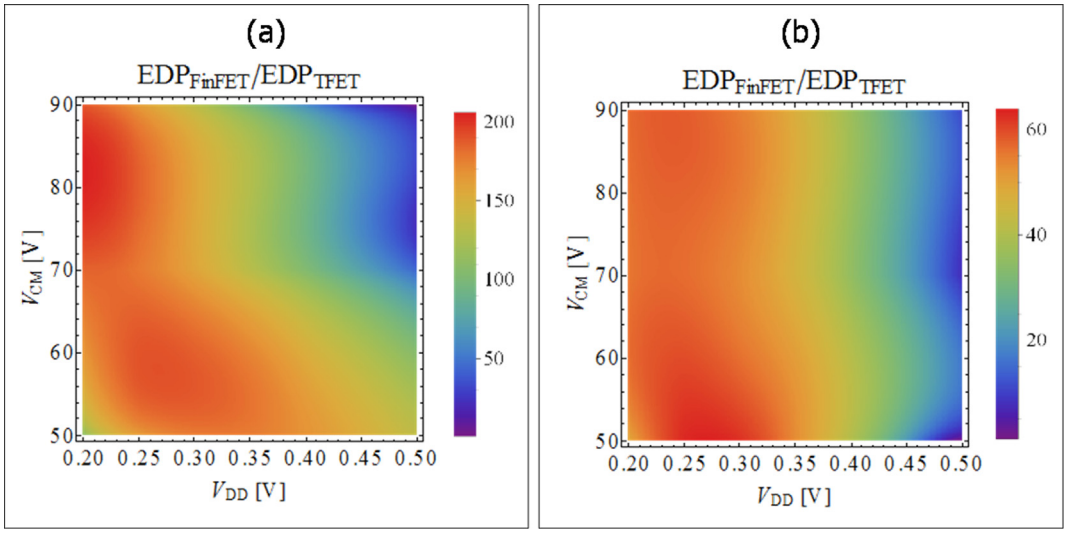

Fig. 27. EDP ratio between FinFET and TFET design as a function of V_{DD} and V_{CM} for the comparators in Fig. 25.

write operation for both TFET and FinFET SRAMs. Irrespective of the unidirectional limit, the outward-faced access-transistors TFET SRAM leads to competitive read and write delays at scaled supply voltage (< 400 mV), when it is operated with a BL pre-charge at $V_{DD}/2$ during the read phase.

- **Voltage up-converters (level-shifter)**. The potentialities of TFET devices have been exploited in the implementation of hybrid TFET/FinFET level-shifters, where TFET devices are introduced in the low supply circuit sections for efficient voltage up-conversion from the ultralow-voltage regime. The mixed solution exhibits superior dynamic performance at the same static power consumption than both pure MOSFET and pure TFET solutions. The same behaviour has been found on four different topologies, thus confirming that the mixed TFET–MOSFET approach is intrinsically suitable for such application.

Highlights related to the **analog/mixed-signal domain**:

- **Basic analog device level figures-of-merit**. TFETs exhibit significantly higher maximum values for the *trans*-conductance efficiency g_m/I_D and intrinsic voltage gain $A_{Vi} = g_m \cdot r_o$ (up to almost two decades for n-type and one decade for p-type) than FinFETs, mainly due to their higher output resistance at low current levels. The f_T of TFETs is slightly higher than that of FinFETs at low current levels (a larger advantage is observed for the n-type device), while it is significantly lower at high current levels, mainly due to the corresponding transconductance behaviour. As regards the TFET output resistance, r_o is larger than the one of FinFETs for currents in the μA range, while they tend to be similar for very low current levels.
- **Current mirrors**. The large output resistance of TFETs can be conveniently exploited in the design of current mirrors, considering that they require a high output resistance to deliver an almost constant output current against output voltage variations. When compared to a FinFET implementation, TFET-based design has the potential to significantly reduce the circuit complexity of a low-voltage current mirror, without any significant performance loss.
- **Operation Amplifier**. The capability of simple TFET design to perform with comparable performance of more complex FinFET implementations has been demonstrated also for the operational amplifiers, where the simple TFET operation amplifier shows both DC and AC figures-of-merit comparable with the folded and telescopic cascode FinFET operation amplifiers, while featuring a reduced power consumption.
- **Comparators**. TFET-based comparators (both conventional and double tail architectures) allow for better energy-delay-product in the ultra-low voltage regime for a large swing of the common-mode input voltage and V_{DD}, up to an EDP better than 200 and 60 times for the conventional and double tail implementations, respectively. Furthermore, the TFET-based conventional topology offers similar EDP performance compared to the more complex double tail topology, basically because of the lower sensitivity to the asymmetric characteristic of *p*/*n*-type TFETs, enabling potential area saving.

From a general perspective, the key messages of this study are:

- the pros (i.e. low subthreshold swing and high output resistance) and cons (i.e. ambipolarity, unidirectionality, p- versus n-type asymmetry, large gate-to-drain intrinsic capacitance, higher sensitivity to variability sources) of TFETs with respect to MOSFETs can be balanced at best by adopting new circuit topologies with respect to standard CMOS solutions;
- while research on TFETs focuses mostly on switches for digital circuits, TFETs exhibit potential interesting advantages also for analog and mixed-signal applications; these advantages might be emphasized in niche applications, by exploiting the low-temperature dependence of TFET operation;
- the introduction of TFET in mainstream CMOS technologies will likely be limited to electronic systems operating at extremely reduced voltage (lower than 400 mV) and by preferentially adopting an hybrid TFET/MOSFET implementation, which takes advantage of both transistor options. At such small voltages, (time dependent) variability may end up being the most stringent requirement dictating the application window of such technology.

Acknowledgment

The research leading to these results has received funding from the European Community's Seventh Framework Programme under grant agreement No. 619509 (project E2SWITCH).

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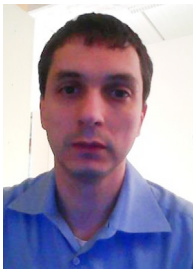

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