Ferroelectric field-effect transistors based on solution-processed electrochemically exfoliated graphene

Jonas Heidler, Sheng Yang, Xinliang Feng, Klaus Müllen, Kamal Asadi

PII: S0038-1101(17)30707-4
DOI: https://doi.org/10.1016/j.sse.2018.03.008
Reference: SSE 7413

To appear in: *Solid-State Electronics*

Received Date: 19 September 2017
Revised Date: 14 March 2018
Accepted Date: 28 March 2018

Please cite this article as: Heidler, J., Yang, S., Feng, X., Müllen, K., Asadi, K., Ferroelectric field-effect transistors based on solution-processed electrochemically exfoliated graphene, *Solid-State Electronics* (2018), doi: https://doi.org/10.1016/j.sse.2018.03.008

Ferroelectric field-effect transistors based on solution-processed electrochemically exfoliated graphene

Jonas Heidler[1, a], Sheng Yang[1], Xinliang Feng[2], Klaus Müllen[1,3] Kamal Asadi[1,*]

[1] Max-Planck Institute for Polymer Research, Ackermannweg 10, 55128 Mainz, Germany.

[2] Molecular Functional Materials, Department of Chemistry and Food Chemistry, Technische Universität Dresden, 01062 Dresden, Germany.

[3] University of Mainz, Institute of Physical Chemistry, Duesbergweg 10, 55128, Mainz, Germany.

[a] Present address: Paul Scherrer Institute, OFLC/102, 5232 Villigen, Switzerland

* E-mail Address: asadi@mpip-mainz.mpg.de

Abstract

Memories based on graphene that could be mass produced using low-cost methods have not yet received much attention. Here we demonstrate graphene ferroelectric (dual-gate) field effect transistors. The graphene has been obtained using electrochemical exfoliation of graphite. Field-effect transistors are realized using a monolayer of graphene flakes deposited by the Langmuir-Blodgett protocol. Ferroelectric field effect transistor memories are realized using a random ferroelectric copolymer poly(vinylidenefluoride-co-trifluoroethylene) in a top gated geometry. The memory transistors reveal ambipolar behaviour with both electron and hole accumulation channels. We show that the non-ferroelectric bottom gate can be advantageously used to tune the on/off ratio.

Keywords: Electrochemically exfoliated graphene, ferroelectric, field-effect transistor, memory, graphene

1. Introduction

Graphene holds great promise for microelectronic applications.[1–5] Digital memories based on graphene have been proposed and different graphene memory concepts based on charge trapping[6–9] and ferroelectric gating[10–16] have been demonstrated. There have been many efforts to integrate ferroelectrics (both organic and inorganic) with graphene for non-volatile memory applications.[17] In all cases a transistor is used with a planar structure. The ferroelectric memories have been realized using graphene obtained from either mechanical exfoliation or chemical vapour deposition (CVD).

Due to good mechanical properties and flexibility, graphene has been suggested for low-cost, flexible electronics. Mechanically exfoliated graphene, however, does not meet the up-scaling and industrial production demand. CVD growth wherein an organic precursor is decomposed at elevated temperatures on a Cu or Ni foil,[18] requires post-growth transfer of graphene to a target substrate using a sacrificial transfer layer and wet etching of the metal foil.[19–21] The etching process is typically done in an aqueous acidic environment. As a result, transferred CVD graphene is usually highly doped and exhibit a large uncontrolled shift in the Dirac voltage. The lack of control over the Dirac voltage results in typically absence of electron channel in the transistor, as well as the reliability and irreproducibility issues in the performance of discrete graphene memories. Moreover, the thermal budget (process temperature and time) for CVD-grown graphene is incompatible with low-cost and low-temperature technologies.[22–25] For low-cost, flexible electronic applications, a low-temperature solution-based graphene production technology is still needed, which eventually enables solution-processed graphene ferroelectric transistors. Viable solution processed memories based on low-cost graphene have not been demonstrated yet.

Recently, low-cost graphene mass production methods have been proposed that yield high-quality graphene sheets at low temperatures particularly suitable for applications in disposable and printed electronics. Electrochemical (EC) exfoliation of graphite sheets in aqueous solutions has been demonstrated as an effective and high yielding route toward up-scaled graphene fabrication.[26–29] It has been shown that EC-exfoliation in electrolytes leads to flakes with large lateral size of up to 44 μm and typically less than 3 layers. EC-exfoliated graphene flakes have a low oxidation degree (a carbon/oxygen ratio of 17.2). The reported hole mobility in EC-exfoliated graphene is about 300 cm^2/Vs, much lower than that of CVD graphene however suitable for low-cost printed electronic applications.[30] Despite the potential of EC-exfoliated graphene for micro-electronic applications, functional devices such as memories have not been reported so far.

Here, we describe the fabrication of ferroelectric memories based on electrochemically exfoliated graphene. By adjusting the processing parameters, a layer of connected graphene flakes that bridges the gap between the source and drain electrodes can be obtained using Langmuir-Blodgett thin-film deposition. Graphene transistors are realized by deposition of the flakes on a substrate with pre-patterned source and drain electrodes. The fabrication process yields reproducible metal/graphene contacts that are on par with previously reported metal/graphene contacts using the conventional methods, *e.g.* photolithography, contact deposition, followed by etching or lift-off.[31–35] The ferroelectric field-effect transistors display ambipolar behaviour, *i.e.* both electron and hole accumulation channels can be realized. We demonstrate the basic hysteretic transfer characteristics of a ferroelectric transistor. The remanent ferroelectric polarization modulates conductance of the graphene layer. Bistable conductance at zero gate bias can be achieved using the two different polarization states of the ferroelectric layer. We further show that memory on/off ratio can be tuned by introducing a second control gate electrode. The performance of the ferroelectric transistors presented in our work is comparable with those realized with mechanically exfoliated or CVD grown graphene.[36] Therefore, electrochemically exfoliated graphene can be suggested as a low-cost solution-processed alternative for application of graphene in digital memories.

2. Experimental

The exfoliation of graphene from graphite was carried out in a dual-electrode system, thereby employing graphite foil as an anode and platinum foil as cathode. To prepare the electrolyte solution, ammonium sulphate was dissolved in deionized water (0.1 mol/L). The exfoliation was initiated by applying a positive voltage (+10 V) to the graphite anode. Exfoliated graphene flakes finally floated on the surface of the electrolyte and the exfoliation process lasted for 15 minutes. The resultant exfoliated graphene flakes were then collected by vacuum filtration with a polytetrafluoroethylene (PTFE) membrane filter and washed three times with water to remove any salt traces. The graphene dispersion was obtained by treating the flakes in dimethylformamide (DMF) via mild sonication in an ice bath. The dispersion was then kept for 12 hours to eliminate un-exfoliated flakes or aggregates. Details of the exfoliation process have been reported previously.[30] The supernatant graphene dispersion (ca. 0.2 mg/mL) was subsequently mixed with chloroform (1:3 v/v). 100 μL of the mixture were carefully dropped onto the water surface in the Langmuir-Blodgett (LB) trough. The thin graphene film was compressed by the LB barrier. The surface tension was monitored using a tensiometer. The EC-exfoliated graphene layer was finally transferred onto the substrate through vertical dip-coating. Transistor structures were fabricated on 150 mm highly doped p-type Si wafers with 250 nm of thermally grown SiO_2. Au/Ti (150 nm/2 nm) source and drain electrodes were obtained by conventional photolithography. Ti was used as an adhesion layer. The electrode spacing was varied from 5 μm to 40 μm. The ferroelectric random copolymers of poly(vinylidenefluoride) with trifluoroethylene (P(VDF-TrFE)) (65/35 mol %) were spin-coated from butanone on top of the graphene layer and acted as the ferroelectric gate dielectric.[37–39] The P(VDF-TrFE) layer thickness amounted to 1 μm. No change in the optical images were observed upon spin-coating of the P(VDF-TrFE) layer. Detailed SEM imaging could not be performed after P(VDF-TrFE) deposition due to charging issues. The top gate Au electrode was evaporated through a shadow mask following a vacuum annealing step at 140 °C to enhance the crystallinity of the P(VDF-TrFE) layer.[40] It is well-established that the annealing step is crucial to enhance the ferroelectric response of the P(VDF-TFE) layer.[41,42] Presence of graphene does not influence crystallization of the P(VDF-TrFE) over layer.[43] Furthermore we probed P(VDF-TrFE) morphology after annealing using AFM. Typical needle/star-shaped crystallites were observed. Devices were measured in ambient condition and in vacuum (10^{-6} mbar), but no significant differences were observed. We note that all measurements were performed under dark condition at a constant temperature (T= 293 K) to minimize sporadic effect of ambient light absorption and temperature variations. The device layout and the chemical structure of the compounds are given in figure 1.

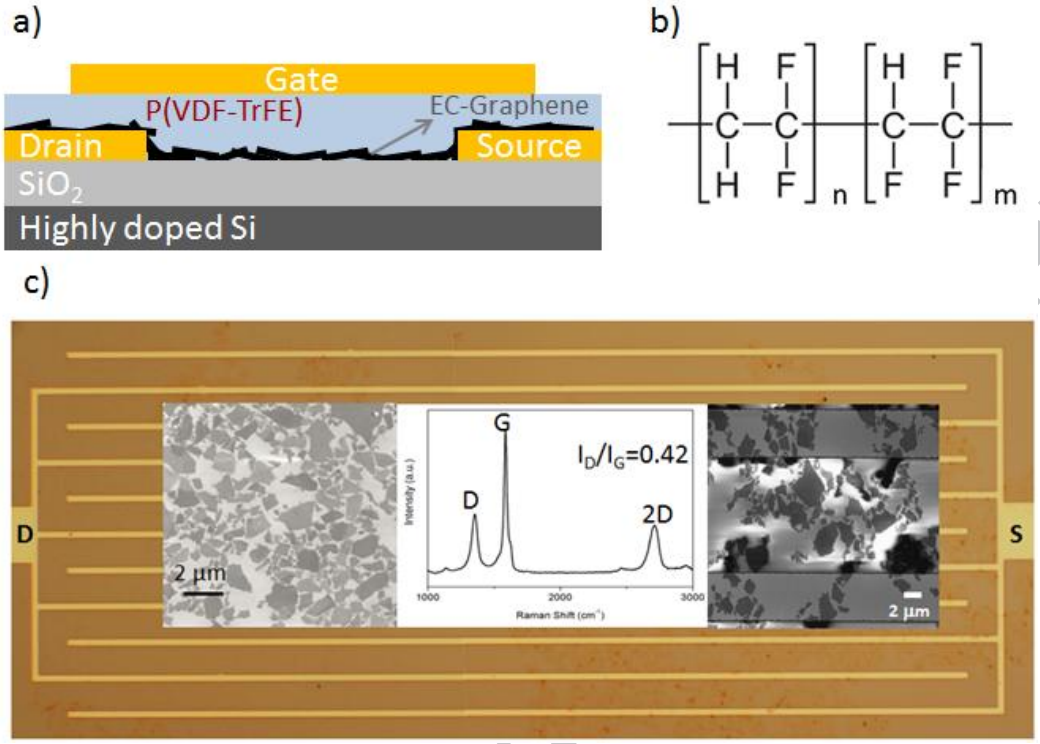


Figure 1. a) Schematic description of the dual-gate ferroelectric transistor with electrochemically exfoliated graphene flakes in the channel. b) Schematic representation of the chemical structure of P(VDF-TrFE). c) Optical image of a transistor with interdigitated finger electrode geometry. The FET surface covered with EC-exfoliated graphene flakes appeared as orange spots on the surface. The insets show an SEM image of dark grey graphene flakes on the light grey SiO_2 surface (left), the corresponding Raman spectra (middle) and on the right a typical SEM image of the EC-graphene flakes between two gold

3. Results and discussion

The morphology and quality of the EC-exfoliated graphene were evaluated using scanning electron microscopy and Raman spectroscopy. Figure 1c shows a typical SEM image of the EC-exfoliated flakes. It is known that for 80% of the flakes the lateral size is larger than 5.0 μm (figure 1c), and 85% of EC-graphene flakes comprise thin graphene (≤3 layers), where single and bilayer graphene are the dominant products (together ~72%). A typical Raman spectrum (also given in figure 1c) was recorded near the center of a graphene flake using a 532 nm excitation laser incident on the flake deposited SiO_2 surface. The spectrum gave an I_D/I_G ratio of 0.42, which is much smaller than for chemically or thermally reduced graphene oxide (~1.1−1.5) and suggests the formation of graphene flakes with relatively low degree of defects.[44] We have previously published an extensive analysis of the exfoliated flakes using Raman spectroscopy.[30] The flakes were subsequently transferred onto a pre-patterned transistor structure using LB thin-film deposition. An optical image of the device is given in figure 1c. It is evident that the flakes did not fully cover the device area. To arrive at a reliable statistics for graphene flake coverage on the substrates, we analysed numerous SEM images taken from different parts of the substrate. The inspected area was always larger than 100 μm2. In figure 1c, a typical 10μm x 10μm is shown. The graphene coverage on SiO2 surface calculated from the SEM images amount to 50%. The variation in coverage is within 5-10% depending on the grayscale threshold used for the image processing. Due to the presence of OH bonds, the SiO_2 surface is likely to trap accumulated electrons and cause an undesirable hysteresis in the transfer characteristics. The surface of the SiO_2 layer was therefore passivated with hexamethyldisilazane (HMDS) prior to EC-exfoliated graphene deposition on FET substrates. As a result of HMDS treatment hysteresis due to charge trapping disappears from the transfer characteristics thereby enabling correct evaluation of the hysteresis caused by the ferroelectric polarization.[45]

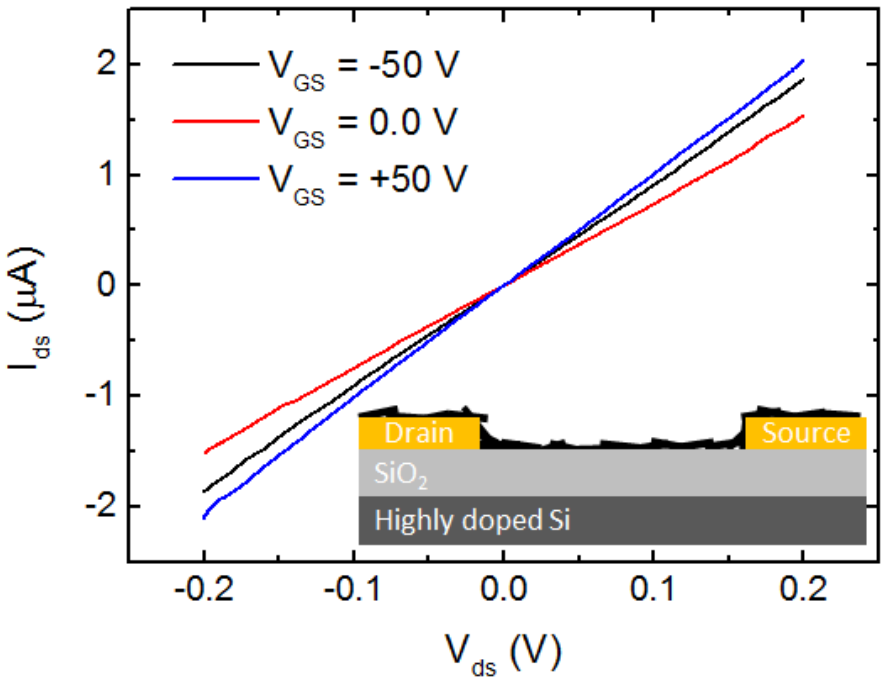


Figure 2. Output characteristics of a bottom-gate EC-exfoliated graphene transistor. The inset shows the FET layout. The channel length and width are 5 μm and 10000 μm, respectively.

The output characteristic of a typical transistor is presented in figure 2. The current reveals a linear dependence upon the source drain bias and can be modulated with the applied bottom gate bias. The coverage of the substrate by the flakes as shown in the right inset of figure 1c, is incomplete. Hence calculating the mobility by taking only the geometrical device dimensions, as defined by the photolithography process, leads to a severe underestimation of the mobility (a value of nearly 10^{-3} cm^2/Vs was calculated). To correctly evaluate the mobility, the channel width of the graphene transistor must be determined. The flakes are randomly oriented and do not fully cover the substrates. A careful inspection of the transistor substrate was performed using SEM to identify the positions where the graphene flakes make a bridge between the two Au electrodes. A typical SEM image of the channel is shown in figure 1c. The channel width of the transistors was estimated using the following protocol: First the bridging positions were identified. Subsequently, the width of the contact between the flake and the drain electrode was taken as the channel width at the respective position. The total channel width was obtained by summation of the channel width of all connecting bridges. Upon channel width correction, a mobility of 100 cm^2/Vs was obtained, which is very close to previously reported values.[30,46] It has been recently shown that graphene deposition onto pre-patterned substrates has minimal adverse effects on the quality of the graphene layer and yields high quality reproducible metal/graphene contacts.[35] Furthermore, upscaling of the device fabrication process has been demonstrated.

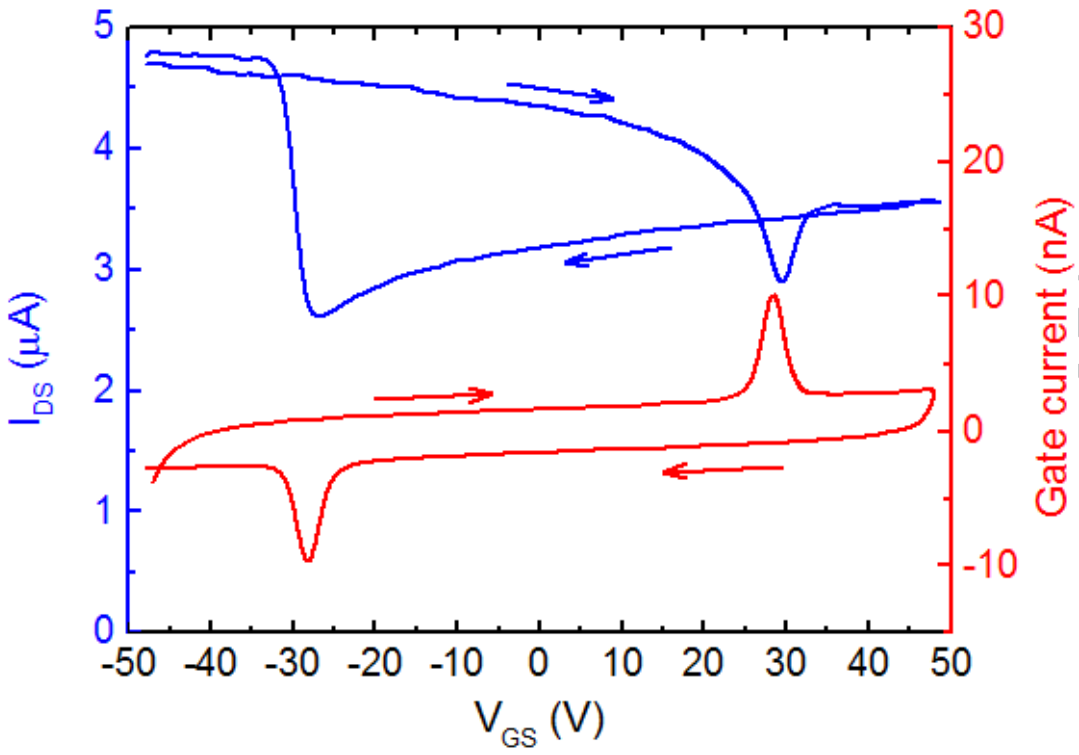


Figure 3. Output characteristics (blue) and the displacement gate leakage current (red) of a top-gate ferroelectric field-effect transistor based on EC-exfoliated graphene flakes. The device layout is shown in figure 1a. The channel length and width are 5 μm and 10000 μm, respectively.

Next, a layer of the ferroelectric polymer P(VDF-TrFE) was spin coated onto the graphene film. The FeFETs were completed by deposition of a gold top gate electrode. A low bias of 100 mV was applied to the drain electrode. The source was grounded, and the gate bias was swept from -50 V to 50 V and back. A typical transfer curve of the FeFET is given in figure 3. At -50 V gate bias, P(VDF-TrFE) is fully negatively polarized. The negative polarization is stabilized by accumulated holes in the EC-graphene layer, which leads to formation of a hole channel in the graphene layer. As the gate voltage increases towards positive values, at about +30 V, the coercive field is reached and the polarization of the ferroelectric switches its direction. The hole current suddenly drops, and the gate leakage, displacement current shows a switching peak. Due to polarization reversal, the channel is depleted from holes. Electrons are then accumulated to stabilize and compensate for the positive ferroelectric polarization. As a result, an electron channel is formed; the current shows a sudden rise, and the transistor is back to the on-state albeit in the electron accumulation regime. Upon a reverse sweep, when the gate bias reaches the coercive field at -30 V, the ferroelectric polarization is reversed. The displacement current exhibits a peak, and the polarization is again negative and stabilized with accumulated holes. The EC-exfoliated FeFETs reveals typical ambipolar behaviour. It should be noted that SiO_2 substrate usually p-dopes the graphene layer.[9] Hence the hole current is slightly higher than the electron current. It should be noted that since graphene is a zero band gap semiconductor, it can never be depleted; hence there is no threshold voltage for graphene FeFETs. Instead, the position of the Dirac point is sensitive to the gate bias.[10,13] In EC-graphene FeFETs, the Dirac point is doubled due to the polarization switching of the gate dielectric and coincides with the coercive voltage of the ferroelectric gate. It is well-known that surface treatment of SiO_2 with self-assembled monolayers such as HMDS promotes electron conduction in the semiconductor atop layer due to effective hindrance of electron trapping by the SiO_2 layer.[45] Observation of the ambipolar behaviour in the FeFETs can be attributed to the surface treatment of the SiO_2 layer with HMDS.

It has been demonstrated that the on/off ratio at zero top gate bias in FeFETs can be controlled using the bottom gate.[47] Hence, we introduced a second gate and characterized the performance of the dual-gate FeFET. The device layout is schematically presented in figure 1a. The drain bias was fixed at 100 mV and the gate bias on the ferroelectric top gate was swept from −50 V to +50 V and back. The source electrode was grounded. The transfer curves for three different bottom gate biases of 0 V, and ±40 V are displayed in figure 4. Application of 0 V on the non-ferroelectric bottom SiO_2 gate has no influence on the FeFET transfer characteristics, and the device shows a performance similar to figure 3. Next, a negative bias of -40 V is applied on the bottom gate. Application of a negative bias has two effects; firstly, the current for the hole accumulation regime is increased. Secondly, the current for the electron accumulated channel is reduced. The hole current is due to formation of two hole accumulation layers due to negative polarization of both the ferroelectric top and non-ferroelectric bottom gates. For the electron accumulation channel, the ferroelectric is positively polarized whereas the bottom gate is negative. The graphene layer cannot effectively screen the top and bottom potentials by supplying holes and electrons for the top and bottom channels, respectively. As a result, the bottom gate bias slightly depolarizes (by less than 10%) the ferroelectric layer.[47] Hence, the density of the accumulated electrons is reduced, and a lower electron current is measured. A similar trend, but opposite, is observed for positive bottom gate bias of +40 V; the current for the electron channel increases whereas for the hole accumulated channel the current is reduced. As a result, the on/off ratio in an EC-graphene FeFET can be controlled by applying a bias to the bottom gate, as shown in figure 4b. Moreover, despite the large voltages on the bottom gate, the displacement current peak of the ferroelectric gate remains intact, and no splitting or reduction of the peaks are observed, indicating that the bottom gate does not influence the switching voltage of the top ferroelectric gate.[48]

The time that the FeFETs can retain data in the absence of power, hence data retention time, is of particular importance for any practical applications. The FeFETs realized with electrochemically exfoliated graphene and P(VDF-TrFE) gate typically show robust retention time, as shown in figure 5. There was no significant deterioration of the on/off ratio after 10^4 seconds. The exact mechanism for slight drop in the on/off ratio over time is not clear yet. Nevertheless we speculate that polarization induced accumulated charges in the channel may also compensation of dopant anions leading to less compensation charges to stabilize polarization. As a result, the P(VDF-TrFE) layer slightly depolarizes hence leading to the observed drop in the on/off ratio.

4. Conclusions

In conclusion, we have demonstrated ferroelectric field-effect transistors based on a low-cost electrochemically exfoliated graphene flakes. The LB-film of graphene flakes shows a hole field-effect mobility of 100 cm^2/Vs. The device fabrication is compatible with low temperature processing on foils. The EC-graphene ferroelectric transistors reveal ambipolar hysteretic transfer characteristics. The single gated transistors possess robust memory characteristics. A second non-ferroelectric gate has been introduced which can advantageously control the current level in either of the electron or hole charge accumulation regimes. Biasing the bottom gate has limited influence on the polarization status of the top ferroelectric gate. FeFETs realized with P(VDF-TrFE) typically show robust performance in terms of retention time and cycle endurance.[49–51] The ferroelectric transistors with EC-exfoliated graphene are characterized by highly reproducible and well-defined hysteretic response, and can be a good candidate for non-volatile memory applications in low-cost printable electronics.

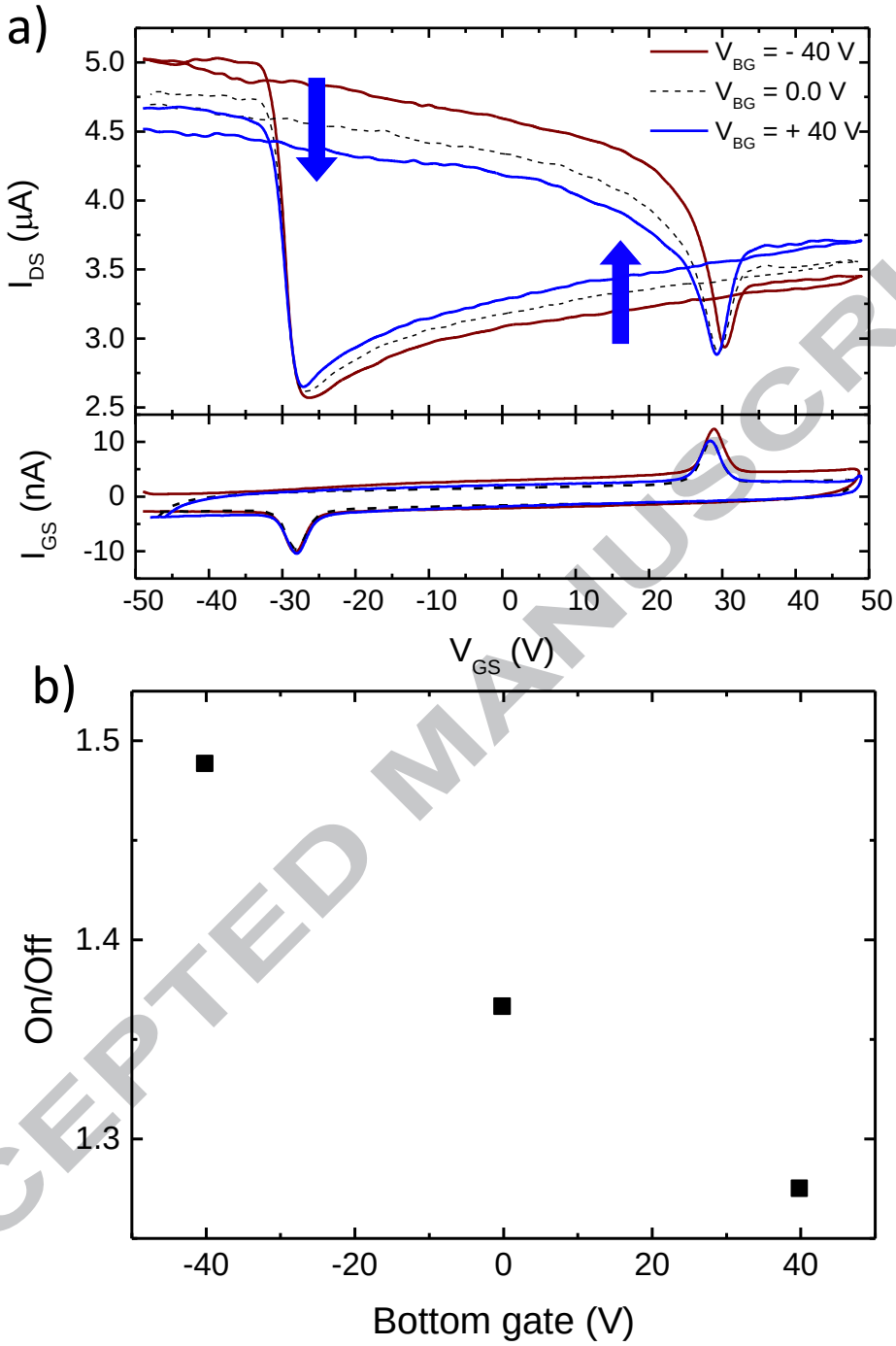


Figure 4. a) Output characteristics (top) and the displacement gate leakage current (bottom) of a dual-gate ferroelectric field-effect transistor based on EC-exfoliated graphene flakes. The current in the channel can be manipulated using a bias applied on the bottom non-ferroelectric gate. Depending on the polarity of the non-ferroelectric gate bias, electron or hole current is enhanced, as indicated by arrows in the figure. The channel length and width are 5 μm and 10000 μm, respectively. b) On/Off ratio as function of the non-ferroelectric bottom gate bias.

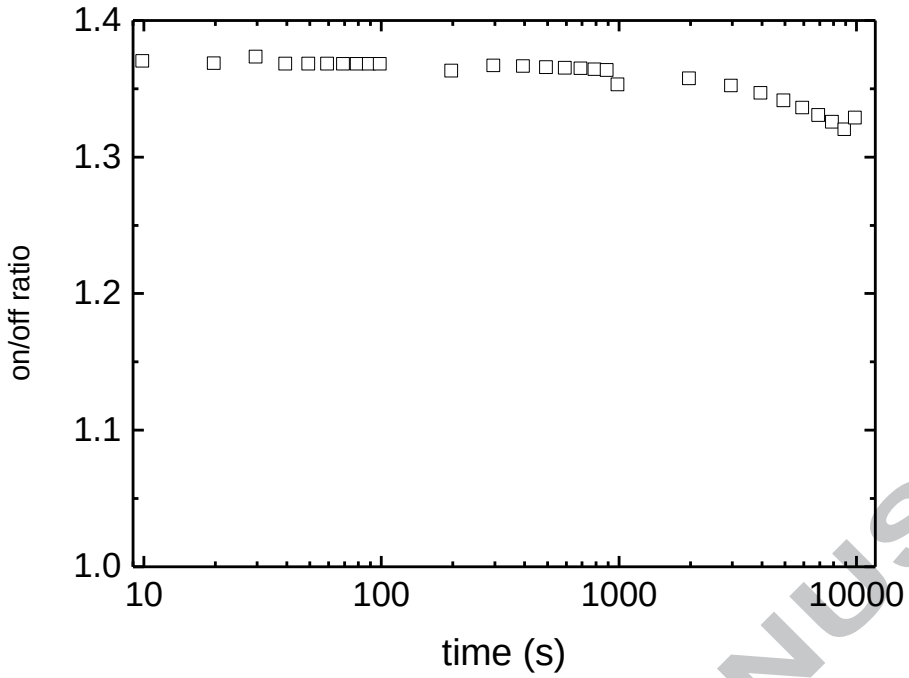


Figure 5. Retention time of the on/off ratio at zero gate bias.

Acknowledgements

K.A. acknowledges Alexander von Humboldt Foundation for the funding provided in the framework of the Sofja Kovalevskaja Award endowed by the Federal Ministry of Education and Research, Germany. The authors acknowledge Professors D. M. de Leeuw and P.W.M. Blom for fruitful discussions and the Max-Planck Institute for Polymer Research (Mainz, Germany) for the financial and technical support.

References

1 A. K. Geim and K. S. Novoselov, *Nat. Mater.*, 2007, 183.
2 P. Avouris and F. Xia, *MRS Bull.*, 2012, **37**, 1225.
3 F. Bonaccorso, Z. Sun, T. Hasan and a C. Ferrari, *Nat. Photonics*, 2010, **4**, 611.
4 F. Schwierz, *Nat. Nanotech*, 2010, **5**, 487.
5 K. S. Novoselov, a. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva and a. a. Firsov, *Science (80-.).*, 2011, **306**, 666.
6 S. A. Imam, T. Deshpande, A. Guermoune, M. Siaj and T. Szkopek, *Appl. Phys. Lett.*, 2011, **99**.
7 S. M. Kim, E. B. Song, S. Lee, J. Zhu, D. H. Seo, M. Mecklenburg, S. Seo and K. L. Wang, *ACS Nano*, 2012, **6**, 7879.
8 S. Lee, E. B. Song, S. Kim, D. H. Seo, S. Seo, T. Won Kang and K. L. Wang, *Appl. Phys. Lett.*, 2012, **100**, 23109.
9 M. Sup Choi, G.-H. Lee, Y.-J. Yu, D.-Y. Lee, S. Hwan Lee, P. Kim, J. Hone and W. Jong Yoo, *Nat. Commun.*, 2013, **4**, 1624.
10 Y. Zheng, G. X. Ni, C. T. Toh, M. G. Zeng, S. T. Chen, K. Yao and B. öZyilmaz, *Appl. Phys. Lett.*, 2009, **94**, 30.
11 H. J. Hwang, J. H. Yang, Y. G. Lee, C. Cho, C. G. Kang, S. C. Kang, W. Park and B. H. Lee, *Nanotechnology*, 2013, **24**, 175202.
12 W. Lee, O. Kahya, C. T. Toh, B. Özyilmaz and J.-H. Ahn, *Nanotechnology*, 2013, **24**, 475202.
13 Y. Zheng, G. X. Ni, C. T. Toh, C. Y. Tan, K. Yao and B. öZyilmaz, *Phys. Rev. Lett.*, 2010, **105**, 166602.
14 W. Y. Kim, H.-D. Kim, T.-T. Kim, H.-S. Park, K. Lee, H. J. Choi, S. H. Lee, J. Son, N. Park and

B. Min, *Nat. Commun.*, 2016, **7**, 10429.
15 N. Park, H. Kang, J. Park, Y. Lee, Y. Yun, J. H. Lee, S. G. Lee, Y. H. Lee and D. Suh, *ACS Nano*, 2015, **9**, 10729.
16 Y.-J. Doh and G.-C. Yi, *Nanotechnology*, 2010, **21**, 105204.
17 W. Jie and J. Hao, *Nanoscale*, 2014, **6**, 6346.
18 X. Li, W. Cai, J. An, S. Kim, J. Nah, D. Yang, R. Piner, a. Velamakanni, I. Jung, E. Tutuc, S. K. Banerjee, L. Colombo and R. S. Ruoff, *Science (80-.).*, 2009, **324**, 1312.
19 X. Wan, K. Chen and J. Xu, *Small*, 2014, **10**, 4443.
20 P. Avouris and C. Dimitrakopoulos, *Mater. Today*, 2012, **15**, 86.
21 J. Feng, W. Li, X. Qian, J. Qi, L. Qi and J. Li, *Nanoscale*, 2012, **4**, 4883.
22 S. Bae, H. Kim, Y. Lee, X. Xu, J.-S. Park, Y. Zheng, J. Balakrishnan, T. Lei, H. Ri Kim, Y. Il Song, Y.-J. Kim, K. S. Kim, B. Özyilmaz, J.-H. Ahn, B. H. Hong and S. Iijima, *Nat. Nanotechnol.*, 2010, **5**, 574.
23 Z. Y. Juang, C. Y. Wu, A. Y. Lu, C. Y. Su, K. C. Leou, F. R. Chen and C. H. Tsai, *Carbon N. Y.*, 2010, **48**, 3169.
24 J. Wang, M. Liang, Y. Fang, T. Qiu, J. Zhang and L. Zhi, *Adv. Mater.*, 2012, **24**, 2874.
25 G. Jo, M. Choe, S. Lee, W. Park, Y. H. Kahng and T. Lee, *Nanotechnology*, 2012, **23**, 112001.
26 K. R. Paton, E. Varrla, C. Backes, R. J. Smith, U. Khan, A. O'Neill, C. Boland, M. Lotya, O. M. Istrate, P. King, T. Higgins, S. Barwich, P. May, P. Puczkarski, I. Ahmed, M. Moebius, H. Pettersson, E. Long, J. Coelho, S. E. O'Brien, E. K. McGuire, B. M. Sanchez, G. S. Duesberg, N. McEvoy, T. J. Pennycook, C. Downing, A. Crossley, V. Nicolosi and J. N. Coleman, *Nat. Mater.*, 2014, **13**, 624.
27 S. Bose, T. Kuila, N. H. Kim and J. H. Lee, *Graphene*, 2014, 81.
28 J. N. Coleman, *Acc. Chem. Res.*, 2013, **46**, 14.
29 C. Y. Su, A. Y. Lu, Y. Xu, F. R. Chen, A. N. Khlobystov and L. J. Li, *ACS Nano*, 2011, **5**, 2332.
30 K. Parvez, Z. S. Wu, R. Li, X. Liu, R. Graf, X. Feng and K. Müllen, *J. Am. Chem. Soc.*, 2014, **136**, 6083.
31 K. Nagashio, T. Moriyama, R. Ifuku, T. Yamashita, T. Nishimura and A. Toriumi, in *Technical Digest - International Electron Devices Meeting, IEDM*, 2011.
32 J. a. Robinson, M. Labella, M. Zhu, M. Hollander, R. Kasarda, Z. Hughes, K. Trumbull, R. Cavalero and D. Snyder, *Appl. Phys. Lett.*, 2011, **98**, 2011.
33 K. Nagashio, T. Nishimura, K. Kita and A. Toriumi, *Appl. Phys. Lett.*, 2010, **97**.
34 E. Watanabe, A. Conwill, D. Tsuya and Y. Koide, *Diam. Relat. Mater.*, 2012, **24**, 171.
35 K. Asadi, E. C. Timmering, T. C. T. Geuns, A. Pesquera, A. Centeno, A. Zurutuza, J. H. Klootwijk, P. W. M. Blom and D. M. De Leeuw, *ACS Appl. Mater. Interfaces*, 2015, **7**, 9429.
36 Y. L. Sun, D. Xie, J. L. Xu, X. M. Li, C. Zhang, R. X. Dai, X. Li, X. J. Meng and H. W. Zhu, *Carbon N. Y.*, 2016, **96**, 695.
37 T. Furukawa, *IEEE Trans. Electr. Insul.*, 1989, **24**, 375.
38 A. J. Lovinger, *Science (80-.).*, 1983, **220**, 1115.
39 Y. J. Park, I. S. Bae, S. Ju Kang, J. Chang and C. Park, *IEEE Trans. Dielectr. Electr. Insul.*, 2010, **17**, 1135.
40 K. Asadi, M. Li, P. W. M. Blom, M. Kemerink and D. M. De Leeuw, *Mater. Today*, 2011, 14, 592–599.
41 R. C. G. Naber, C. Tanase, P. W. M. Blom, G. H. Gelinck, A. W. Marsman, F. J. Touwslager, S. Setayesh and D. M. de Leeuw, *Nat Mater*, 2005, **4**, 243.
42 J. F. Legrand, *Ferroelectrics*, 1989, **91**, 303.
43 S. H. Bae, O. Kahya, B. K. Sharma, J. Kwon, H. J. Cho, B. Özyilmaz and J. H. Ahn, *ACS Nano*, 2013, **7**, 3130.
44 L. Buglione, E. L. K. Chng, A. Ambrosi, Z. Sofer and M. Pumera, *Electrochem. commun.*, 2012, **14**, 5.
45 L. Chua, J. Zaumseil, J. Chang, E. C.-W. Ou, P. K.-H. Ho, H. Sirringhaus and R. H. Friend, *Nature*, 2005, **434**, 194.

46 K. Parvez, R. Li, S. R. Puniredd, Y. Hernandez, F. Hinkel, S. Wang, X. Feng and K. Müllen, *ACS Nano*, 2013, **7**, 3598.

47 I. Katsouras, D. Zhao, M.-J. Spijkman, M. Li, P. W. M. Blom, D. M. De Leeuw and K. Asadi, *Sci. Rep.*, 2015, **5**, 12094.

48 K. Asadi, P. W. M. Blom and D. M. De Leeuw, *Appl. Phys. Lett.*, 2011, **99**.

49 R. C. G. Naber, K. Asadi, P. W. M. Blom, D. M. De Leeuw and B. De Boer, *Adv. Mater.*, 2010, **22**, 933.

50 J. J. Brondijk, K. Asadi, P. W. M. Blom and D. M. De Leeuw, *J. Polym. Sci. Part B Polym. Phys.*, 2012, **50**, 47.

51 D. Zhao, I. Katsouras, M. Li, K. Asadi, J. Tsurumi, G. Glasser, J. Takeya, P. W. M. Blom and D. M. de Leeuw, *Sci. Rep.*, 2014, **4**, 5075.

Jonas Heidler received his MSc. degree from RheinMain University of Applied Sciences, Germany. He did his research thesis on fabrication and simulation of graphene ferroelectric memories. He is currently pursuing his PhD degree at the Paul Scherrer Institute in Switzerland.

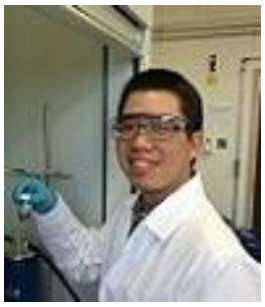
Sheng Yang studied as a PhD student at the Max-Planck-Institute for Polymer Research in Mainz since September 2013. Starting from March 2016 he shifted his study to Prof. Feng's group in TU Dresden. His main interest is the exfoliation of 2D materials from solutions and the applications in electronics.

Xinliang Feng received his PhD degree in 2008 at the Max Planck Institute for Polymer Research, and subsequently was appointed as a group leader. He became a distinguished group leader at the Max-Planck Institute for Polymer Research in 2012. He is now at the Technical University of Dresden, Germany. His current scientific interests include graphene, two-dimensional nanomaterials, organic conjugated materials, and carbon-rich molecules and materials for electronic and energy-related applications.

Klaus Müllen received his PhD degree at the University of Basel in 1972. He received his habilitation in 1977 at ETH, Zürich. In 1979 he became a Professor at the University of Cologne, and in 1983 at the Johannes-Gutenberg-University, Mainz. He joined the Max Planck Society in 1989 as one of the directors of the Max Planck Institute for Polymer Research. His broad research interests range from the development of new polymer-forming reactions, including methods of organometallic chemistry, to the chemistry and physics of small molecules, graphenes, dendrimers and biosynthetic hybrids, formation of multi-dimensional polymers, architectures, nanocomposites, and molecular materials with liquid crystalline properties for electronic and optoelectronic devices.

Kamal Asadi received his PhD degree in solid-state physics from University of Groningen, the Netherlands. He joined Royal Philips Electronics in The Netherlands as a research scientist. His work at Philips was focused on the investigation of metal-oxides, ferroelectrics and graphene for opto-electronic applications. In 2014 he moved to Max-Planck Institute for Polymer Research with the prestigious Sofja Kovalevskaja Award. His current research interests are electro-active polymers, magnetic nanopartciles, graphene, metal oxides and organic multi-ferroics.


Jonas Heidler


Sheng Yang


Prof. Xinliang Feng


Prof. Klaus Müllen


Dr. Kamal Asadi

Highlights

Solution processed graphene ferroelectric field-effect transistor memories have been demonstrated based on electrochemically exfoliated graphene, and ferroelectric polymers.

The on/off ratio in the graphene FeFET can be tuned by a second non-ferroelectric gate.

Graphene ferroelectric field-effect transistors showed good memory performance such as long retention time.