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Implementation of application specific soft-core architecture for switching converters☆

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ABSTRACT

Application Specific Processors (ASPs) are used in many areas. In this paper, an application specific soft-core processor for control of switching power converters is designed and implemented. The proposed designed architecture is constructed based on fixed-point arithmetic with minimal functional units. The control algorithm, which is used in this architecture, is Finite-Set Model Predictive Control (FS-MPC). The proposed soft-core processor is coded in VHSIC Hardware Description Language (VHDL) and implemented on Field-Programmable Gate Array (FPGA) platform. This architecture consists of minimum functional unit with only two adders and two multipliers, a control unit and a selection unit. The designed architecture is general and low cost and can be used in any type of converters. In this paper the functionality of the processor is examined by three types of converters namely three-phase inverters, dual transistor forward converter and active front end rectifier. In comparison with other controllers, output results indicate the accuracy of proposed architecture.

1. Introduction

General-purpose processors are capable of performing various applications and tasks. They can be inefficient in terms of implementation costs, particularly for devices that are designed to execute special operations. Moreover, general-purpose processors show low performance in computationally intensive applications. Therefore, Application Specific Processors (ASP) appeared as a solution for high performance and low-cost processors. ASPs can be found approximately in each device we use on a daily basis such as TVs, cell phones, GPSs, few to mention.

An ASP is specifically designed for an application in which high performance, low cost, and low power consumption are required. There are two types of ASPs: hard-core processor and soft-core processor. A hard-core processor cannot be reconfigured after fabrication and after fabrication, all its modules are fixed. Soft-core processors, on the other hand, are systems which can be deployed on programmable logic ICs, such as Field Programmable Gate Arrays (FPGAs). In this type of systems, the processor and its surrounding peripherals are created by using the available resources on a programmable logic device and which can be modified according to any specific set of requirements. Main benefits of soft-core system are flexibility, easy for verification and visibility to signal behaviors. Famous soft-core processors are Dossmatik [1], MCL51 [2],

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Nios [3], Cortex-M1 [4], Leon2 [5], PicoBlaze [6] and LatticeMico8 [7]. Some applications of soft-core processors are in video and image processing [8], internet of things [9], energy harvesting [10] and signal processing [11].

Switching power converters are one of the active research areas in electronics, which covers a wide range of applications, from low current/low voltage such as energy harvesting systems to high power/current applications [12]. Different control algorithms for power converters have been widely studied, and new methods are developed and introduced continuously. Some of these new schemes are hysteresis, linear controls, fuzzy, neural networks, neuro–fuzzy, sliding mode, adaptive control and predictive control [13].

Design and implementation of a controller for these algorithms can be a challenge in practice, as they need to be easy to use, flexible, low-cost, reliable, and low power. This area is considered as a multi-disciplinary, which requires knowledge of power electronic, control and hardware design; therefore, efficiency of the implemented hardware is usually overlooked. Most of reported research works in this field utilize off-the-shelf digital controllers/processors, for power converters. In comparison with other devices, off-the-shelf microcontrollers are cheap, easy to use, but offer low computation resources and are inflexible in terms of accuracy and speed. In addition to the general-purpose microcontrollers, in recent years, FPGAs also have been widely used as a preferred platform for the digital controller implementation. FPGA implementations are mostly synthesized using standard synthesizers and are not resource optimized. Using general-purpose soft-core is rather easy, more flexible compared with microcontrollers, but might not meet the specific requirements of a design, such as speed, power consumption and reliability, where, more efficient design approach requires hardware design and optimization knowledge.

In this paper, an application specific soft-core processor for control of switching power converters is designed and implemented. To the authors' best of knowledge, this is the first Power-Switching Application-Specific-Processor (PS-ASP). This architecture considers essential requirements of power switching controllers for practical applications. The major subject in the former methods, however, is their hardware design procedure. Since hardware design for control algorithms is a multi-threaded process, it is challenging for power electronics engineers to solve both control algorithm issues and hardware design efficiency at the same time. Our method offers a new solution to this problem. We are introducing a design method based on a predefined soft-core architecture in which the hardware datapath is synthesized. This approach provides a solution for power electronics engineers by which they can design efficient control hardware with minimum cost. This is different from a microcontroller-based approach which is limited to the hardware resources available on the microcontroller chip. Also, it is different from other FPGA-based approaches and automatic synthesis tools, which either offer simplified drag and synthesis methods by hiding design complexity or offering a large amount of hardware and FPGA parameters and professional design details.

The implemented architecture is optimal in terms of utilized resources (only two adders and two multipliers), which makes it an effective nominee for an integrated circuit implementation of this processor.

Proposed architecture details are presented, which give the transparency to future designers to acquire this design approach and to apply modifications for further improvements and/or industrial applications. With this approach, the proposed processor design is optimum in terms of minimizing required hardware components. Furthermore, other features of this processor are reusability for modified switching circuits, flexibility and generality which results in an easy use of any type of switching converters.

This paper is organized as follows: The review of previous works is presented in Section 2, the proposed architecture is described in Section 3, the implementation examples and implementation results are presented in Sections 4 and 5 respectively followed by the conclusion in Section 6.

2. Review

There are different techniques for control algorithms implementation. The primary controllers were analogue, and in fact they were PID controllers with operational amplifiers. Recently most of control algorithms are digitally implemented, and analogue controllers are only applied when utterly essential. Digital controllers can be divided into hardware and software-based implementations [13].

Software based approaches use microprocessors and/or microcontrollers to implement the computational algorithms (hard-core processors). In this technique, all instructions are executed sequentially; as a result, one of the challenges for complex systems is real-time implementation. This type of controllers has a medium reliability, medium flexibility, low cost and low/medium ability to implement advanced algorithms [14].

In [15] an adaptive control of buck converter has been implemented using a microcontroller (ARM Cortex M4). A DC-DC boost converter with micro-computer controlled maximum power point tracking (MPPT) has presented in [16]. A method for measurement of DC-Link voltage for power converter systems by using a TMS320F28335 microcontroller in [17] is introduced. Here by applying synchronization to DC-link voltage sampling and A/D conversion via PWM modulator, strong electromagnetic noises are avoided. In [18] a digital controller IC for single and dual-phase DC-DC switching converters is introduced. In steady-state the controller works as a digital PWM controller and during transient it activates the duty ratio correction logic.

In hardware-based approaches, controllers are implemented using Complex Programmable Logic Devices (CPLDs) and FPGAs (soft-core processors). Particularly FPGAs, which consist of logic elements, can implement many operations in parallel.

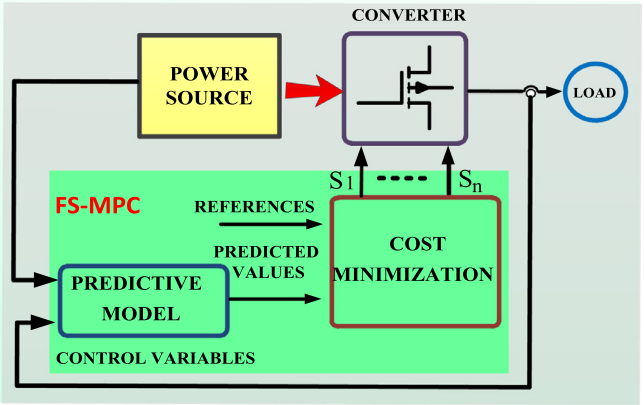

Fig. 1. FS–MPC in switching power converters.

Therefore, matched to software-based techniques, the computation time is generally lower. Other features of this kind of controllers are reliability, high flexibility, low cost and high ability to implement advanced algorithms [14].

In [19] a predictive control for three-phase four-leg inverter is presented and implemented on a dSPACE DS1104 platform. Output results indicate a low precision while digital controller is not optimized.

A dual transistor forward converter is presented in [20] in which transient performance has been improved by using a digital controller for charge balance. Unfortunately, presented results show low precision for high current step changes.

In [21] a digital control algorithm for an active front end rectifier by applying model predictive control is represented. This technique presents an improvement in switching power electronic converters, which greatly rely on the advancement of novel control algorithms and the implementation methods of the new algorithms.

Model Predictive Control (MPC) is an extensive class of various control schemes [22]. In this method, performance of the system, for a specific set of objective variables, is calculated up to a definite prediction horizon. Accordingly, an optimal sequence of values for the objective variables are determined using a cost function. There are studies about application of MPC in switching converters in which control algorithms is digitally implemented for one kind of converters such as AC-DC, DC-DC or DC-AC [23].

This research presents design and implementation of a low-cost soft-core architecture for switching power converters. Proposed architecture consists of fixed-point arithmetic and minimal functional units. The control algorithm, which is used in this architecture is a Finite-Set Model Predictive Control (FS-MPC). The proposed design is evaluated, and its functionality is assessed for various word-lengths.

3. The proposed architecture

This section presents the proposed soft-core architecture. There are several factors to determine various units in an architecture, such as hardware cost, computational accuracy, sampling frequency, speed, control algorithm complexity, and usability. For instance, if precision is the design goal, the word-length must be increased, which will result in a higher implementation cost, or if sampling frequency needs to be increased, the speed of the processer should be increased too, which means number of required arithmetic units and final system cost will increase. If control algorithm is complex the architecture should finish the computation in the sampling interval, accordingly more parallelism is required which results in a higher number of functional units and system cost.

In this work predictive control is adopted as our main control algorithm. One of the advantages of the predictive control is the elimination of modulator stage. In other control schemes, such as PWM, a modulator produces the switching state, but in this technique the optimum switching state is determined and applied to the power switches using a cost function. One kind of model predictive control is FS-MPC [22], which is suitable for systems with discrete nature. Therefore, since the switching power converters are analysed in a discrete space, the FS-MPC would be a very strong candidate. A general block diagram for FS-MPC in switching power converters is depicted in Fig. 1. According to this figure, the current values of the control variables are measured, and their future values are predicted based on a set of mathematical equations implemented in the predictive model block. Since the number of switches (S_i) is n and each switch can be ON or OFF, there are 2^n switching states. In the cost minimization section by applying cost function for all switching states, the state that minimizes the cost function is selected and applied to the switches. Cost function is defined as:

$$g = \sum_{All\ \ Variables} |P - P^*|, \tag{1}$$

where, P is predicted value and P^* is its reference value.

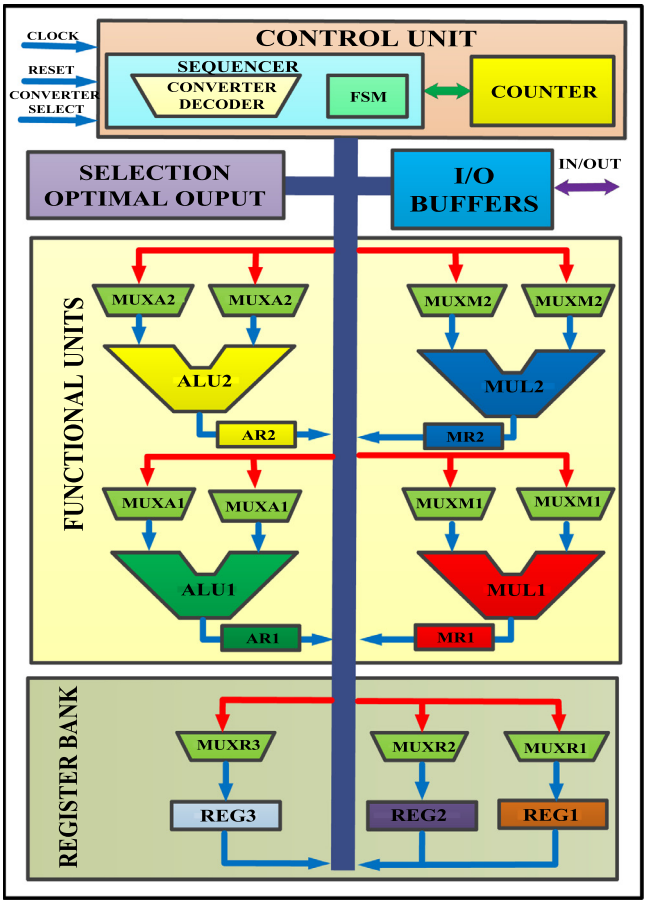

Fig. 2. Proposed architecture.

Now the objective is to design a processor which provides a trade-off between hardware design costs and requirements of the FS-MPC algorithm. The proposed architecture is depicted in Fig. 2, which consists of different blocks as follows.

- Functional Units (FU): this section is responsible for computing cost function(s), which consists of two multipliers (MUL), two adders (ALU) and eight multiplexers (MUX). At the output of each adder and multiplier, there is a register (AR1, AR2, MR1, MR2) to store the output to be used in the next states.
- Register Bank (RB): this is a temporary memory to save output of the FUs. This block consists of three registers (REG) and three multiplexers (MUX).
- I/O Buffers (IOB): input and output of data are controlled by these buffers. Buffers are temporary memories to hold output or input data while they are transported.
- Control Unit (CU): It manages other units by providing timing and control signals. This is a sequential circuit consist of a counter and sequencer.
- Counter (CR): this section is an n-bits counter, which provides 2^n switching states, where n is the number of converter switches.
- Sequencer (SQ): in this unit, there are Finite-State Machine (FSM) and a converter decoder. FSM provides appropriate control signals for datapath units. For proper decoding of control commands and selects a converter, a decoder is utilized in this block. This decoder is selected by input keys (CONVERTER SELECT).
- Selection (SEL): in this block by comparing calculated cost functions for all switching states, the state which produces minimum cost function is selected as optimal switching state and finally is sent to the output buffers.

This application specific soft-core architecture is coded in VHDL and synthesized on an Altera cyclone IV and Xilinx Virtex II platforms as a proof. The architecture is flexible in terms of word-length of the functional units. Word-length is defined by user. In Table 1 resource usages for various word-lengths are presented. According to this table there is a trade-off between word-length and hardware cost. Accuracy of computation has a great impact on output quality and even on stability of the output. To interface with this architecture, instruction sets are introduced as shown in Table 2. These instructions are defined based on functional units and necessary operations in the control algorithm.

Table 1
Results of used resources in terms of word-length.

Word- length		40	32	22	16	15	8	7
Area (Slice)	**Multiplier**	168	133	103	72	67	34	33
	Adder	60	48	38	29	26	16	14

Table 2
Instruction set for processor programing.

INSTRUCTION	DESCRIPTION
ADD1 *a,b*	Addition of *a* and *b*. The result is saved in AR1.
ADD2 *a,b*	Addition of *a* and *b*. The result is saved in AR2.
MUL1 *a,b*	Multiplication of *a* and *b*. The result is saved in MR1.
MUL2 *a,b*	Multiplication of *a* and *b*. The result is saved in MR2.
MOV *a,b*	Copy *b* to *a*.
In *a*	Input data to *a*.
Out *a*	Output data to *a*.
If then	If condition, then operation

4. Case studies

One of the features of the proposed soft-core processor is generality, which lets users to utilize it in many kinds of converters. In this research, we examine the proposed processor in three types of converters:

- DC to AC converter (three-phase four-leg inverter)
- DC to DC converter (dual transistor forward converter)
- AC to DC converter (active front end rectifier)

In the following sections by analysing the converters we find a mathematical model for predictive control and finally digital implementation of corresponding controller.

4.1. DC to AC converter (three-phase four-leg inverter)

A Three-phase two-level four-leg inverter is shown in Fig. 3a. In this topology S_u,S_v,S_w and S_x are the switching states that are selected by predicting model. The fourth-leg is coupled to the neutral point of the load through the *R–L* filter, permitting for controllability of the zero-sequence current/voltage [23]. By applying mathematical analysis, the operation of the inverter can be expressed as:

$$v_{mN} = s_m v_{dc},\ m = u, v, w, x, \tag{2}$$

$$v_{mN} = \left(R_{fm} + R_m\right) i_m + L_{fm}\frac{di_m}{dt} + v_{nN}\ , m = u, v, w, \tag{3}$$

$$\frac{di_m}{dt} = \frac{1}{L_{fm}}\left[(v_{mN} - v_{nN}) - \left(R_{fm} + R_m\right) i_m\right] m = u, v, w, x, \tag{4}$$

Based on (2) and (4), the load neutral voltage V_{nN} can be expressed as follows:

$$V_{nN} = L_{eq} v_{dc} \sum_{m=u,v,w,x} \frac{S_m}{L_{fm}} - L_{eq} \sum_{m=u,v,w,x} \frac{R_{fm} + R_m}{L_{fm}}, \tag{5}$$

$$L_{eq} = \left(\sum_{m=u,v,w,x} \frac{1}{L_{fm}}\right)^{-1}, \tag{6}$$

$$\sum_{m=u,v,w,x} i_m = 0 \tag{7}$$

$$\frac{di_m}{dt} = \frac{i_m(k+1) - i_m(k)}{T_s},\ m = u,\ v,\ w, \tag{8}$$

where, T_s is sampling time. According to the above equations, the discrete model of the inverter is given by

$$i_m(k+1) = \frac{T_s}{L_{fm}}\left[(v_{mN} - v_{nN}) - \left(R_{fm} + R_m\right) i_m(k)\right] + i_m(k),\ m = u, v, w \tag{9}$$

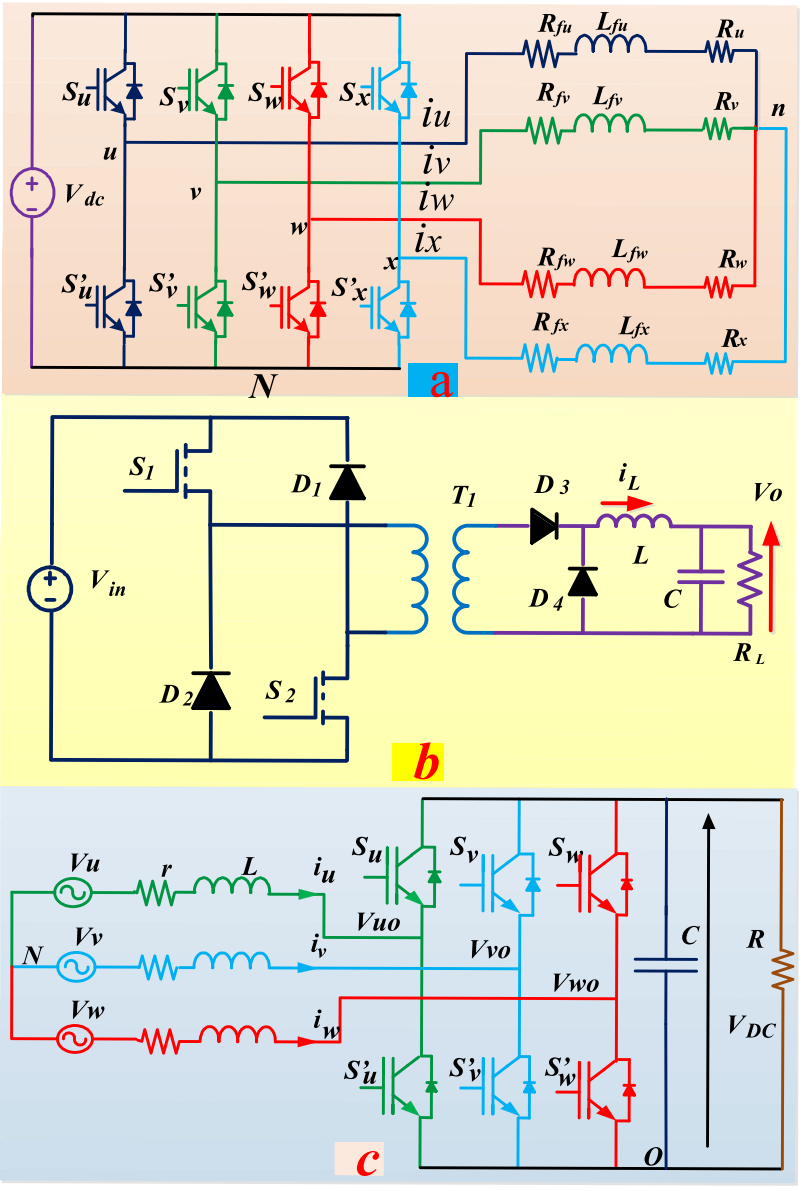

Fig. 3. Three type of converters. (a) Three-phase four-leg inverter. (b) Dual transistor forward converter. (c) Active front end rectifier.

The current error for each input can be defined as:

$$e_m = i_m^*(k+1) - i_m(k+1) \tag{10}$$

where, i_m^* is the reference current. The cost function is calculated by:

$$g = \sum_{m=u,v,w} |e_m|, \tag{11}$$

The arithmetic structure (scheduling) for computing cost function is depicted in Fig. 4a. This scheduling is matched to the proposed architecture, which contains two adders, two multipliers and three registers. There are 11 states to calculate cost function. All coefficients in this diagram have been derived from Eq. (9). According to the Fig. 4a the instruction set for programming the processor in the first three states are represented in Fig. 5.

4.2. DC to DC converter (dual transistor forward converter)

A Dual Transistor Forward Converter (DTFC) is depicted in Fig. 3b. The main control objectives in this converter are minimizing transient time, as well as overshoot/undershoot in the output voltage under load variations. The transient time

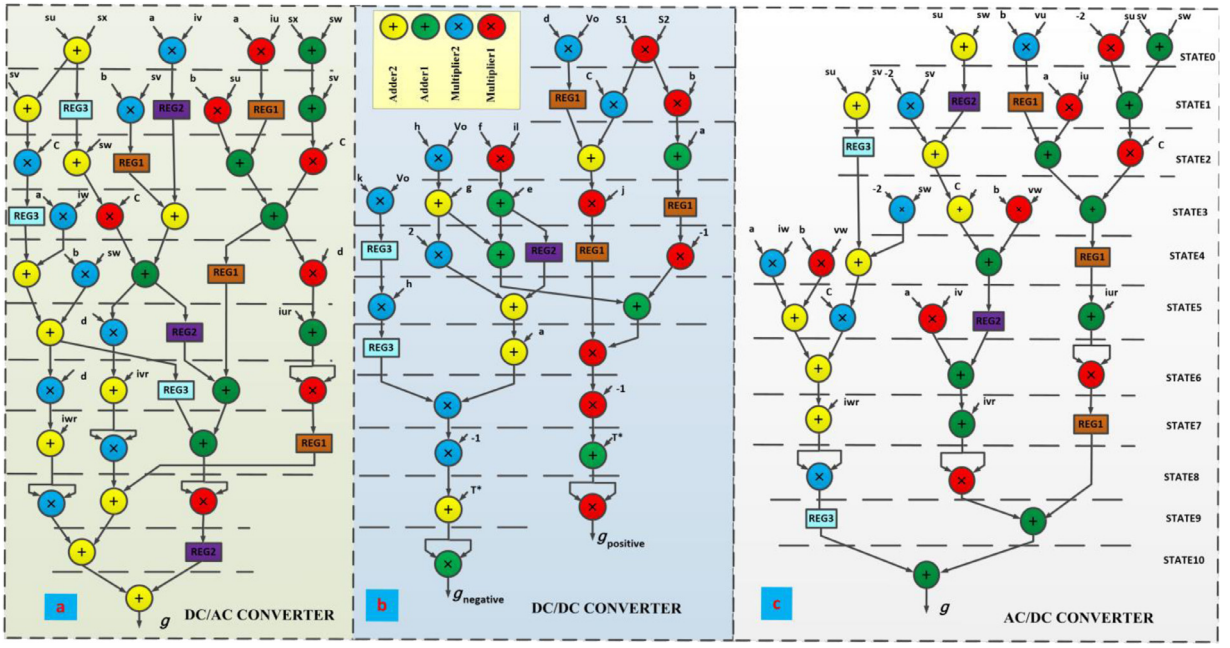

Fig. 4. Arithmetic structure for computing cost function. (a) DC/AC converter. (b) DC/DC converter. (c) AC/DC converter.

STAT0: ADD1 SW,SX/ MUL1 iu,a / MUL2 iv,a/ ADD2 SX,SU;
STATE1: ADD1 AR1,Sv/ MOV REG1,MR1/ MUL1 Su,b/ MOV REG2,MR2/ MUL2 Sv,b/ MOV REG3,AR2/ ADD2 AR2,Sv;
STATE2: MUL1 c, AR1/ ADD1 REG1,MR1/ MOV REG1,MR2/ ADD2 Sw,REG3/ MUl2 c,AR2;

Fig. 5. Instruction set for a three-phase inverter.

is calculated by Charge Balance Control (CBC) technique [20]. In the following, the summary of this approach is represented. Eq. (12) presents the basic theory of CBC.

$$v_c(t_b) - v_c(t_a) = \frac{^{i}cavrege}{C} = 0 \rightarrow \frac{\int_{t_a}^{t_b} i_c(t)dt}{t_b - t_a} = 0, \tag{12}$$

In this equation, t_a and t_b are the beginning and end of the transition time respectively. This equation points to the DC output voltage as fits to the reference voltage after a transition time, furthermore, if at time t_b the current i_L matches to the new load current, the circuit would be settled down from a transient time. In Fig. 6 the performance of DTFC under load current varying is depicted. In Fig. 6a output current and output voltage in positive steps is shown. Our aim is to compute T_1, T_2 and T_3 by applying CBC approach and to minimize them. For this purpose, the discharge section (A_1) and the recharge section (A_2) must be calculated initially. These sections have indeterminate shapes; thus, the easiest way is to approximate them by triangles (A'_1, A'_2), as depicted in Fig. 6b [24]. The mathematical computations are represented briefly as

$$i_{o2} = \frac{1}{2}(i_{L1} + i_{L2}) - 2\frac{C}{T_s}(v_{o2} - v_{o1}) \tag{13}$$

$$\frac{di_L}{dt}|_{rise} = \frac{S_1 S_2 n v_{in} - 2v_o}{2L} = m_1, \quad \frac{di_L}{dt}|_{fall} = -\frac{v_o}{L} = -m_2, \tag{14}$$

where, n is the turn's ratio of the transformer and S_1,S_2 are switching states that have values 0 and 1.

$$T'_1 = \frac{i_{o2} - i'_{L1}}{m_1}, \; A'_1 = \frac{1}{2}T'_1\left(i_{o2} - i'_{L1}\right) \tag{15}$$

$$i'_{L1} = i_{L1} + \frac{S_1 S_2 n v_{in}}{L}\frac{T_s}{8} \tag{16}$$

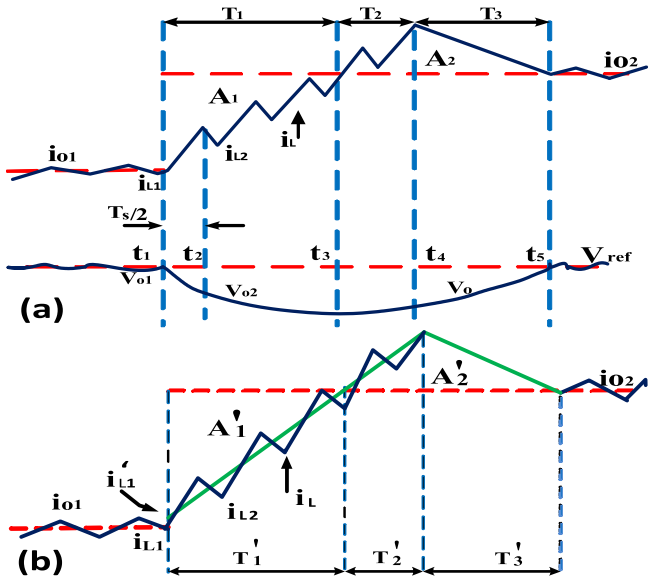

Fig. 6. *Operation of the DTFC.* (**a**) Outputs in positive step change. (**b**) Approximation of A_1 and A_2 for positive step[24].

To have a CBC algorithm, A'_1 must equal toA'_2.

$$A'_2 = \frac{1}{2}\left(T'_2 + T'_3\right)(i_{L3} - i_{o2}),\ i_{L3} = i_{o2} + m_2 T'_3 = i_{o2} + m_1 T'_2 \tag{17}$$

$$\frac{T'_2}{T'_3} = \frac{m_2}{m_1} \tag{18}$$

$$T'_2 = \sqrt{\frac{A'_1}{K}},\ K = \frac{m_1(m_2 + m_1)}{2m_2},\ T'_3 = \frac{m_1}{m_2} T'_2 \tag{19}$$

T_2 and T_3 can be realized as

$$T_2 = T'_2 - \frac{T_s}{4}, T_3 = T'_3 + \frac{T_s}{4} \tag{20}$$

$$T_{tran} = T_1 + T_2 + T_3 = \frac{i_{o2} - i'_{L1}}{m_1}\left(1 + \sqrt{1 + \frac{m_1}{m_2}}\right) \tag{21}$$

According to Taylor expansion

$$T_{tran} \approx 2\frac{i_{o2} - i'_{L1}}{m_1} \tag{22}$$

For negative load, current step changes, similar to positive step, we can analyse the system and calculate the transient time. Therefore, it can be achieved as

$$T_{tran} \approx 2\frac{i_{L1} - i_{o2}}{m_2} \tag{23}$$

and the cost function is defined as

$$g = \sum |T - T^*| \tag{24}$$

where, T is predicted transient time and T^* is its reference. The arithmetic structure for calculation of cost function in negative and positive load step changing is shown in Fig. 4b. In this scheduling, the numbers of states for computing cost function in positive and negative changes are 10 and 11 states respectively. The numbers of functional units are matched to proposed architecture. According to the Fig. 4b the instruction sets for programming the processor in the first three states are represented in Fig. 7.

STAT0: MUL1 S1,S2/ MUL2 Vo,d;
STATE1: MUL1 b,MR1/ MUL2 MR1,c/ MOV REGa,MR2;
STATE2: ADD1 a,MR1/ ADD2 MR2,REG1/ MUL1 iL,f/ MUl2 Vo.h:

Fig. 7. Instruction set for dual transistor forward converter.

STAT0: ADD1 SW,SV/ MUL1 Su,-2 / MUL2 Vu,b/ ADD2 SW,SU;
STATE1: ADD1 AR1,MR1/ MUL1 iu,a/ MOV REG1,MR2/ MOV REG2,AR2/ MUL2 Sv,-2/ ADD2 Sv,Su;
STATE2: MUL1 c, AR1/ ADD1 MR1,REG1/ ADD2 REG2,MR2/ MOV REG3,AR2;

Fig. 8. Instruction set for active front end rectifier.

4.3. AC to DC converter (active front end rectifier)

The Active Front End (AFE) rectifier is shown in Fig. 3c. In the following, the mathematic model of the converter is represented [20].

$$V_m = ri_m + L\frac{di_m}{dt} + V_{m0} + V_{0N}\, m = u,\ v,\ w \tag{25}$$

$$V_{0N} = \frac{V_{u0} + V_{v0} + V_{w0}}{3} \tag{26}$$

$$V_{u0} = S_u V_{dc},\ V_{v0} = S_v V_{dc},\ V_{w0} = S_w V_{dc} \tag{27}$$

where, S_u,S_v,S_w are switching states.

$$L\frac{di_u}{dt} = -ri_u + V_u - \frac{1}{3}(2S_u - S_v - S_w)V_{dc} \tag{28}$$

$$L\frac{di_v}{dt} = -ri_v + V_v - \frac{1}{3}(-S_u + 2S_v - S_w)V_{dc} \tag{29}$$

$$L\frac{di_w}{dt} = -ri_w + V_w - \frac{1}{3}(-S_u - S_v + 2S_w)V_{dc} \tag{30}$$

$$\frac{di_m}{dt} = \frac{i_m(k+1) - i_m(k)}{T_s},\ m = u, v, w \tag{31}$$

Similar to Eqs. (9), (10) and (11) the cost function can be calculated.

The arithmetic structure (scheduling) for computing cost function is shown in Fig. 4c. This scheduling is matched to proposed architecture, which contains two adders, two multipliers and three registers. There are 11 states to calculate the cost function. The instruction sets for programming the architecture in the first three states are depicted in Fig. 8.

5. Implementation results

In this section, fixed-point based processor is examined in the proposed converters and output results for various circuit situations and different word-lengths are presented. Each Word-Length (WL) composed of integer length and fraction length. One bit is considered as a sign bit. Word-length, integer length and fraction length have been selected based on nature of numbers and corresponding computations.

5.1. DC to AC converter

In this section the precision of designed processor for a three-phase inverter is presented. According to Figs. 1,3c the processor connects to the converter. Output currents (i_u,i_v,i_w) and DC- link voltage (v_{dc}) are inputs and optimum switching states (s_u,s_v,s_w,s_x) are outputs. For this objective, balanced and unbalanced load situations are verified. In each case, various word-lengths with several integer and fraction lengths are considered. In each word-length one bit is considered as sign bit.

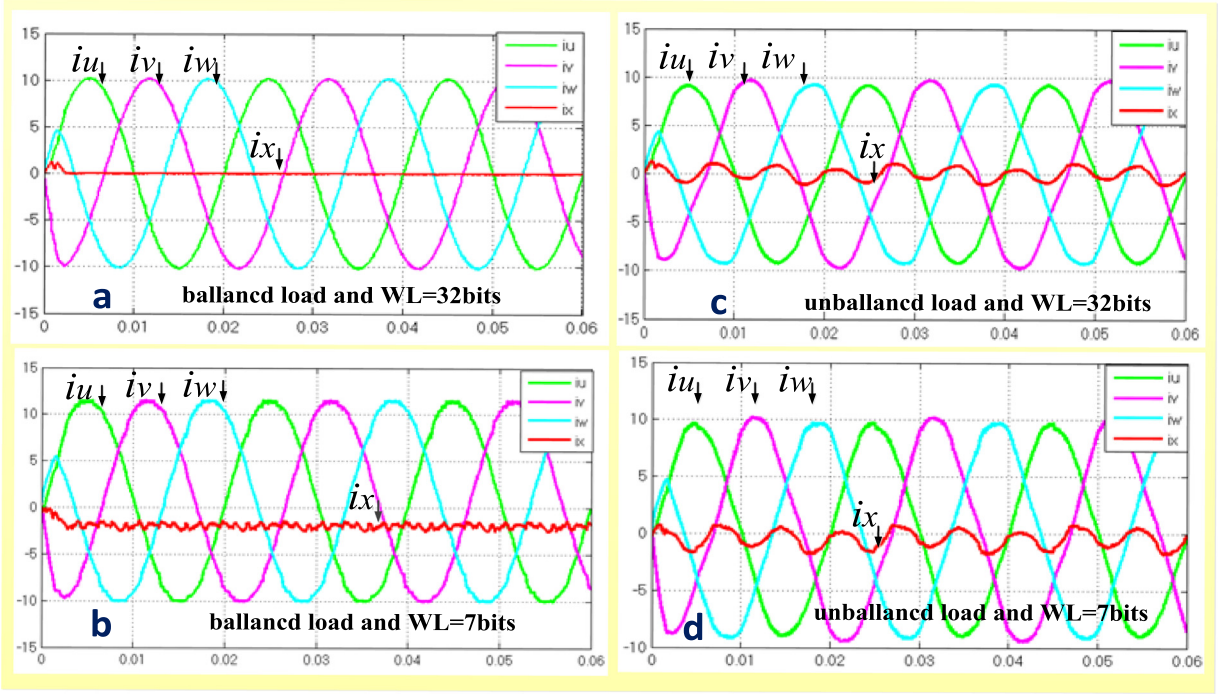

Fig. 9. Operation of three-phase inverter with proposed processor for various situations.

Here word-lengths are between 32 bits and 7 bits. Word-lengths greater than 32 bits result in higher implementation costs and have no effect on system accuracy. With word-lengths smaller than 7 bits, on the other hand, precision is unacceptable. Therefore, there is a trade-off between the output precision, word-length and hardware cost.

In this inverter, the frequency of output current is 50 HZ, the DC voltage (V_{dc}) is 150 v, the filter resistance (R_f) is 0.05 Ω, the filter inductance (L_f) is 6 mH and sampling time (T_s) is 50 μs. Output results for four states are depicted in Fig. 9. For balanced load (R = 2.5 Ω) output currents for word-lengths 32 and 7 bits are shown in Fig. 9a and b respectively. Here by using total harmonic distortion (THD) and DC component, the precision of output results is verified. In Fig. 9a, integer length is 15 bits and fraction length is16 bits. THD of each phase current is 0.43% and DC component approximately is zero. Output results show good accuracy of designed system for this state.

In Fig. 9b, THD of phase currents are different, and their values are 3.08%, 2.93% and 2.75% for i_u, i_v and i_w respectively. Here the accuracy of system is decreased, so the current of fourth-leg is not zero and its rms value is 0.63 A. The DC component for i_u is 0.14 A. Integer and fraction lengths are 4 and 2 bits. In Fig. 9c and d output currents for unbalanced conditions are depicted. In these states, R_u, R_v and R_w are 5, 3.5 and 4 Ω respectively. In Fig. 9c word-length is 32 bits, integer and fraction lengths are 15 and 16 bits. Here, THD for i_u is 3.32%, for i_v is 6.2% and 3.2% for i_w. The rms value of i_x is 0.63 A. The DC component for i_u is 0.03 A. In Fig. 9d, THD of phase currents are 4.1%, 6.5% and 4.1% for i_u, i_v and i_w respectively. Here the amplitude of different phases is not equal, so the precision of outputs is reduced. The DC component for i_u is 0.12 A and $i_{x(\mathrm{rms})}$ is 0.87 A. Integer length is 4 bits and fraction length is 2 bits. The results of this work are compared with results in [25]. In balanced load conditions the minimum THD in this work is 0.43% and in [25] is 4.21%.

5.2. DC to DC converter

In this section, results for the implemented processor in DC to DC converter which is depicted in Fig. 3b are presented. The main control objective is to minimize settling time and overshoot/undershoot in the output voltage. In this circuit, $V_{in} = 20$ v, $f_s = 250$ kHz, $C = 100$??f, $L = 15$??H and $V_o = 5$ v. Output voltage (Vo) and inductor current (i_L) are inputs and optimum switching states (S_1, S_2) are outputs. Here negative and positive load current step changes are verified. In this circuit if current step change is greater than 3 A then deviation in output voltage will be seen, which shows the accuracy of proposed architecture. Output results for various conditions are depicted in Fig. 10. Word-lengths are considered between 40 bits and 22 bits. According to this figure if negative current change is occurred in the circuit, so overshoot in the output voltage will be observed. In Fig. 10a, load current changes from 5 A to 1 A (negative step). In Fig. 10b word-length is 40 bits, settling time is 25??s and overshoot is 0.25 v. Here integer length and fraction length are 17 bits and 22 bits respectively. In Fig. 10c word-length is 22 bits, settling time is 140??s and overshoot is 0.5 v. Here integer length and fraction length are 4 bits and 17 bits respectively. In Fig. 10d, load current change from 1 A to 5 A (positive step) thus there is undershoot in

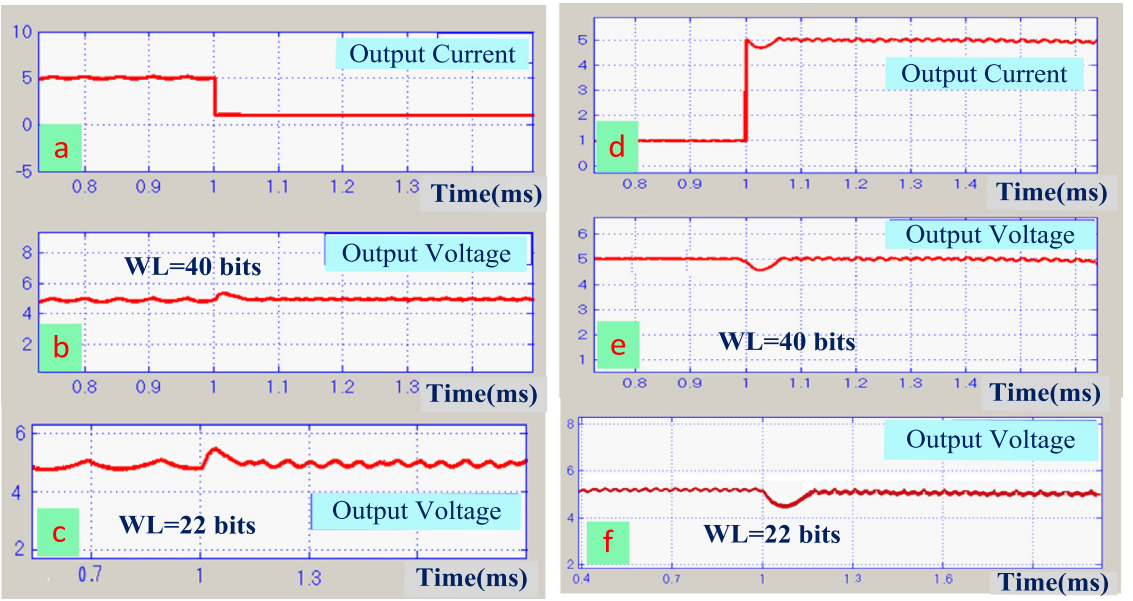

Fig. 10. Performance of the DTFC with proposed processor. (a, b, c) negative load step. (d, e, f) positive load step.

the output voltage. In Fig. 10e word-length is 40 bits, settling time is 55??s and overshoot is 0.4 v. Here integer length and fraction length are 17 bits and 22 bits respectively. In Fig. 10f word-length is 22 bits, settling time is 150??s and overshoot is 0.6 v. Here integer length and fraction length are 4 bits and 17 bits respectively. According to these results, it can be concluded that with decreasing in word-length, the precision of output results has reduced.

This work and results of work in [20] are compared together. In this work the minimum value for overshoot/undershoot is 0.25 v, but in [20] this value is 0.6 v. So, the overshoot/undershoot voltage is reduced by 58.3%. The minimum value for settling time is 30 ??s, but in [20] this time is 40 ??s. Therefor the recovery time is reduced by 25% for a positive/negative load step change. ΔIo/Io and ΔVo/Vo of this work are 80% and 4% respectively but in [20] ΔIo/Io is 50% and ΔVo/Vo is 5%. These comparisons show the precision of the proposed processor and its performance.

5.3. AC to DC converter

In this section the operation of proposed processor in AC to DC converter (active front end rectifier) which is depicted in Fig. 3c is examined. Input currents (i_u,i_v,i_w), input voltages (v_u,v_v,v_w) and DC- link voltage (v_{dc}) are inputs and optimum switching states (s_u,s_v,s_w) are outputs. The objective parameters are transient time, undershoot in output voltage, THD and power factor in AC side. Word-lengths are selected between 15 bits and 32 bits. In this circuit the amplitude of three-phase input voltage (V_{smax}) is 30 v, sampling frequency (f_s) is 25 kHz, C is 1500??f, L is 15 mH, r is 0.4 Ω and V_o is 55 v.

In Fig. 11a results for WL = 32 bits and load changing from 30 Ω to 20 Ω are represented. Integer length is 12 bits and fraction length is 19 bits. Here THD for each phase is 3.22%, power factor = 1, undershoot = 3 v and transient time = 0.05 s. Output results for load varying from 30 Ω to 15 Ω and WL = 32 bits are represented in Fig. 11b. Here undershoot is 4.1 v, transient time is 0.08 s, THD of input current is 3.39%, power factor is equal to 1, integer length is 12 bits and fraction length is 19 bits. In Fig. 11c results for WL = 15bits, integer length = 5bits, fraction length = 9bits and load changing from 30 Ω to 20 Ω are depicted. In this figure undershoot is 6.5 v and transient time is 0.08 s. Here THD for each of input phase currents is 10.15%. The angle between the input voltage and current is zero. In Fig. 11d results for load varying from 30 Ω to 15 Ω and WL = 15 bits are shown. Input currents have same THDs, and their values are 10.2%. This figure reveals the unity power factor. The undershoot is 8 v and transient time is 0.1 s. Integer length and fraction length are 5 bits, 9 bits respectively. According to these results, in smaller WL's the THD, undershoot and recovery time are bigger, so a trade-off exists between these parameters.

In Fig. 12 experimental setup of proposed architecture in DC–DC converter and output results for various conditions are depicted. This figure shows a good matching between experimental and simulation results.

6. Conclusion

An application specific soft-core processor for control switching power converters is designed and implemented. The main features of this processor are being low-cost, flexible, high precision and easy to use. The architecture of this processor has minimum functional units to compute complex control algorithms such as predictive control. Architecture is flexible

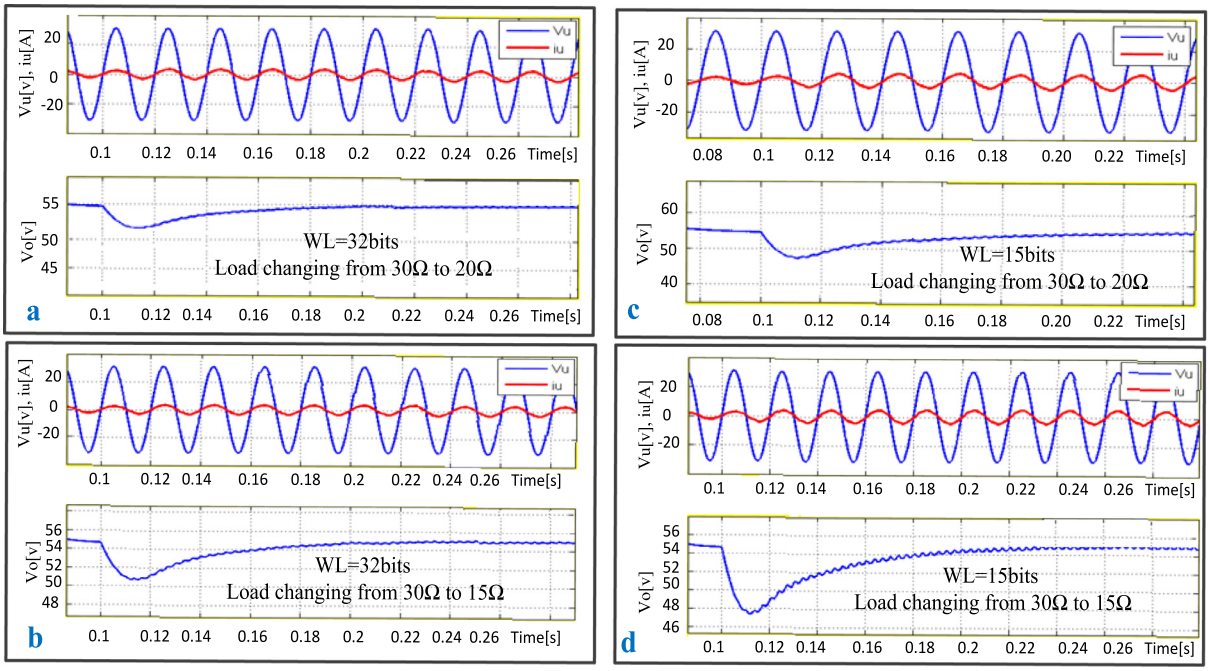

Fig. 11. Operation of AC to DC converter with proposed processor.

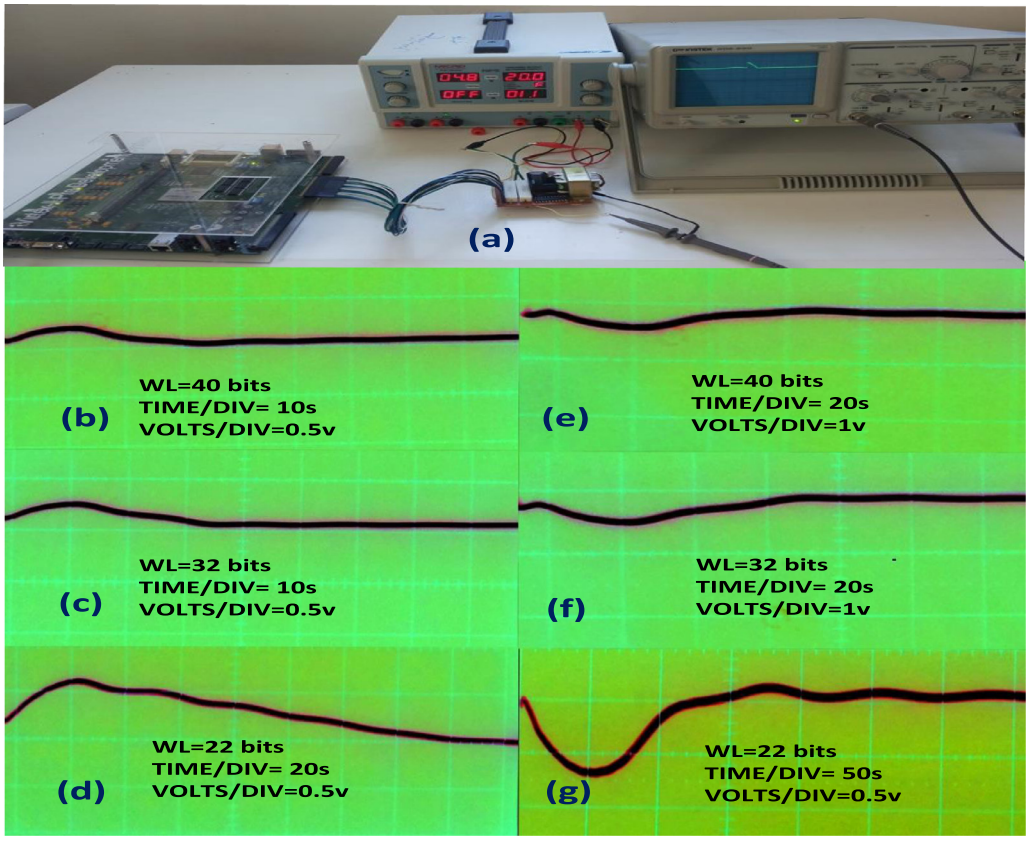

Fig. 12. *Experimental setup*. (**a**) Proposed architecture with DC–DC converter. (**b, c, d**) negative load step change. (**e, f, g**) positive load step change.

in terms of word-length of the functional units. The proposed processor is implemented on FPGA platform and examined in three types of converters such as DC–AC, DC–DC and AC–DC converters. In DC–AC converter word-lengths are between 32 bits and 7 bits. Here by using THD and DC component, the precision of output results is verified. Output results show good accuracy of designed system for this converter. In a DC–DC converter the proposed processor has tested. The main control objective is to minimize settling time and overshoot/undershoot in the output voltage. In this circuit if current step change is greater than 3 A then deviation in output voltage will be seen, which shows the accuracy of proposed architecture. Word-lengths are considered between 40 bits and 22 bits. In this work the minimum and maximum values for overshoot/undershoot is 0.25 v and 0.6 v, these values show the precision of the proposed processor and its performance. The operation of proposed processor in AC–DC converter has examined. Here voltages overshoot/undershoot, Transition Time, THD and power factor of input currents are considered as accuracy cost measures. To evaluate performance of the processor negative load current steps are considered. In these states, load resistance changes from 30 Ω to 20 Ω and 15 Ω. Other features of this processor are reusability for modified switching circuits and generality which results to easy use in any type of switching converters.

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