Modular Parallel Multi-Inverter System for High-Power Inductive Power Transfer

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Abstract—In order to provide high and extendable power levels for inductive power transfer (IPT) system, a parallel multi-inverter system based on modular inverter is presented. Various power requirements can be implemented via adjustment of the number of paralleled inverters, which provide a high modularity. A master-slave scheme is employed for the switching-driver signals of parallel inverters, where one acts as a leader while others as followers. Despite of the master-slave scheme, the proposed circuit topology has natural robustness because of the equality in terms of the hardware configuration of each modular inverter. For proper parameters, the output phase (current lagging corresponding voltage) of an inverter is lower than the average of output phase of all inverters, when its output voltage lags behind others, and vice versa. Based on this approach, PI controllers are designed to implement phase synchronization for output voltages of all inverters. An IPT prototype supplied by the proposed parallel multi-inverter with 3 inverters was designed, built and tested. Experiments shown that the proposed parallel multi-inverter system has not only good circulating current suppression capacity, but also excellent performance of phase synchronization. The maximum DC-DC efficiency was 94% at a 35.1 kW receiving power. This paper is accompanied by a Matlab/Simulink file demonstrating phase synchronization control.

Index Terms—Inductive power transfer, modular inverter, parallel-connected inverters, circulating current suppression, phase synchronization.

I. INTRODUCTION

To achieve high power levels while maintaining a high efficiency is a key requirement for many IPT applications, such as fast charging for high speed trains and for electrical vehicles [1]-[6]. Commonly, high power is shared by multiple inverters or invert-legs instead of a single inverter. Multilevel inverters [7], [8], input-series output-parallel (ISOP) inverters [9]-[11], and parallel multi-inverter system [12]-[21] are three typical topologies integrating the power from various inverters. The main issue of multilevel inverters for IPT is voltage-balance [7], [8]. The topology of multilevel inverters has an advantage of voltage stress reduction for semiconductor devices. However, it is hard maintain all inverters in phase at a high-switching frequency for IPT applications, which leads to a possible high voltage un-balance and therefore possible malfunction. Similarly, ISOP topology shares the input DC voltage equally among all inverters, which requires a high input DC voltage to provide high output power, and it is not reported for IPT applications [9]-[11]. With regard to parallel multi-inverter system, the main issue is current-balance [12]-[21]. The parallel multi-inverter topology shares the total current among various inverters while the current un-balance is suppressed by properly designed circulating-suppression controllers [12]-[20] or circuit topologies [21]. For the application of grid-connected inverters or un-interruptible power supply, current-balance controller is relatively easy to implemented because of the low operating frequency (i.e., 50 Hz) and resulting sampling speed requirement [12]-[18]. The droop control is a common algorithm for these 50 Hz applications. However, the current-balance controller is a bit difficult to implement for IPT applications, considering the influence of the high operating frequency on the sampling and the driver signal propagation delay. The literature [19] shows a design of a 3 kW experimental IPT using a parallel two-inverter topology, where a controller based on active and reactive currents decomposition is designed to minimize the circulating current among inverters. The literature [20] presents a parallel topology to integrate power from multiple inverters via transformers. The power sharing is obtained with a synchronous clamp-mode h-bridge control method. Because of the use of high-frequency transformers, the efficiency is dropped down. In practice, its reported efficiency for the power supply is 94% and 80.5% for the whole IPT system considering the loss in the wireless links, respectively. Being subject to the speed of sampling and controller execution, the operating frequencies of [19] and [20] are both 20 kHz instead of 85 kHz.
band recommended by the standard of SAE TIR J2954.

The literature [21] proposes an inverter consisting of 6 switching-legs that operates at the band of 85 kHz without any current-balance controller. The output currents from these switching-legs are integrated via 6 coupled inductors. The coupled inductor plays an important role to suppress circulating currents among switching-legs. However, the fixed number of inverter-legs lack of the flexibility, considering various power requirements for different application cases.

Alternatively, this paper presents a novel power-integrating topology with parallel multi-inverters whose output power can be regulated through adjusting the number of paralleled inverters. Fig. 1(a) shows the schematic of the proposed system with \( n \) inverters, where coupling ICTs (ICTs, or coupling inductors) are employed to suppress possible outer-modular circulating currents among inverters. A common DC source \( V_{DC} \) is employed to feed all inverters. The output voltage from the \( i \)-th inverter is \( v_{oi} \), where \( 1 \leq i \leq n \). The voltage \( v_{oi} \) is the joint output voltage of the multi-inverter system. In terms of these voltages, the high-order harmonics and the DC components are not considered because only fundamental component can pass through the LC resonant circuit. Fig. 1(b) depicts the equivalent circuit of Fig. 1(a), where each ICT (ICT, for example) is composed of a primary inductor (\( L_{IP} \), for example), a secondary inductor (\( L_{IS} \), for example), a leakage inductor (\( L_{leak} \) for both sides), and a parasitic resistance \( r_{ICT} \). The branch impedance \( Z_b \) represents the total equivalent series resistance and reactance as

\[
Z_b = 2j\omega L_{leak} + 2r_{ICT}.
\]

To provide higher output current, each modular inverter consists of 4 half-bridge switching-legs, which are connected in parallel with 4 ICTs as shown in Fig. 1(c) [21]. The 4 switching-legs share a common DC voltage source \( V_{DC} \). \( v_{o1} \) through \( v_{o4} \) are the fundamental components of voltages generated by these 4 switching-legs, respectively. The ICTs are employed to suppress both the inner-modular circulating currents among legs of an inverter module and the outer-modular circulating currents among inverters [21]. Moreover, various power requirements can be implemented via adjusting the number of paralleled inverters, which provides a high modularity and extendibility.

Phase synchronization is the key issue resulting from parallel operation of multi-inverters, although it is not much difficult for grid-connected inverters due to the low operating frequency and the existence of phase reference from the grid. A high phase asynchrony leads to large circulating currents and power losses. For multi-switching-legs in the same inverter, driver delay is relatively small and ignored in this paper. Beyond the inverter topology and circulating current suppression method proposed in literature [21] with constant number of switching-legs, the main target of the paper is to provide a master-slave control strategy to implement phase synchronization for parallel multi-inverters employed by high power IPT. Although a master-slave scheme is employed for the phase synchronization control, the proposed circuit topology has natural robustness because of the equality in terms of the hardware configuration of each modular inverter. That's to say, all inverter have the same hardware configuration. A distinguish address (namely, 0 through 255) is assigned to different modular inverter. At the start-up stage, all inverters share their addresses via the CAN bus while the inverter with the smallest address behaves as the master one. When some a slave inverter is broken down (for example, its CAN communication is lost), its status can be detected by the main unit and removed from the parallel system. The removing action involves some re-arrangement of the ICTs which is not detailed because of the limit length of article. When the master inverter is broken down (for example, its CAN communication is lost or no pulse is transferred to slave ones ), the failure will be detected by slave inverters easily and the slave inverter with the smallest address will take the place of the original master inverter. In general, the proposed topology has nice robustness attributed to good equality in terms of the hardware configuration of each modular inverter.

For a multi-inverter system, where the slave inverters follow...
the switching signal of the master inverter, the switching frequency is the same for all inverters while the phase asynchrony is mainly attributed to the transmission delay of components in the signal transmission pathway. Hence, one has to detect and compensate the delay to achieve phase synchronization. The direct measurement method, which measures the phase differences between the inverter output currents and the joint current can be employed, where extra measurement components are required. Alternatively, an indirect measurement method, which does not involve the joint current but employs the output phase for zero-voltage-switching (ZVS) detection is proposed. The output phase refers to the angle, the current lags the voltage of an inverter. Considering the measurement of output phase for ZVS is always needed in a practical IPT system, the proposed indirect method is cost saving.

The rest of this paper is organized as follows: Section II analyzes the output phase angles under various numbers of paralleled inverters, while Section III conducts simulations to analyzes the relation between the output phase (the current lagging the corresponding voltage) and phase (the output voltage lagging the reference) of the inverter. Section IV designs a controller to synchronize the phase for various inverters. Finally, a laboratory prototype with 3 modular inverters was designed, built, and tested to supply an IPT system up to 35.1 kW. Experimental results are provided to validate the theoretical analyzes and conclusions are drawn.

II. ANALYSIS OF OUTPUT PHASE ANGLE

Assuming all windings of ICTs for outside of inverters (namely, ICT1 through ICTn) have the same number of turns. Hence, inductances of the primary inductor and the secondary inductor of the ICT are equal to the magnetizing inductance \(L_{M}\). Based on the Kirchhoff law in frequency-domain, the relationship between the output voltages and currents from various inverters presented in Fig. 1(a) can be expressed by

\[
v_{o1}^v - v_{o2}^v = (2j\omega L_{M} + Z_{L})i_{o1} - j\omega M_{ICT} i_{o2} - j\omega M_{ICT} i_{o3}
\]

\[
v_{o2}^v - v_{o3}^v = (2j\omega L_{M} + Z_{L})i_{o2} - j\omega M_{ICT} i_{o3} - j\omega M_{ICT} i_{o4}
\]

\[\ldots\]

\[v_{o1}^v - v_{o4}^v = (2j\omega L_{M} + Z_{L})i_{o4} - j\omega M_{ICT} i_{o5} - j\omega M_{ICT} i_{o6}
\]

\[\quad\ldots\]

\[v_{o}^v = Z_{load}i_{o}^v
\]

\[i_{o} = \sum_{i=1}^{n} i_{oi}
\]

where \(i_{oi}\) through \(i_{on}\) are the output currents from various inverters, \(M_{ICT}\) is the mutual inductance between the two windings of the ICT, namely,

\[M_{ICT} = L_{M}\]

(3)

\(i_{o}\) and \(Z_{load}\) are the total output current and the input impedance, respectively. Substitution (3) into (2), one can yield output current from each inverter easily.

For the system with 2 inverters, the currents from various inverters are

\[i_{o1} = \frac{Z_{load}(v_{o1}^v - v_{o2}^v) + 2j\omega L_{M}(v_{o1}^v + v_{o2}^v) + 2j\omega Z_{L}v_{o1}^v}{4(Z_{load} + j\omega Z_{L})(2j\omega L_{M} + j\omega Z_{L})}.
\]

(4)

\[i_{o2} = \frac{Z_{load}(v_{o2}^v - v_{o3}^v) + 2j\omega L_{M}(v_{o1}^v + v_{o2}^v) + 2j\omega Z_{L}v_{o2}^v}{4(Z_{load} + j\omega Z_{L})(2j\omega L_{M} + j\omega Z_{L})}.
\]

Under the condition that the branch impedance \(Z_{o}\) is much lower than \(Z_{load}\) and can be ignored, (4) is simplified to

\[i_{o1} = \frac{Z_{load}(v_{o1}^v - v_{o2}^v) + 2j\omega L_{M}(v_{o1}^v + v_{o2}^v)}{8j\omega L_{M}Z_{load}}
\]

(5)

\[i_{o2} = \frac{Z_{load}(v_{o2}^v - v_{o3}^v) + 2j\omega L_{M}(v_{o1}^v + v_{o2}^v)}{8j\omega L_{M}Z_{load}}
\]

When all inverters are fed by a common DC voltage source \(V_{DC}\), the output voltages from inverters can be assumed to have the same amplitude \(V_{amp}\). Hence, \(v_{o1}^v\) and \(v_{o2}^v\) can be expressed by

\[v_{o1}^v = V_{amp}e^{\theta_1},
\]

(6)

\[v_{o2}^v = V_{amp}
\]

where \(\theta_1\) is the phase angle that voltage \(v_{o2}\) lags behind \(v_{o1}\). The impedances of inverters are

\[Z_{o1} = \frac{v_{o1}^v}{i_{o1}}
\]

(7)

\[Z_{o2} = \frac{v_{o2}^v}{i_{o2}}
\]

Substitution (5) and (6) into (7) yields the impedances

\[Z_{o1} = \frac{Z_{load}}{8j\omega L_{M}Z_{load}}(1+ e^{-j\theta_1}) + \frac{2j\omega L_{M}Z_{load}}{1+ e^{-j\theta_1}}.
\]

(8)

\[Z_{o2} = \frac{Z_{load}}{8j\omega L_{M}Z_{load}}(1+ e^{j\theta_1}) + \frac{2j\omega L_{M}Z_{load}}{1+ e^{j\theta_1}}.
\]

One defines the output phases for various inverters as

\[\phi_1 = \text{atan2}(\text{imag}(Z_{o1}), \text{real}(Z_{o1})),
\]

(9)

\[\phi_2 = \text{atan2}(\text{imag}(Z_{o2}), \text{real}(Z_{o2}))
\]

where atan2 is the arctangent function with two arguments whose output range is \(-\pi\) to \(\pi\). The functions imag and real are employed to obtain the imaginary part and the real part, respectively.

For a multi-inverter system with 3 inverters, the output currents from inverters can be obtained from (2) as

\[i_{o1} = \frac{Z_{load}(v_{o1}^v - v_{o2}^v - v_{o3}^v) + 2j\omega L_{M}(v_{o1}^v + v_{o2}^v + v_{o3}^v)}{9j\omega L_{M}Z_{load}}
\]

(10)

\[i_{o2} = \frac{Z_{load}(v_{o2}^v - v_{o3}^v - v_{o1}^v) + 2j\omega L_{M}(v_{o1}^v + v_{o2}^v + v_{o3}^v)}{9j\omega L_{M}Z_{load}}
\]

\[i_{o3} = \frac{Z_{load}(v_{o3}^v - v_{o1}^v - v_{o2}^v) + 2j\omega L_{M}(v_{o1}^v + v_{o2}^v + v_{o3}^v)}{9j\omega L_{M}Z_{load}}
\]

To analyze the influence of the output voltage delay on the output phase angle, one assumes that the output voltages of all slave inverters are the same while \(v_{o1}\) (representing the voltage of the master inverter) leads them by a angle \(\theta_4\), namely

\[v_{o1} = V_{amp}e^{\theta_1},
\]

(11)

\[v_{o2-3} = V_{amp}
\]

where \(v_{o2-3}\) represents the voltages \(v_{o2}\) and \(v_{o3}\). Considering the equivalence of all slave inverters in terms of driver signal propagation delay, the assumption that the output voltages of all slave inverters are the same is reasonable. In the following analysis, \(v_{o1}\) refers to the output voltage of the master inverter.
while other voltages (i.e., \(v_{o2}, v_{o3}, v_{o4}\), and so on) refer to those for slave inverters.

As a result, the impedances of inverters are

\[
Z_{o1} = \frac{9 j o L_s Z_{load}}{Z_{load}(2-2e^{-j\phi}) + j o L_s (1+2e^{-j\phi})}.
\]

\[
Z_{o2} = \frac{9 j o L_s Z_{load}}{Z_{load}(1-e^{-j\phi}) + j o L_s (2+e^{-j\phi})}.
\]

With the same assumption used by (11), the impedances for system with 4, 5, and 6 parallel inverters are given in (13) through (15), respectively

\[
Z_{o3} = \frac{16 j o L_s Z_{load}}{Z_{load}(5-5e^{-j\phi}) + j o L_s (1+3e^{-j\phi})}.
\]

\[
Z_{o4} = \frac{16 j o L_s Z_{load}}{Z_{load}(1-e^{-j\phi}) + j o L_s (3+e^{-j\phi})}.
\]

\[
Z_{o5} = \frac{16 j o L_s Z_{load}}{Z_{load}(3-3e^{-j\phi}) + j o L_s (3+e^{-j\phi})}.
\]

\[
Z_{o6} = \frac{25 j o L_s Z_{load}}{Z_{load}(10-10e^{-j\phi}) + j o L_s (1+4e^{-j\phi})}.
\]

\[
Z_{o7} = \frac{25 Z_{load}}{4+e^{j\phi}}.
\]

\[
Z_{o8} = \frac{25 j o L_s Z_{load}}{Z_{load}(5-5e^{-j\phi}) + j o L_s (4+e^{-j\phi})}.
\]

\[
Z_{o9} = \frac{72 j o L_s Z_{load}}{Z_{load}(35-35e^{-j\phi}) + 2 j o L_s (1+5e^{-j\phi})}.
\]

\[
Z_{o10} = \frac{72 j o L_s Z_{load}}{Z_{load}(35-35e^{-j\phi}) + 2 j o L_s (1+5e^{-j\phi})}.
\]

\[
Z_{o11} = \frac{72 j o L_s Z_{load}}{Z_{load}(35-35e^{-j\phi}) + 2 j o L_s (1+5e^{-j\phi})}.
\]

\[
Z_{o12} = \frac{72 j o L_s Z_{load}}{Z_{load}(35-35e^{-j\phi}) + 2 j o L_s (1+5e^{-j\phi})}.
\]

\[
Z_{o13} = \frac{72 j o L_s Z_{load}}{Z_{load}(35-35e^{-j\phi}) + 2 j o L_s (1+5e^{-j\phi})}.
\]

\[
Z_{o14} = \frac{72 j o L_s Z_{load}}{Z_{load}(35-35e^{-j\phi}) + 2 j o L_s (1+5e^{-j\phi})}.
\]

\[
Z_{o15} = \frac{72 j o L_s Z_{load}}{Z_{load}(35-35e^{-j\phi}) + 2 j o L_s (1+5e^{-j\phi})}.
\]

The impedance expressions for more numbers of parallel inverters can also be obtained from (2), but it is somewhat complex and not presented here. As a result, the output phases for various inverters can be obtained with the same method expressed by (9).

III. SIMULATION FOR OUTPUT PHASE ANGLE

To provide a stable supply for the IPT system, all inverters composing the parallel multi-inverter system should operate in phase. A main-slaver scheme is employed for the phase synchronization of parallel multi-inverter system, where one inverter acts as the leader while others follow the leader regarding to the frequency and phase. Although the phase deviations between various output voltages reflect the status of phase synchronization directly, they are hard to measure correctly because of the high operating frequency together with the inevitable inconsistency of propagation delay of measured signals. In contrast, the measurement of the output phase of an inverter is more precise because all signal pathways are in the same PCB board. Hence, the output phase instead of the output voltage phase is sampled for the phase synchronization control. The rest of this section analyzes the relation between the output phases (current lagging voltage of corresponding inverter), the average of them for all inverters, and the output voltage phase of the inverter. The expected conclusion is that the deviation between the output phase of an inverter and the average of all inverters reflects the in-phase status of the inverter output voltage.

Regarding to a practical inverter, the output phase angle defined by its output current lagging voltage is easy to measure and commonly used for ZVS detection [4]. To find the relations between the output phase and the voltage delay angle, simulations are conducted for a typical S-S compensated IPT system shown in Fig. 2,

![Fig. 2. A typical S-S compensated IPT system.](image)

where \(v_o\) represents the joint output voltage from parallel interferers, \(C\) and \(L\) are the resonant capacitors and inductors, \(r_1\) and \(r_2\) are parasitic resistances, \(k\) is the coupling factor between two sides, and \(R_L\) is the equivalent load resistance, respectively. The parameters for the simulations are listed in Table I.

<table>
<thead>
<tr>
<th>symbol</th>
<th>parameter</th>
<th>value</th>
</tr>
</thead>
<tbody>
<tr>
<td>(f)</td>
<td>Operating frequency</td>
<td>85 kHz</td>
</tr>
<tr>
<td>(k)</td>
<td>Coupling coefficient between the sending and receiving coils</td>
<td>0.22</td>
</tr>
<tr>
<td>(L)</td>
<td>Resonant inductance at both the sending side and the receiving side</td>
<td>32.5 (\mu)H</td>
</tr>
<tr>
<td>(C)</td>
<td>Resonant capacitance at both the sending side and the receiving side</td>
<td>113.0 nF</td>
</tr>
<tr>
<td>(r_1)</td>
<td>Parasitic resistance at the sending side</td>
<td>50 m(\Omega)</td>
</tr>
<tr>
<td>(r_2)</td>
<td>Parasitic resistance at the receiving side</td>
<td>50 m(\Omega)</td>
</tr>
<tr>
<td>(R_L)</td>
<td>Load resistance at the receiving side</td>
<td>8.0 (\Omega)</td>
</tr>
</tbody>
</table>

Besides the parameters listed in Table I, the magnetizing inductance \(L_M\) of ICTs has an important impact on the output phase as shown in (8) and (12) through (15). A high \(L_M\) is expected in terms of good circulating current suppression capacity. However, the higher parasitic resistance resulting from a higher \(L_M\) degenerates the overall efficiency.

Hence, a relatively small \(L_M\), which is half of the resonant inductance \(L\), is employed for the first 5 simulations, then 3 simulations with higher \(L_M\) are conducted for expected result. Fig. 3 depicts the relations between output phases (namely, \(\phi_1, \phi_2, \phi_3, \ldots\)) versus the output voltage delay angle \(\theta_t\) that the slave inverters lag behind the master inverter. The average \(\phi_{avg}\) of the output phases for all inverters is also shown for comparison.

Ignoring Fig. 3(d), (e), and (g), some important conclusions can be drawn from Fig. 3:

1) When the output voltages of slave inverters are in phase with that of the master inverter (i.e., \(\theta_t = 0\)), their output phases (i.e., \(\phi_2\) through \(\phi_n\)) are equal to the average of all output phases (i.e., \(\phi_{avg}\)).
the master inverter (i.e., $\phi_1$ through $\phi_n$) are higher than the average of all output phases (i.e., $\phi_{avg}$), and vice versa. This character can be explained as follows: All of the inverters output currents tend to be almost in-phase because of the existence of coupling inductors. As a result, the inverter, whose output voltage leads the others, has a higher phase difference between its voltage and the "in-phase" current, namely, a higher output phase.

3) The output phase of the master inverter (i.e., $\phi_1$) strictly monotonically increases with the voltage delay phase (i.e., $\theta_1$). Although there is a different rate of increase, this conclusion is always correct under various numbers (from 2 through 6) of parallel inverters.

4) The average of output phase $\phi_{avg}$ is almost constant under various voltage delay phase $\theta_1$ and numbers of parallel inverters.

However, some plots in Fig. 3(d), (e), and (g) are not rigidly consistent with above conclusions. By comparing Fig. 3(d) with (f), and (g) with (h), however, one can see that the inconsistency can be eliminated with employing a modestly higher magnetizing inductance $L_M$ of the ICTs.

In short, under proper parameters, the deviation between the output phase of an inverter and the average of all inverters reflects the in-phase status of the inverter output voltage. To achieve synchronization, in general, one can regulate its output voltage phase based on the error between its output phase and the average of all output phases. Based on above analysis, a control scheme is designed in the following sub-section.

IV. PHASE SYNCHRONIZATION CONTROL

A. Controller Scheme for Phase Synchronization

Fig. 4 depicts the control scheme of the phase synchronization for the parallel multi-inverter system where a master-slave structure is employed. Although more inverters can be added in, only two slave units are employed in Fig. 4 for simplification. The main control unit generates a square wave signal, which drivers the inverter #1 directly (in practice, isolated driver components are included but ignored here for simplification). The average value of output phases is calculated in the main unit. The square wave signal from the main control unit is also transmitted to other slave control units via physical signal wires together with corresponding transceivers for each unit board. The phases $\Delta\phi_2$ and $\Delta\phi_3$ represent the time delays due to the introduction of the transceivers and signal propagation pathways. $\phi_1$ is the output phase determined by the current lagging the voltage of the inverter in the main unit, and similarly for $\phi_2$ and $\phi_3$ in the slave units, respectively. $\phi_{avg}$ is the average value of output phases for all inverters. $\text{Err}_{avg}^{1}$ and $\text{Err}_{avg}^{2}$ are the errors of the output phases and the average value, respectively. $\phi_{c2}$ and $\phi_{c3}$ are the outputs of PI controllers, respectively. $\Delta\phi_{c2}$ and $\Delta\phi_{c3}$ are the angles which compensate the delays of $\Delta\phi_2$ and $\Delta\phi_3$, respectively. When a minus output from the PI controller happens, an angle of $2\pi$ is added to it to obtain a positive compensated phase always.

![Fig. 4. Master-slave control scheme of the phase synchronization for the parallel multi-inverter system](image)

Despite of different software configuration regarding to different unit, their hardware configuration is the same. If one more slave unit is added, for example, only one modification is required in the average calculation whose coefficient is changed from $1/3$ to $1/4$ except the hardware of the added...
unit. This character provides a good extendibility for the proposed parallel multi-inverter system.

B. Controller Simulation

With regard to #1 PI controller operating in the first slave unit, the position control algorithm can be expressed as

$$\phi_{C1}(k + 1) = K_p \times Err_{2,\text{avg}}(k) + K_i \times \sum (Err_{2,\text{avg}}(k))$$  \(22\)

where \(K_p\) and \(K_i\) are the proportion coefficient and the integral coefficient, respectively, and \(\sum (Err_{2,\text{avg}}(k))\) represents the accumulation of deviations \(Err_{2,\text{avg}}\) till the \(k\) calculation, respectively. The same control algorithm is applied to the other slave inverters.

Fig. 5 depicts the SIMULINK simulation circuit model and the regulation process with PI controllers at the start-up stage. The discrete sampling time of the SIMULINK model is 1e-6 s. For the PI controller, a shorter sampling time commonly results to a faster response. However, the communication speed of the CAN bus is limited. As a result, the sampling rate of the PI controller is 1 kHz. In Fig. 5(a), inverter is replaced by a controlled AC voltage source whose phase is regulated by a variable time delay module. The initial driver phase delay is depicted by a transport delay module. Output phase is measured by Fourier module which is not shown for simplification. ICTs depicted by a transport delay module. Output phase is measured by SUM && MOD and variable time delay are time based, a grain on degree unit while other modules, including transport delay, parasitic resistances, load resistance and mutual inductance are the same with listed in Tab. I. After analyzing and adjusting the PI parameters to obtain a curve with better dynamic performance, parameters \(K_p = 0.25\) and \(K_i = 0.06\) were employed for both slave inverters. Fig. 5(b) and (c) depicts the regulation process regarding to the output phases and their average value at the startup stage with the given initial delay of 10° (namely, transport delay of 1/85000/36 s) for both slave inverters. One can see that all inverters arrive at a phase synchronization within about 0.3 s. Note that \(\phi_2\) and \(\phi_3\) depicted in Fig. 5(b) are overlapped, and similarly for \(\phi_{C2}\) and \(\phi_{C3}\) in (c).

V. Prototype and Experimental Verification

A. Prototype of Parallel Multi-inverter System

Fig. 6 shows the parallel multi-inverter prototype, where the modular inverter is depicted in (a). The modular inverter is mainly composed of three modules, namely, the control card, the driver card, and the power stage. Additionally, heat sinks are employed for the inverter switches. Two driver cards, each consists of four isolated drivers, are employed to connect the control card and the power stage. Two MCUs, namely, an FPGA of XC6SLX9-3TQG144I and an ARM of STM32F407VG, and other auxiliary components constitute the control card. The half-bridge switching legs of the inverter...
are constructed with C2M0025120D SiC MOSFETs whose nominal parameters are 1200 V and 90 A. For the inner-module circulating current suppression, four ICTs for each modular inverter are manufactured with toroidal core of T300-2 and Litz-wire of 500×0.1 mm. The self-inductance about 10 µH and the leakage inductance about 1.6 µH were obtained with 30 winding turns at each side of the ICTs.

The square wave driver signal for each C2M0025120D is generated by an FPGA. The FPGA operates at a frequency of 199.5 MHz. Hence, the driver signal switches for each 1173 FPGA CLKs to generate a system operating frequency of 85 kHz. The FPGA samples the output phase between the current and the voltage outputted from the same switching leg with the help of zero-crossing module, then sends the angle value to corresponding ARM via SPI communication. For the prototype, all phases including the switching periods, the output phases and the compensated phases are measured or represented by CLKs of FPGA whose counting frequency is 199.5 MHz. Namely, a period of 2347 FPGA CLKs are equal to 360° at an operating frequency of 85 kHz.

The parallel multi-inverter system consisting of three modular inverters is shown in Fig. 6(b), where one plays the leader and the others act as followers. If a higher power level is required, more modular inverters can be added while things left to do are the selection of proper coupling inductors with corresponding number of ICTs and modifying the coefficient for the output phase average value calculated according to the number of the paralleled inverters. For the outer-module circulating current suppression, 3 higher power ICTs were manufactured. Each of them is with 2 toroidal cores T300-2 and Litz-wire of 1000×0.1 mm. The self-inductance about 14 µH and the leakage inductance about 2 µH were obtained with 24 winding turns at each side of the ICTs.

The square wave driver signal generated by the FPGA in the main control card is transmitted to the slave cards via transceivers, besides the driver of the inverter of the main unit. The MAX485 was employed as the transceivers because of its good anti interference capability resulting from its differential driver mode. Besides that, the main control card receives the phase angles from two slave cards, then calculates the average value of these three and sends back to the slave control cards via CAN communication. The PI controller operates in each ARM of the slave control card, and outputs corresponding compensated CLks to the FPGA, which generates square wave driver signal according to the receiving square wave driver signal and the compensated CLks. For simplification, only one signal for the upper switch driver is sent to the slave inverter. Hence, the FPGA of slave inverter detects the switching frequency and the duty via the change of the received pulse signal and generates driver signal for the lower switch.

### B. Prototype of IPT

An S-S compensated IPT supplied by the proposed parallel multi-inverter system with three modular inverters was constructed and shown in Fig. 7. Three adjustable DC voltage source modules REG75030 were connected in parallel to obtain a high power common DC bus feeding all inverters. The nominal parameters of REG75030 are 750 V and 20 A. Regarding dimensions, both coils at the sending and receiving sides were the same: a rectangle 89 cm by 69 cm at the outer sides and 84 cm by 64 cm at the inner sides. Each planar solenoid coil contains 4 turns of Litz-wire, which consists of 5000 isolated strands with an outer diameter of 10 mm. The diameter of the strand is 0.1 mm. The gap of two coils is 20 cm.
C. Experiment for Circulating Current Suppression under Phase Out-sync

<table>
<thead>
<tr>
<th>symbol</th>
<th>value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f$</td>
<td>Operating frequency 85 kHz</td>
</tr>
<tr>
<td>$f_{FPGA}$</td>
<td>FPGA clock frequency 199.5 MHz</td>
</tr>
<tr>
<td>$d$</td>
<td>Gap between two coils 20 cm</td>
</tr>
<tr>
<td>$M$</td>
<td>Coupling inductance of two coils 7.25 $\mu$H</td>
</tr>
<tr>
<td>$L_R$</td>
<td>Resonant inductance at the sending side 32.3 $\mu$H</td>
</tr>
<tr>
<td>$C_R$</td>
<td>Resonant capacitance at the sending side 113.1 nF</td>
</tr>
<tr>
<td>$r_{CS}$</td>
<td>Parasitic resistance of the resonant capacitor at the sending side 2 $\mu$O</td>
</tr>
<tr>
<td>$r_{LS}$</td>
<td>Parasitic resistance of the resonant inductor at the sending side 25 $\mu$O</td>
</tr>
<tr>
<td>$L_S$</td>
<td>Resonant inductance at the receiving side 31.6 $\mu$H</td>
</tr>
<tr>
<td>$C_S$</td>
<td>Resonant capacitance at the receiving side 112.4 nF</td>
</tr>
<tr>
<td>$r_{CR}$</td>
<td>Parasitic resistance of the resonant capacitor at the receiving side 2 $\mu$O</td>
</tr>
<tr>
<td>$r_{LR}$</td>
<td>Parasitic resistance of the resonant inductor at the receiving side 22 $\mu$O</td>
</tr>
<tr>
<td>$R_{load}$</td>
<td>Load resistance of the rectifier at the receiving side 10.5 $\Omega$</td>
</tr>
<tr>
<td>$L_{M,I}$</td>
<td>Magnetizing inductances of ICTs for inner-circulating current suppression 9.7 $\mu$H–10.2 $\mu$H</td>
</tr>
<tr>
<td>$L_{Leak,I}$</td>
<td>Leakage inductances of ICTs for inner-circulating current suppression 1.55 $\mu$H–1.62 $\mu$H</td>
</tr>
<tr>
<td>$r_{ICT,I}$</td>
<td>Parasitic resistance at each winding of ICTs for inner-circulating current suppression 29.4 $\mu$O–30.9 $\mu$O</td>
</tr>
<tr>
<td>$L_{M,O}$</td>
<td>Magnetizing inductances at each winding of ICTs for inner-circulating current suppression 13.7 $\mu$H–13.9 $\mu$H</td>
</tr>
<tr>
<td>$L_{Leak,O}$</td>
<td>Leakage inductances at each winding of ICTs for inner-circulating current suppression 1.82 $\mu$H–2.07 $\mu$H</td>
</tr>
<tr>
<td>$r_{ICT,O}$</td>
<td>Parasitic resistance at each winding of ICTs for inner-circulating current suppression 18.7 $\mu$O–20.6 $\mu$O</td>
</tr>
<tr>
<td>$r_{DS}$</td>
<td>Parasitic resistance of the MOSFET 25 $\mu$O</td>
</tr>
<tr>
<td>$Q_i$</td>
<td>Charge at the MOSFET gate 161 nC</td>
</tr>
<tr>
<td>$t_r$</td>
<td>Raising time of the MOSFET 32 ns</td>
</tr>
<tr>
<td>$t_i$</td>
<td>Falling time of the MOSFET 28 ns</td>
</tr>
<tr>
<td>$V_F$</td>
<td>Forward voltage drop of the rectifier at the receiving side 1.87 $V$</td>
</tr>
<tr>
<td>$r_{CF}$</td>
<td>Parasitic resistance of the rectifier filter capacitor 8 $\mu$O</td>
</tr>
</tbody>
</table>

Considering a high AC current and resulting high reactive voltage, 226 film capacitors, 1 nF each, were connected in parallel, then in series with other 226 ones, 1 nF each, to form a 113 nF compensated capacitance at both sides. At the receiving side, two DSE12X101-12A rectifiers were used to construct a full-bridge rectifier. The main parameters are listed in Table II, where resistances, inductances, and capacitances were measured with an Agilent E4980A LCR meter at 85 kHz.

Because of the component propagation delays in the transmission pathway of the driver signal, the driver signals and the output voltages of the slave inverters will lag behind those of the master inverter at the initial status. In order to check the suppressing capability for circulating current due to phase out-sync, the output currents from the master inverter and one slave inverter are measured under initial phase out-sync, where the phase delay compensations are not employed. Under a common input DC voltage 100 V for inverters, the output voltages and currents are captured by a 4-channel oscilloscope, Tektronix DPO 2004B and shown in Fig. 8(a), where channel 3 and 2 show for the output voltage and current of the master inverter, while channel 4 and 1 show those of the slave inverter, respectively. The waveforms for both slave inverters were almost the same; therefore those for another slave one are not presented. From the voltage waveforms of Fig. 8(a), one can observe that the voltage phase difference is about 12°, which is mainly attributed to the MAX485 transceivers in the driver signal pathway. The current difference between two inverters were below 0.5 A, which shows that the coupling inductors has good suppression capacity in terms of the outer-circulating current. Moreover, an experiment with a deliberate additional 5° (namely, 33 FPGA CLks under 85 kHz operating frequency) delay besides the initial delay is applied to this slave inverter, was conducted to examine the currents. Fig. 8(b) shows that the current difference increases with the phase delay, but still remains a small one.

Additionally, output currents from various inverters show small phase difference for both cases of the initial driver signal delay and the deliberate 5° delay. As a result, the phase difference of output phases (namely, the current lags behind the corresponding voltage) is almost determined by the difference of the voltages while that of currents plays an ignorable role. Conversely, the relative magnitudes of output phases reflect their magnitudes of phase delays, which agrees with the conclusion of simulation in Section III.

![Fig. 8. Output voltages and currents without delay compensation of driver signal. (a) is for the initial phase out-sync and (b) is for an additional driver delay of 5° besides the initial one.](0885-8993 (c) 2018 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.)
105 V, both PI controllers work together to regulate the phases of output voltages as soon as detecting a DC voltage above 103 V.

The PI parameters of the prototype were the same as mentioned in Section IV.B, namely, $K_p = 0.25$, $K_i = 0.06$ and a sampling rate of 1 kHz. The output phases, their average and compensated phases are sampled and stored by corresponding ARMIs and uploaded to a private computer with RS232 communication if required. For the initial case, the measured output phases of the master inverter and two slave ones were 250, 188 and 194 CLKs, respectively. The measured delay compensations of two slave inverters after synchronization were $\Delta \phi_2 = -75$ and $\Delta \phi_3 = -74$ CLKs, respectively. As a result, the practical compensations executed by the FPGA were $\Delta \phi_2 = 2272$ and $\Delta \phi_3 = 2273$ considering $2\pi$ (namely, 2347 CLKs at 85 kHz) is added for minus compensations, respectively. In fact, the compensated CLKS of -75 can also be expressed by -11.5° considering the period of 2347 CLKs at 85 kHz, which had good agreement with the measured delay of 12° shown in Fig. 8(a). This verifies that the PI controller can trace the phase delay correctly.

For the case of a deliberate 5° (namely, 33 CLKs) delay besides the initial one, the measured output phases of the master inverter and two slave ones were 246, 165, and 203 CLKs, respectively. The measured delay compensations of two slave inverters after synchronization were $\phi_2 = -108$ and $\phi_3 = -74$ CLKs, respectively. As a result, the practical compensations executed by the FPGA were $\Delta \phi_2 = 2239$ and $\Delta \phi_3 = 2273$, respectively. Considering the delay of 16.5° (a initial delay of 11.5° plus a deliberate 5°) equals to 108 CLKS at 85 kHz, one can see that PI controller can compensate the delay correctly.

Fig. 9 illustrates the regulation process of the phase synchronization for the startup stage while DC voltages is raised from 100 V to 105 V, where (a) is for the case of initial delay, (b) for the deliberate 5° delay besides the initial one and (c) for the waveform after phase synchronization. One can see that the phase regulations were finished within a short time (i.e., less than 0.3 s). Fig. 9(a) and (b) shows good agreements with simulated results by Simulink shown in Fig. 5(a) and (b), respectively.

After the phase synchronization, the input voltage for all inverters are regulated to 700 V, which leads to an input DC current of 53.3 A. The output voltages and currents of the master inverter and one slave inverter were captured and shown in Fig. 10. One can see that these plots show good agreement between both the amplitudes and the phases of voltages and currents. The measured voltage at the 10.5 Ω resistance load is 607 V, which means a received power of 35.1 kW. The measured DC-DC efficiency was 94% which is defined by the power consumed in the load resistance divided by that outputted from the DC voltage modules.

Practically, the loss at the primary side can be evaluated based on the measured current, impedance angles and parameters listed in Tab. II [21] by

$$P_{\text{load}} = P_{\text{loss}} + P_{\text{DS}} + P_{\text{ICT,1}} + P_{\text{ICT,0}} + P_{\text{LP}} + P_{\text{CP}}$$

where $P_{\text{loss}}$, and $P_{\text{DS}}$ are losses in all MOSFETs due to turn-off and on-state resistance, $P_{\text{ICT,1}}$, and $P_{\text{ICT,0}}$ are losses in inner ICTs and outer ICTs due to parasitic resistance, $P_{\text{LP}}$ and $P_{\text{CP}}$ are losses in the resonant inductor and the capacitor at the primary side, respectively. These losses can be calculated by [21]
are the losses in the rectifier, the 0.04
0.04
0.08
0.02
0.1
0.06
This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2019.2891064, IEEE
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capacitor which can be calculated respectively by
filter capacitor , the resonant inductor and the resonant
in Tab. II (assuming
respectively.  As a result, losses in various components can be
RMS through the 10.5
amplitude at the secondary side is
lags behind the voltage of the inverter is
difference between the measured 94% overall efficiency.

P_{\text{eff}} = \frac{\omega(t_e/3 + t_i/2)V_f i_d \sin \theta}{2\pi} 

P_{\text{rDS}} = 6(i_d/12)^2 r_{\text{DS}} 

P_{\text{rICT,1}} = 12(i_d/12)^2 r_{\text{ICT,1}} 

P_{\text{rICT,O}} = 3(i_d/3)^2 r_{\text{ICT,O}} 

P_{\text{LP}} = i_d^2 r_{\text{LP}}/2 

P_{\text{CP}} = i_d^2 r_{\text{CP}}/2 

In terms of the receiving side, its total loss is
P_{\text{lossS}} = P_{\text{VF}} + P_{\text{CF}} + P_{\text{rLS}} + P_{\text{rCS}} ,

where $P_{\text{VF}}$, $P_{\text{CF}}$, $P_{\text{rLS}}$ and $P_{\text{rCS}}$ are the losses in the rectifier, the filter capacitor, the resonant inductor and the resonant capacitor which can be calculated respectively by

$P_{\text{VF}} = \sqrt{2} V_f i_s$

$P_{\text{CF}} = \frac{i_d^2 r_{\text{CF}}}{2} \left( \frac{\pi}{8} - 1 \right)$

$P_{\text{rLS}} = \frac{i_d^2 r_{\text{LS}}}{2}$

$P_{\text{rCS}} = \frac{i_d^2 r_{\text{CS}}}{2}$

TABLE III

<table>
<thead>
<tr>
<th>symbol</th>
<th>Losses due to</th>
<th>value</th>
<th>Accounting for</th>
</tr>
</thead>
<tbody>
<tr>
<td>$P_{\text{rLP}}$</td>
<td>loss in the resonant inductor at the primary side</td>
<td>437.66 W</td>
<td>31.64%</td>
</tr>
<tr>
<td>$P_{\text{rICT,O}}$</td>
<td>losses in all outer ICTs due to parasitic resistance</td>
<td>259.95 W</td>
<td>18.79%</td>
</tr>
<tr>
<td>$P_{\text{VF}}$</td>
<td>loss in the rectifier due to forward voltage drop</td>
<td>239.19 w</td>
<td>17.29%</td>
</tr>
<tr>
<td>$P_{\text{rICT,1}}$</td>
<td>losses in all inner ICTs due to parasitic resistance</td>
<td>107.51 W</td>
<td>7.77%</td>
</tr>
<tr>
<td>$P_{\text{rDS}}$</td>
<td>loss in the resonant inductor at the secondary side</td>
<td>102.25 W</td>
<td>7.39%</td>
</tr>
<tr>
<td>$P_{\text{rICT,2}}$</td>
<td>losses in all inner ICTs due to parasitic resistance</td>
<td>99.47 W</td>
<td>7.19%</td>
</tr>
<tr>
<td>$P_{\text{rDS}}$</td>
<td>loss in all MOSFETs due to on-state resistance</td>
<td>41.45 W</td>
<td>3.00%</td>
</tr>
<tr>
<td>$P_{\text{CF}}$</td>
<td>Loss in the resonant capacitor at the sending side</td>
<td>48.01 W</td>
<td>3.47%</td>
</tr>
<tr>
<td>$P_{\text{CP}}$</td>
<td>loss in the filter capacitor at the primary side</td>
<td>39.78 W</td>
<td>2.88%</td>
</tr>
<tr>
<td>$P_{\text{rCS}}$</td>
<td>loss in the resonant capacitor at the secondary side</td>
<td>8.18 W</td>
<td>0.59%</td>
</tr>
</tbody>
</table>

The measured overall output current amplitude at the primary side is $i_0 = 199.5$ A, impedance angle that the current lags behind the voltage of the inverter is $\theta = 35.8^\circ$, the current amplitude at the secondary side is $i_S = 91.2$ A and the current RMS through the 10.5 $\Omega$ load resistance is $I_{\text{load}} = 57.8$ A, respectively. As a result, losses in various components can be obtained based on these measured values and parameters listed in Tab. II (assuming $r_{\text{CF}} = 30$ m$\Omega$ and $r_{\text{ICT,1}} = 19.6$ m$\Omega$, respectively). The loss breakdown calculated by (23) through (26) is listed in Tab.III. The total loss is 1.39 kW which accounts for about 4% of the overall power. There is about 2% difference between the measured 94% overall efficiency.

Considering the ignored core loss in ICT windings and measuring errors of the currents, voltages and impedance angles, the evaluated loss breakdown is reasonable. Besides, one can see that loss in resonant inductor at the primary side accounts for the highest percentage, which means that a proper designed inductor with a lower parasitic resistance is the future direction to achieve higher efficiency.

E. Experiment for Phase Synchronization with Variable Operating Frequency

Assuming the time delay of the signal pathway is constant, the delay expressed by phase angle varies with the operating frequency. Additionally, the frequency variation leads to a different final output phase for all inverter after synchronization. Considering the inductive loads for most IPT applications, the output phase and compensation will increase with the operating frequency. When the frequency is increased from 85 kHz to 88 kHz (namely, increase by 3.53%), the compensated CLKS will also increase by 3.53% in theory. In short, the compensated CLKS have to be regulated according to the frequency dynamically. Fig. 11 illustrates the phase regulation process, where the frequency increases from 85 kHz to 88 kHz. The final measured compensated CLKS are $\phi_2 = -78$ and $\phi_3 = -77$, respectively, which is about 3.53% increase compared with the original compensated ones, namely -75 and -74, respectively. As a result, the output phases arrive at a stable status within a few ms because a small compensation change is needed. The output voltages and currents after synchronization with the frequency change are not presented because they are almost the same with those in Fig. 9(e), except the output phases and magnitudes.

Fig. 11. Measured regulation process under frequency varying from 85 kHz to 88 kHz. (a) Output phases. (b) Compensated CLKS of slave inverters.

F. Experiment for Phase Synchronization with Variable Load

Load variation is another possible disturbance besides frequency change. Fig. 12 depicts the regulation process when the load varies from 10 $\Omega$ to 15 $\Omega$. The measured compensated CLKS after synchronization were the same as those before load change, namely, $\phi_2 = -75$ and $\phi_3 = -74$. This is because the operating frequency remains constant, which requires constant compensated CLKS regardless of the load. Additionally, there is an unexpected sharp increase at the beginning of the regulation process in terms of the compensated CLKS. This is attributed to the communication delay of CAN, which imposes an older average output phase to the PI controller. As a result, a wrong error between the average and the measured output
phase leads to an unexpected sharp increase of the compensated CLKs.

In order to avoid the violent fluctuations of the output phases, the compensation regulation can be suspended for a few ms when a sharp change of output phase is detected. Fig. 12(c) and (d) depicts the results with suspended compensation, respectively. One can see that smaller fluctuations are obtained. The suspended action isn’t applied to the case of frequency change. Practically, the controller can detect the frequency change immediately from the input driver pulse signal.

![Figure 12](image)

Fig. 12. Phase regulation process under load varying from 10 Ω to 15 Ω. (a) and (b) are output phases and corresponding compensated CLKs of slave inverters with immediate compensating while (c) and (d) with a regulation suspend of 5 ms after a sharp change of output phase is detected.

VI. CONCLUSIONS

The paper has proposed a novel parallel multi-inverter system with modular inverter for high power IPT applications. Different numbers of slave units can be selected according to the required level of the output current and power, which provides great flexibility for IPT systems with different power requirements. The proposed inverter has good suppression capability for the outer-modular circulating current. A PI controller has been designed, built, and tested to synchronize the output voltages of inverters. Some other significant conclusions can be drawn as follows.

1) Each modular inverter in the parallel multi-inverter system has the same hardware configuration; hence it can operate independently or in parallel multi-inverter schemes, which results in high modularity.

2) For a proper magnetizing inductance $L_M$, the deviation between the output phase of an inverter and the average phase value of all inverters reflects the phase status of the inverter output voltage. If the output phase is lower than the average of all output phases, the output voltage necessarily lags behind the others, and vice versa. This approach provides a possibility for synchronization regulation of the output voltage based on the error between the output phase and the phase average value of all inverters.

3) The required magnetizing inductance $L_M$ increases with the number of parallel inverters in order to correctly reflect the phase status of the inverter output voltage via inverter output phase.

4) For the proposed main-slave phase synchronization control scheme, the paralleled inverters can achieve phase synchronization with the proposed PI controllers in a short time interval even under disturbances of frequency variation or load change.

REFERENCES


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