Modular Parallel Multi-Inverter System for High-Power Inductive Power Transfer

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Abstract—In order to provide high and extendable power levels for inductive power transfer (IPT) system, a parallel multi-inverter system based on modular inverter is presented. Various power requirements can be implemented via adjustment of the number of paralleled inverters, which provide a high modularity. A master-slave scheme is employed for the switching-driver signals of parallel inverters, where one acts as a leader while others as followers. Despite of the master-slave scheme, the proposed circuit topology has natural robustness because of the equality in terms of the hardware configuration of each modular inverter. For proper parameters, the output phase (current lagging corresponding voltage) of an inverter is lower than the average of output phase of all inverters, when its output voltage lags behind others, and *vice versa*. Based on this approach, PI controllers are designed to implement phase synchronization for output voltages of all inverters. An IPT prototype supplied by the proposed parallel multi-inverter with 3 inverters was designed, built and tested. Experiments shown that the proposed parallel multi-inverter system has not only good circulating current suppression capacity, but also excellent performance of phase synchronization. The maximum DC-DC efficiency was 94% at a 35.1 kW receiving power. This paper is accompanied by a Matlab/Simulink file demonstrating phase synchronization control.

Index Terms—Inductive power transfer, modular inverter, parallel-connected inverters, circulating current suppression, phase synchronization.

I. INTRODUCTION

To achieve high power levels while maintaining a high efficiency is a key requirement for many IPT applications, such as fast charging for high speed trains and for electrical vehicles [1]-[6]. Commonly, high power is shared by multiple inverters or invert-legs instead of a single inverter. Multilevel inverters [7], [8], input-series output-parallel (ISOP) inverters [9]-[11], and parallel multi-inverter system [12]-[21] are three typical topologies integrating the power from various inverters. The main issue of multilevel inverters for IPT is voltage-balance [7], [8]. The topology of multilevel inverters has an advantage of voltage stress reduction for semiconductor devices. However, it is hard maintain all inverters in phase at a high-switching frequency for IPT applications, which leads to a

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Digital Object Identifier XXXXXX

possible high voltage un-balance and therefore possible malfunction. Similarly, ISOP topology shares the input DC voltage equally among all inverters, which requires a high input DC voltage to provide high output power, and it is not reported for IPT applications [9]-[11]. With regard to parallel multi-inverter system, the main issue is current-balance [12]-[21]. The parallel multi-inverter topology shares the total current among various inverters while the current un-balance is suppressed by properly designed circulating-suppression controllers [12]-[20] or circuit topologies [21]. For the application of grid-connected inverters or un-interruptible power supply, current-balance controller is relatively easy to implemented because of the low operating frequency (i.e., 50 Hz) and resulting sampling speed requirement [12]-[18]. The droop control is a common algorithm for these 50 Hz applications. However, the current-balance controller is a bit difficult to implement for IPT applications, considering the influence of the high operating frequency on the sampling and the driver signal propagation delay. The literature [19] shows a design of a 3 kW experimental IPT using a parallel two-inverter topology, where a controller based on active and reactive currents decomposition is designed to minimize the circulating current among inverters. The literature [20] presents a parallel topology to integrate power from multiple inverters via transformers. The power sharing is obtained with a synchronous clamp-mode h-bridge control method. Because of the use of high-frequency transformers, the efficiency is dropped down. In practice, its reported efficiency for the power supply is 94% and 80.5% for the whole IPT system considering the loss in the wireless links, respectively. Being subject to the speed of sampling and controller execution, the operating frequencies of [19] and [20] are both 20 kHz instead of 85 kHz

band recommended by the standard of SAE TIR J2954.

The literature [21] proposes an inverter consisting of 6 switching-legs that operates at the band of 85 kHz without any current-balance controller. The output currents from these switching-legs are integrated via 6 coupled inductors. The coupled inductor plays an important role to suppress circulating currents among switching-legs. However, the fixed number of inverter-legs lack of the flexibility, considering various power requirements for different application cases.

Alternatively, this paper presents a novel power-integrating topology with parallel multi-inverters whose output power can be regulated through adjusting the number of paralleled inverters. Fig. 1(a) shows the schematic of the proposed system with n inverters, where coupling ICTs (ICTs, or coupling inductors) are employed to suppress possible outer-modular circulating currents among inverters. A common DC source V_{DC} is employed to feed all inverters. The output voltage from the ith inverter is v_{oi}, where $1 \leq i \leq n$. The voltage v_o is the joint output voltage of the multi-inverter system. In terms of these voltages, the high-order harmonics and the DC components are not considered because only fundamental component can pass through the LC resonant circuit. Fig. 1(b) depicts the equivalent circuit of Fig. 1(a), where each ICT (ICT$_1$, for example) is composed of a primary inductor (L_{1P}, for example), a secondary inductor (L_{1S}, for example), a leakage inductor (L_{leak} for both sides), and a parasitic resistance r_{ICT}. The branch impedance Z_b represents the total equivalent series resistance and reactance as

$$Z_b = 2j\omega L_{leak} + 2r_{ICT}. \qquad (1)$$

To provide higher output current, each modular inverter consists of 4 half-bridge switching-legs, which are connected in parallel with 4 ICTs as shown in Fig. 1(c) [21]. The 4 switching-legs share a common DC voltage source V_{I1}. v_{11} through v_{14} are the fundamental components of voltages generated by these 4 switching-legs, respectively. The ICTs are employed to suppress both the inner-modular circulating currents among legs of an inverter module and the outer-modular circulating currents among inverters [21]. Moreover, various power requirements can be implemented via adjusting the number of paralleled inverters, which provides a high modularity and extendibility.

Phase synchronization is the key issue resulting from parallel operation of multi-inverters, although it is not much difficult for grid-connected inverters due to the low operating frequency and the existence of phase reference from the grid. A high phase asynchrony leads to large circulating currents and power losses. For multi-switching-legs in the same inverter, driver delay is relatively small and ignored in this paper. Beyond the inverter topology and circulating current suppression method proposed in literature [21] with constant number of switching-legs, the main target of the paper is to provide a mast-slave control strategy to implement phase synchronization for parallel multi-inverters employed by high power IPT. Although a master-slave scheme is employed for the phase synchronization control, the proposed circuit topology has natural robustness because of the equality in terms of the hardware configuration of each modular inverter. That's to say,

all inverter have the same hardware configuration. A distinguish address (namely, 0 through 255) is assigned to different modular inverter. At the start-up stage, all inverters share their addresses via the CAN bus while the inverter with the smallest address behaves as the master one. When some a slave inverter is broken down (for example, its CAN communication is lost), its status can be detected by the main unit and removed from the parallel system. The removing action involves some re-arrangement of the ICTs which is not detailed because of the limit length of article. When the master inverter is broken down (for example, its CAN communication is lost or no pulse is transferred to slave ones), the failure will be detected by slave inverters easily and the slave inverter with the smallest address will take the place of the original master inverter. In general, the proposed topology has nice robustness attributed to good equality in terms of the hardware configuration of each modular inverter.
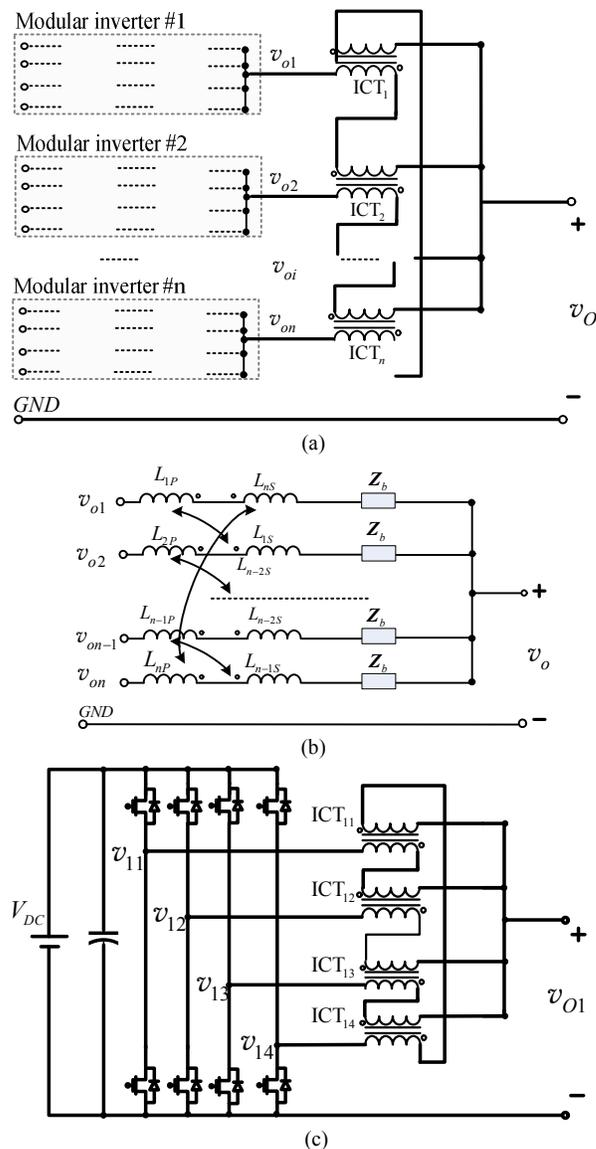
Fig. 1. Scheme of parallel multi-inverter system for high power IPT. (a) Parallel multi-inverter system with n modular inverters. (b) Equivalent circuit of (a). (c) Modular inverter with 4 switching-legs.

For a multi-inverter system, where the slave inverters follow

the switching signal of the master inverter, the switching frequency is the same for all inverters while the phase asynchrony is mainly attributed to the transmission delay of components in the signal transmission pathway. Hence, one has to detect and compensate the delay to achieve phase synchronization. The direct measurement method, which measures the phase differences between the inverter output currents and the joint current can be employed, where extra measurement components are required. Alternatively, an indirect measurement method, which does not involve the joint current but employees the output phase for zero-voltage-switching (ZVS) detection is proposed. The output phase refers to the angle, the current lags the voltage of an inverter. Considering the measurement of output phase for ZVS is always needed in a practical IPT system, the proposed indirect method is cost saving.

The rest of this paper is organized as follows: Section II analyzes the output phase angles under various numbers of paralleled inverters, while Section III conducts simulations to analyzes the relation between the output phase (the current lagging the corresponding voltage) and phase (the output voltage lagging the reference) of the inverter. Section IV designs a controller to synchronize the phase for various inverters. Finally, a laboratory prototype with 3 modular inverters was designed, built, and tested to supply an IPT system up to 35.1 kW. Experimental results are provided to validate the theoretical analyzes and conclusions are drawn.

II. ANALYSIS OF OUTPUT PHASE ANGLE

Assuming all windings of ICTs for outside of inverters (namely, ICT_1 through ICT_n) have the same number of turns. Hence, inductances of the primary inductor and the secondary inductor of the ICT are equal to the magnetizing inductance L_M. Based on the Kirchhoff law in frequency-domain, the relationship between the output voltages and currents from various inverters presented in Fig. 1(a) can be expressed by

$$v_{o1} - v_o = (2j\omega L_M + \mathbf{Z}_b)i_{o1} - j\omega M_{ICT}i_{on} - j\omega M_{ICT}i_{o2}$$
$$v_{o2} - v_o = (2j\omega L_M + \mathbf{Z}_b)i_{o2} - j\omega M_{ICT}i_{o1} - j\omega M_{ICT}i_{o3}$$
$$\dots \qquad , \qquad (2)$$
$$v_{on-1} - v_o = (2j\omega L_M + \mathbf{Z}_b)i_{on-1} - j\omega M_{ICT}i_{on-2} - j\omega M_{ICT}i_{on}$$
$$v_{on} - v_o = (2j\omega L_M + \mathbf{Z}_b)i_{on} - j\omega M_{ICT}i_{on-1} - j\omega M_{ICT}i_1$$
$$v_o = \mathbf{Z}_{load}i_o$$
$$i_o = \sum_{i=1}^n i_{oi}$$

where i_{o1} through i_{on} are the output currents from various inverters, M_{ICT} is the mutual inductance between the two windings of the ICT, namely,

$$M_{ICT} = L_M , \qquad (3)$$

i_o and $\mathbf{Z}_{load}$ are the total output current and the input impedance, respectively. Substitution (3) into (2), one can yield output current from each inverter easily.

For the system with 2 inverters, the currents from various inverters are

$$i_{o1} = \frac{\mathbf{Z}_{load}(v_{o1} - v_{o2}) + 2j\omega L_M(v_{o1} + v_{o2}) + 2j\omega \mathbf{Z}_b v_{o1}}{4(\mathbf{Z}_{load} + j\omega \mathbf{Z}_b)(2j\omega L_M + j\omega \mathbf{Z}_b)} . \qquad (4)$$
$$i_{o2} = \frac{\mathbf{Z}_{load}(v_{o2} - v_{o1}) + 2j\omega L_M(v_{o1} + v_{o2}) + 2j\omega \mathbf{Z}_b v_{o2}}{4(\mathbf{Z}_{load} + j\omega \mathbf{Z}_b)(2j\omega L_M + j\omega \mathbf{Z}_b)}$$

Under the condition that the branch impedance $\mathbf{Z}_b$ is much lower than $\mathbf{Z}_{load}$ and can be ignored, (4) is simplified to

$$i_{o1} = \frac{\mathbf{Z}_{load}(v_{o1} - v_{o2}) + 2j\omega L_M(v_{o1} + v_{o2})}{8j\omega L_M \mathbf{Z}_{load}} . \qquad (5)$$
$$i_{o2} = \frac{\mathbf{Z}_{load}(v_{o2} - v_{o1}) + 2j\omega L_M(v_{o1} + v_{o2})}{8j\omega L_M \mathbf{Z}_{load}}$$

When all inverters are fed by a common DC voltage source V_{DC}, the output voltages from inverters can be assumed to have the same amplitude V_{amp}. Hence, v_{o1} and v_{o2} can be expressed by

$$v_{o1} = V_{amp}e^{j\theta_1} , \qquad (6)$$
$$v_{o2} = V_{amp}$$

where θ_1 is the phase angle that voltage v_{o2} lags behind v_{o1}. The impedances of inverters are

$$\mathbf{Z}_{o1} = \frac{v_{o1}}{i_{o1}} , \qquad (7)$$
$$\mathbf{Z}_{o2} = \frac{v_{o2}}{i_{o2}}$$

Substitution (5) and (6) into (7) yields the impedances

$$\mathbf{Z}_{o1} = \frac{8j\omega L_M \mathbf{Z}_{load}}{\mathbf{Z}_{load}(1 - e^{-j\theta_1}) + 2j\omega L_M(1 + e^{-j\theta_1})} . \qquad (8)$$
$$\mathbf{Z}_{o2} = \frac{8j\omega L_M \mathbf{Z}_{load}}{\mathbf{Z}_{load}(1 - e^{j\theta_1}) + 2j\omega L_M(1 + e^{j\theta_1})}$$

One defines the output phases for various inverters as

$$\phi_1 = \text{atan2}(\text{imag}(\mathbf{Z}_{o1}), \text{real}(\mathbf{Z}_{o1})) , \qquad (9)$$
$$\phi_2 = \text{atan2}(\text{imag}(\mathbf{Z}_{o2}), \text{real}(\mathbf{Z}_{o2}))$$

where atan2 is the arctangent function with two arguments whose output range is $-\pi$ to $-\pi$. The functions imag and real are employed to obtain the imaginary part and the real part, respectively.

For a multi-inverter system with 3 inverters, the output currents from inverters can be obtained from (2) as

$$i_{o1} = \frac{\mathbf{Z}_{load}(2v_{o1} - v_{o2} - v_{o3}) + 2j\omega L_M(v_{o1} + v_{o2} + v_{o3})}{9j\omega L_M \mathbf{Z}_{load}}$$
$$i_{o2} = \frac{\mathbf{Z}_{load}(2v_{o2} - v_{o1} - v_{o3}) + 2j\omega L_M(v_{o1} + v_{o2} + v_{o3})}{9j\omega L_M \mathbf{Z}_{load}} . \qquad (10)$$
$$i_{o3} = \frac{\mathbf{Z}_{load}(2v_{o3} - v_{o1} - v_{o2}) + 2j\omega L_M(v_{o1} + v_{o2} + v_{o3})}{9j\omega L_M \mathbf{Z}_{load}}$$

To analyze the influence of the output voltage delay on the output phase angle, one assumes that the output voltages of all slave inverters are the same while v_{o1}(representing the voltage of the master inverter) leads them by a angle θ_1, namely

$$v_{o1} = V_{amp}e^{j\theta_1} , \qquad (11)$$
$$v_{o2\sim3} = V_{amp}$$

where $v_{o2\sim3}$ represents the voltages v_{o2} and v_{o3}. Considering the equivalence of all slave inverters in terms of driver signal propagation delay, the assumption that the output voltages of all slave inverters are the same is reasonable. In the following analysis, v_{o1} refers to the output voltage of the master inverter

while other voltages (i.e., v_{o2}, v_{o3}, v_{o4}, and so on) refer to those for slave inverters.

As a result, the impedances of inverters are

$$Z_{o1} = \frac{9 j\omega L_M Z_{load}}{Z_{load}(2-2e^{-j\theta_1}) + j\omega L_M (1+2e^{-j\theta_1})} \quad . \quad (12)$$

$$Z_{o2} = Z_{o3} = \frac{9 j\omega L_M Z_{load}}{Z_{load}(1-e^{j\theta_1}) + j\omega L_M (2+e^{j\theta_1})}$$

With the same assumption used by (11), the impedances for system with 4, 5, and 6 parallel inverters are given in (13) through (15), respectively

$$Z_{o1} = \frac{16 j\omega L_M Z_{load}}{Z_{load}(5-5e^{-j\theta_1}) + j\omega L_M (1+3e^{-j\theta_1})}$$

$$Z_{o2} = Z_{o4} = \frac{16 j\omega L_M Z_{load}}{Z_{load}(1-e^{j\theta_1}) + j\omega L_M (3+e^{j\theta_1})} \quad (13)$$

$$Z_{o3} = \frac{16 j\omega L_M Z_{load}}{Z_{load}(3-3e^{j\theta_1}) + j\omega L_M (3+e^{j\theta_1})}$$

$$Z_{o1} = \frac{25 j\omega L_M Z_{load}}{Z_{load}(10-10e^{-j\theta_1}) + j\omega L_M (1+4e^{-j\theta_1})}$$

$$Z_{o2} = Z_{o5} = \frac{25 Z_{load}}{(4+e^{j\theta_1})} \quad (14)$$

$$Z_{o3} = Z_{o4} = \frac{25 j\omega L_M Z_{load}}{Z_{load}(5-5e^{j\theta_1}) + j\omega L_M (4+e^{j\theta_1})}$$

$$Z_{o1} = \frac{72 j\omega L_M Z_{load}}{Z_{load}(35-35e^{-j\theta_1}) + 2 j\omega L_M (1+5e^{-j\theta_1})}$$

$$Z_{o2} = Z_{o6} = \frac{72 j\omega L_M Z_{load}}{Z_{load}(5-5e^{j\theta_1}) + 2 j\omega L_M (5+e^{j\theta_1})} \quad (15)$$

$$Z_{o3} = Z_{o5} = \frac{72 j\omega L_M Z_{load}}{Z_{load}(13-13e^{j\theta_1}) + 2 j\omega L_M (5+e^{j\theta_1})}$$

$$Z_{o4} = \frac{72 j\omega L_M Z_{load}}{Z_{load}(19-19e^{j\theta_1}) + 2 j\omega L_M (5+e^{j\theta_1})}$$

The impedance expressions for more numbers of parallel inverters can also be obtained from (2), but it is somewhat complex and not presented here. As a result, the output phases for various inverters can be obtained with the same method expressed by (9).

III. SIMULATION FOR OUTPUT PHASE ANGLE

To provide a stable supply for the IPT system, all inverters composing the parallel multi-inverter system should operate in phase. A main-slaver scheme is employed for the phase synchronization of parallel multi-inverter system, where one inverter acts as the leader while others follow the leader regarding to the frequency and phase. Although the phase deviations between various output voltages reflect the status of phase synchronization directly, they are hard to measure correctly because of the high operating frequency together with the inevitable inconsistency of propagation delay of measured signals. In contrast, the measurement of the output phase of an inverter is more precise because all signal pathways are in the same PCB board. Hence, the output phase instead of the output voltage phase is sampled for the phase synchronization control. The rest of this section analyzes the relation between the output phases (current lagging voltage of corresponding inverter), the average of them for all inverters, and the output voltage phase

of the inverter. The expected conclusion is that the deviation between the output phase of an inverter and the average of all inverters reflects the in-phase status of the inverter output voltage.

Regarding to a practical inverter, the output phase angle defined by its output current lagging voltage is easy to measure and commonly used for ZVS detection [4]. To find the relations between the output phase and the voltage delay angle, simulations are conducted for a typical S-S compensated IPT system shown in Fig. 2,
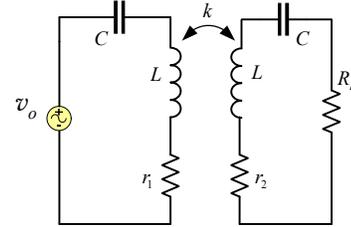
Fig. 2. A typical S-S compensated IPT system.

where v_o represents the joint output voltage from parallel interferers, C and L are the resonant capacitors and inductors, r_1 and r_2 are parasitic resistances, k is the coupling factor between two sides, and R_L is the equivalent load resistance, respectively. The parameters for the simulations are listed in Table I.

TABLE I
PARAMETERS FOR SIMULATIONS

symbol	parameter	value
f	Operating frequency	85 kHz
k	Coupling coefficient between the sending and receiving coils	0.22
L	Resonant inductance at both the sending side and the receiving side	32.5 µH
C	Resonant capacitance at both the sending side and the receiving side	113.0 nF
r_1	Parasitic resistance at the sending side	50 mΩ
r_2	Parasitic resistance at the receiving side	50 mΩ
R_L	Load resistance at the receiving side	8.0 Ω

Besides the parameters listed in Table I, the magnetizing inductance L_M of ICTs has an important impact on the output phase as shown in (8) and (12) through (15). A high L_M is expected in terms of good circulating current suppression capacity. However, the higher parasitic resistance resulting from a higher L_M degenerates the overall efficiency.

Hence, a relatively small L_M, which is half of the resonant inductance L, is employed for the first 5 simulations, then 3 simulations with higher L_M are conducted for expected result. Fig. 3 depicts the relations between output phases (namely, ϕ_1 ϕ_2, ϕ_3, …) versus the output voltage delay angle θ_1 that the slave inverters lag behind the master inverter. The average ϕ_{avg} of the output phases for all inverters is also shown for comparison.

Ignoring Fig. 3(d), (e), and (g), some important conclusions can be drawn from Fig. 3:

1) When the output voltages of slave inverters are in phase with that of the master inverter (i.e., $\theta_1 = 0$), their output phases (i.e., ϕ_2 through ϕ_n) are equal to the average of all output phases (i.e., ϕ_{avg}).

(a), for $n=2$ and $L_M=0.5L$ (b), for $n=3$ and $L_M=0.5L$ (c), for $n=4$ and $L_M=0.5L$ (d), for $n=5$ and $L_M=0.5L$

(e), for $n=6$ and $L_M=0.5L$ (f), for $n=5$ and $L_M=L$ (g), for $n=6$ and $L_M=L$ (h), for $n=6$ and $L_M=2L$
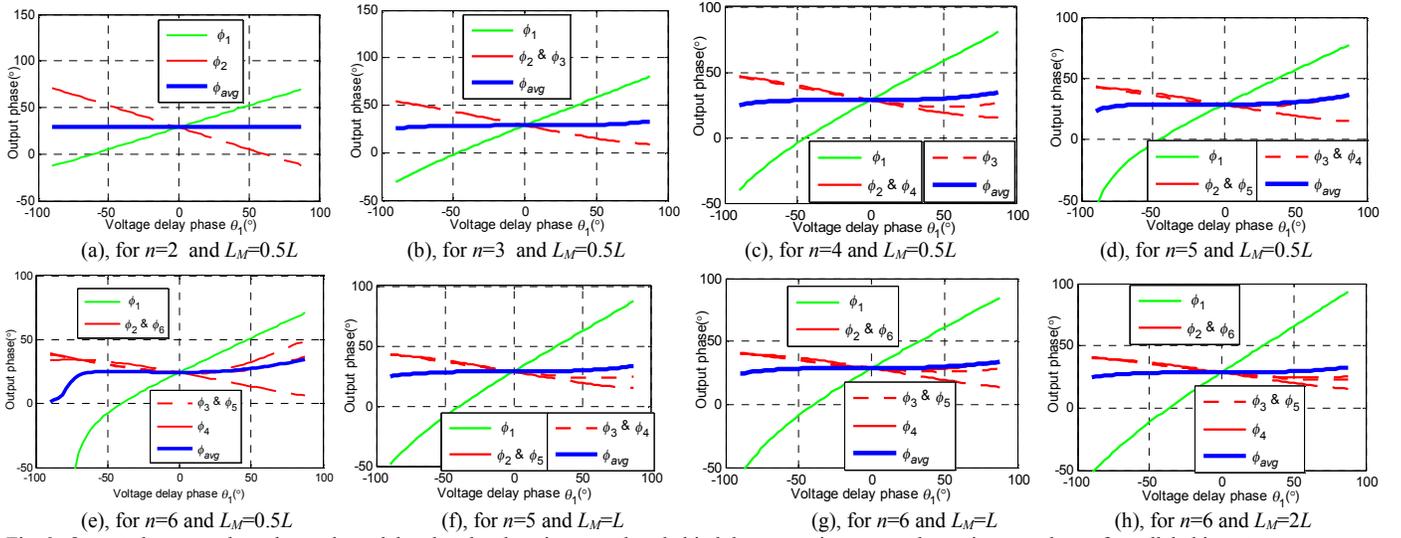
Fig. 3. Output phases vs. the voltage phase delay that the slave inverters lags behind the master inverter under various numbers of paralleled inverters

2) When the output voltages of slave inverters lead that of the master inverter (i.e., $\theta_1 < 0$), their output phase (i.e., ϕ_2 through ϕ_n) are higher than the average of all output phases (i.e., ϕ_{avg}), and *vice versa*. This character can be explained as follows: All of the inverters output currents tend to be almost in-phase because of the existence of coupling inductors. As a result, the inverter, whose output voltage leads the others, has a higher phase difference between its voltage and the "in-phase" current, namely, a higher output phase.

3) The output phase of the master inverter (i.e., ϕ_1) strictly monotonically increases with the voltage delay phase (i.e., θ_1). Although there is a different rate of increase, this conclusion is always correct under various numbers (from 2 through 6) of parallel inverters.

4) The average of output phase ϕ_{avg} is almost constant under various voltage delay phase θ_1 and numbers of parallel inverters.

However, some plots in Fig. 3(d), (e), and (g) are not rigidly consistent with above conclusions. By comparing Fig. 3(d) with (f), and (g) with (h), however, one can see that the inconsistency can be eliminated with employing a modestly higher magnetizing inductance L_M of the ICTs.

In short, under proper parameters, the deviation between the output phase of an inverter and the average of all inverters reflects the in-phase status of the inverter output voltage. To achieve synchronization, in general, one can regulate its output voltage phase based on the error between its output phase and the average of all output phases. Based on above analysis, a control scheme is designed in the following sub-section.

IV. PHASE SYNCHRONIZATION CONTROL

A. Controller Scheme for Phase Synchronization

Fig. 4 depicts the control scheme of the phase synchronization for the parallel multi-inverter system where a master-slave structure is employed. Although more inverters can be added in, only two slave units are employed in Fig. 4 for simplification. The main control unit generates a square wave signal, which drivers the inverter #1 directly (in practice,

isolated driver components are included but ignored here for simplification). The average value of output phases is calculated in the main unit. The square wave signal from the main control unit is also transmitted to other slave control units via physical signal wires together with corresponding transceivers for each unit board. The phases $\Delta\phi_2$ and $\Delta\phi_3$ represent the time delays due to the introduction of the transceivers and signal propagation pathways. ϕ_1 is the output phase determined by the current lagging the voltage of the inverter in the main unit, and similarly for ϕ_2 and ϕ_3 in the slave units, respectively. ϕ_{avg} is the average value of output phases for all inverters. Err_{2_avg} and Err_{3_avg} are the errors of the output phases and the average value, respectively. ϕ_{c2} and ϕ_{c3} are the outputs of PI controllers, respectively. $\Delta\phi_{c2}$ and $\Delta\phi_{c3}$ are the angles which compensate the delays of $\Delta\phi_2$ and $\Delta\phi_3$, respectively. When a minus output from the PI controller happens, an angle of 2π is added to it to obtain a positive compensated phase always.
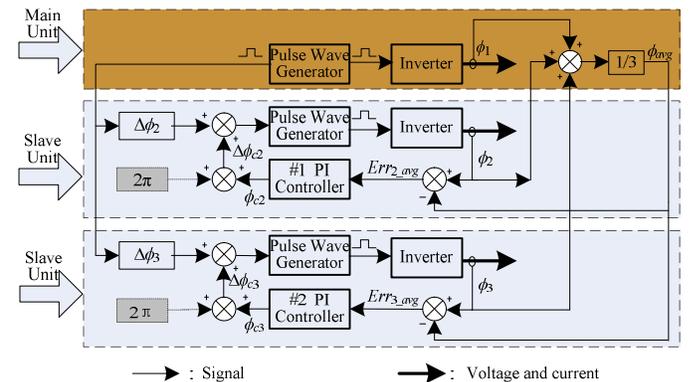
Fig. 4. Master-slave control scheme of the phase synchronization for the parallel multi-inverter system

Despite of different software configuration regarding to different unit, their hardware configuration is the same. If one more slave unit is added, for example, only one modification is required in the average calculation whose coefficient is changed from 1/3 to 1/4 except the hardware of the added

unit. This character provides a good extendibility for the proposed parallel multi-inverter system.

B. Controller Simulation

With regard to #1 PI controller operating in the first slave unit, the position control algorithm can be expressed as

$$\emptyset_{c2}(k+1) = K_p \times Err_{2\_avg}(k) + K_i \times \sum \left(Err_{2\_avg}(k) \right), \quad (22)$$

where K_p and K_i are the proportion coefficient and the integral coefficient, respectively, and $\sum \left(Err_{2\_avg}(k) \right)$ represents the accumulation of deviations Err_{2_avg} till the k calculation, respectively. The same control algorithm is applied to the other slave inverters.
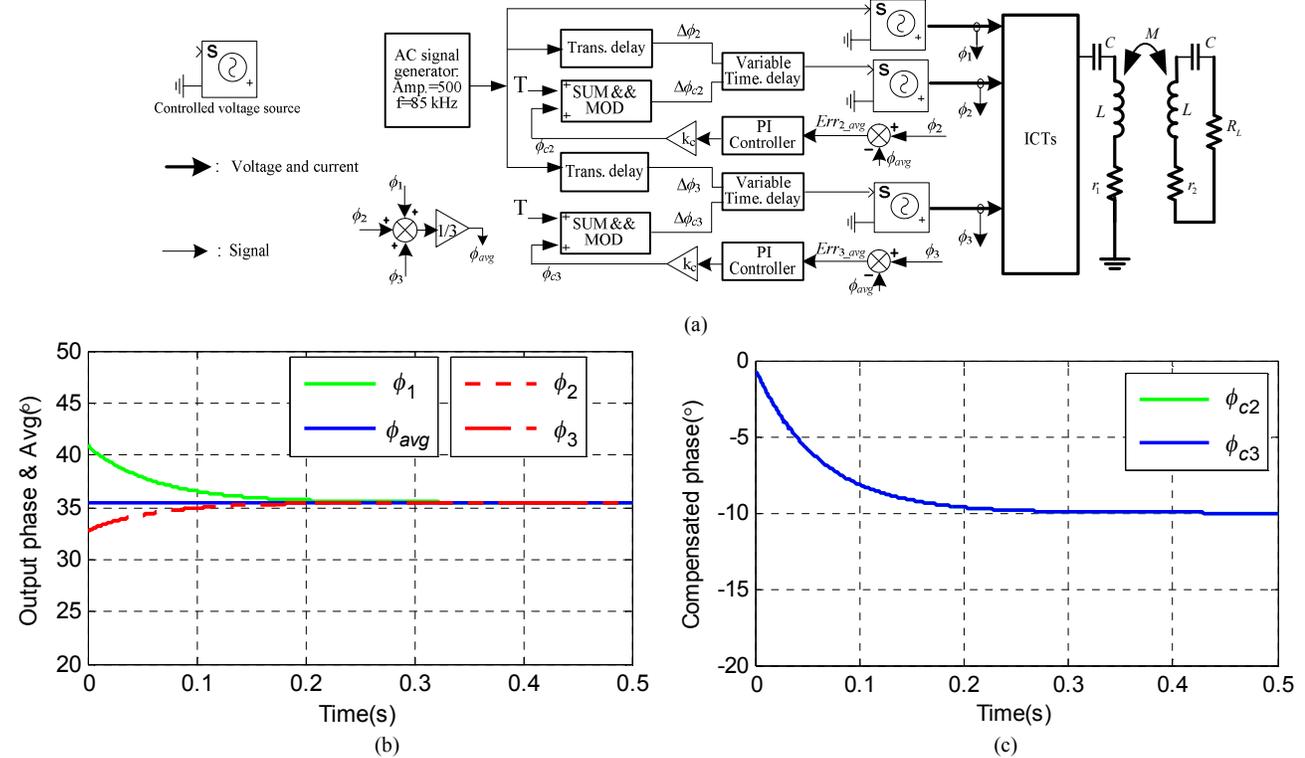
Fig. 5. Simulink simulated circuit and simulated regulation process of phase synchronization for a parallel multi-inverter with 3 inverters and a given initial delay of 10° for both slave inverters. (a) Simulink circuit. (b) Output phases and their average. (c) Compensated phases of two slave inverters

Fig. 5 depicts the SIMULINK simulation circuit model and the regulation process with PI controllers at the start-up stage. The discrete sampling time of the SIMULINK model is 1e^{-7} s. For the PI controller, a shorter sampling time commonly results to a faster response. However, the communication speed of the CAN bus is limited. As a result, the sampling rate of the PI controller is 1 kHz. In Fig. 5(a), inverter is replaced by a controlled AC voltage source whose phase is regulated by a variable time delay module. The initial driver phase delay is depicted by a transport delay module. Output phase is measured by Fourier module which is not shown for simplification. ICTs consist of 3 mutual inductance modules whose self inductance, mutual inductance and self resistance are 16.25μH, 14.25μH and 50 mΩ, respectively. The subsystem 'SUM && MOD' gets the sum of two inputs then outputs the modulo value, namely mod(sum, T) where T is the period in second unit, namely, 1/85000 s. As the input and output of the PI controller are based on degree unit while other modules, including transport delay, SUM && MOD and variable time delay are time based, a grain $k_c = 1/85000/360$ is employed to transfer the unit of degree to the time unit of second. The resonant inductances, capacitances , parasitic resistances, load resistance and mutual inductance are the same with listed in Tab. I. After analyzing and adjusting the

PI parameters to obtain a curve with better dynamic performance, parameters $K_p = 0.25$ and $K_i = 0.06$ were employed for both slave inverters. Fig. 5(b) and (c) depicts the regulation process regarding to the output phases and their average value at the startup stage with the given initial delay of 10° (namely, transport delay of 1/85000/36 s) for both slave inverters. One can see that all inverters arrive at a phase synchronization within about 0.3 s. Note that ϕ_2 and ϕ_3 depicted in Fig. 5(b) are overlapped, and similarly for ϕ_{c2} and ϕ_{c3} in (c) .

V. PROTOTYPE AND EXPERIMENTAL VERIFICATION

A. Prototype of Parallel Multi-inverter System

Fig. 6 shows the parallel multi-inverter prototype, where the modular inverter is depicted in (a). The modular inverter is mainly composed of three modules, namely, the control card, the driver card, and the power stage. Additionally, heat sinks are employed for the inverter switches. Two driver cards, each consists of four isolated drivers, are employed to connect the control card and the power stage. Two MCUs, namely, an FPGA of XC6SLX9-3TQG144I and an ARM of STM32F407VGT, and other auxiliary components constitute the control card. The half-bridge switching legs of the inverter

are constructed with C2M0025120D SiC MOSFETs whose nominal parameters are 1200 V and 90 A. For the inner-module circulating current suppression, four ICTs for each modular inverter are manufactured with toroidal core of T300-2 and Litz-wire of 500×0.1 mm. The self-inductance about 10 µH and the leakage inductance about 1.6 µH were obtained with 30 winding turns at each side of the ICTs.

(a)

(b)
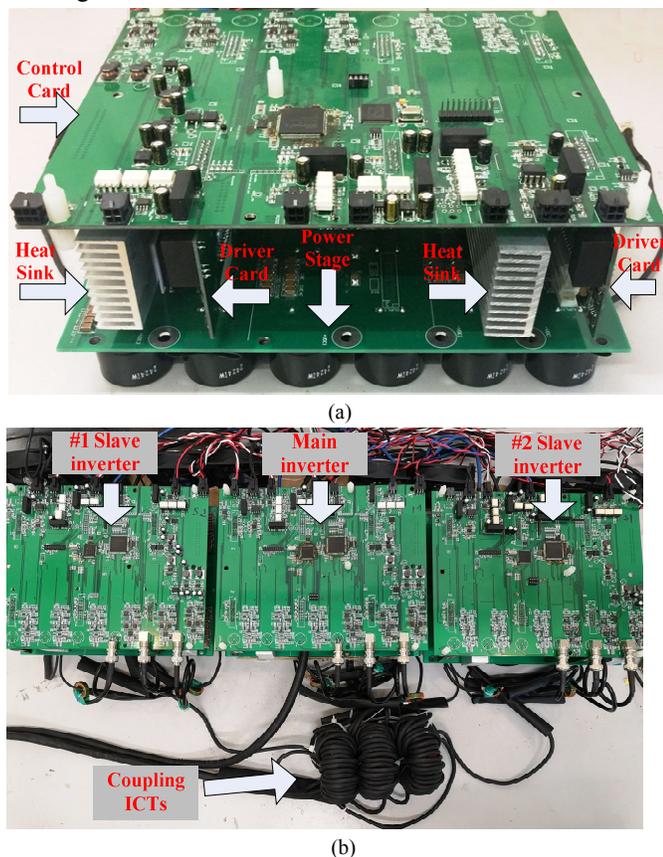
Fig. 6. Prototype of parallel multi-inverter system. (a) Modular inverter with four switching legs. (b) Parallel multi-inverter system with three modular inverters

The square wave driver signal for each C2M0025120D is generated by an FPGA. The FPGA operates at a frequency of 199.5 MHz. Hence, the driver signal switches for each 1173 FPGA CLKs to generate a system operating frequency of 85 kHz. The FPGA samples the output phase between the current and the voltage outputted from the same switching leg with the help of zero-crossing module, then sends the angle value to corresponding ARM via SPI communication. For the prototype, all phases including the switching periods, the output phases and the compensated phases are measured or represented by CLKs of FPGA whose counting frequency is 199.5 MHz. Namely, a period of 2347 FPGA CLKs are equal to 360° at an operating frequency of 85 kHz.

The parallel multi-inverter system consisting of three modular inverters is shown in Fig. 6(b), where one plays the leader and the others act as followers. If a higher power level is required, more modular inverters can be added while things left to do are the selection of proper coupling inductors with corresponding number of ICTs and modifying the coefficient for the output phase average value calculated according to the

number of the paralleled inverters. For the outer-module circulating current suppression, 3 higher power ICTs were manufactured. Each of them is with 2 toroidal cores T300-2 and Litz-wire of 1000×0.1 mm. The self-inductance about 14 µH and the leakage inductance about 2 µH were obtained with 24 winding turns at each side of the ICTs.

The square wave driver signal generated by the FPGA in the main control card is transmitted to the slave cards via transceivers, besides the driver of the inverter of the main unit. The MAX485 was employed as the transceivers because of its good anti interference capability resulting from its differential driver mode. Besides that, the main control card receives the phase angles from two slave cards, then calculates the average value of these three and sends back to the slave control cards via CAN communication. The PI controller operates in each ARM of the slave control card, and outputs corresponding compensated CLKs to the FPGA, which generates square wave driver signal according to the receiving square wave driver signal and the compensated CLKs. For simplification, only one signal for the upper switch driver is sent to the slave inverter. Hence, the FPGA of slave inverter detects the switching frequency and the duty via the change of the received pulse signal and generates driver signal for the lower switch.

B. Prototype of IPT

An S-S compensated IPT supplied by the proposed parallel multi-inverter system with three modular inverters was constructed and shown in Fig. 7. Three adjustable DC voltage source modules REG75030 were connected in parallel to obtain a high power common DC bus feeding all inverters. The nominal parameters of REG75030 are 750 V and 20 A. Regarding dimensions, both coils at the sending and receiving sides were the same: a rectangle 89 cm by 69 cm at the outer sides and 84 cm by 64 cm at the inner sides. Each planar solenoid coil contains 4 turns of Litz-wire, which consists of 5000 isolated strands with an outer diameter of 10 mm. The diameter of the strand is 0.1 mm. The gap of two coils is 20 cm.
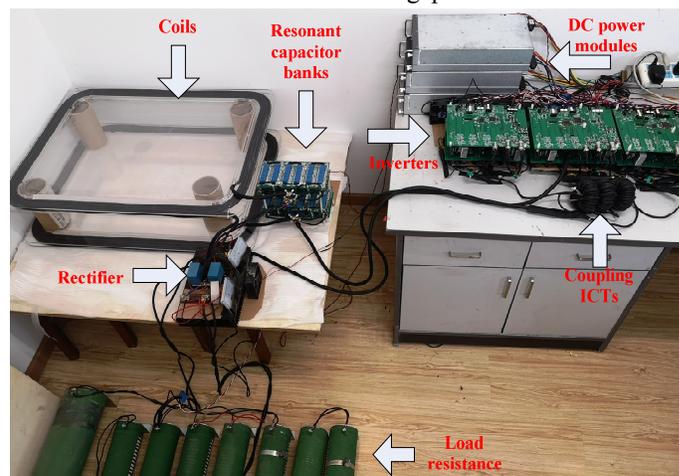
Fig. 7. The IPT prototype supplied by the proposed parallel multi-inverter system

C. Experiment for Circulating Current Suppression under Phase Out-sync

TABLE II
PARAMETERS FOR THE IPT SYSTEM

symbol	parameter	value
f	Operating frequency	85 kHz
f_{FPGA}	FPGA clock frequency	199.5 MHz
d	Gap between two coils	20 cm
M	Coupling inductance of two coils	7.25 µH
L_P	Resonant inductance at the sending side	32.3 µH
C_P	Resonant capacitance at the sending side	113.1 nF
r_{CS}	Parasitic resistance of the resonant capacitor at the sending side	2 mΩ
r_{LS}	Parasitic resistance of the resonant inductor at the sending side	25 mΩ
L_S	Resonant inductance at the receiving side	31.6 µH
C_S	Resonant capacitance at the receiving side	112.4 nF
r_{CP}	Parasitic resistance of the resonant capacitor at the receiving side	2 mΩ
r_{LP}	Parasitic resistance of the resonant inductor at the receiving side	22 mΩ
R_{load}	Load resistance of the rectifier at the receiving side	10.5 Ω
L_{M_I}	Magnetizing inductances of ICTs for inner-circulating current suppression	9.7 µH~10.2 µH
L_{leak_I}	Leakage inductances of ICTs for inner-circulating current suppression	1.55 µH~1.62 µH
r_{ICT_I}	Parasitic resistance at each winding of ICTs for inner-circulating current suppression	29.4 mΩ~30.9 mΩ
L_{M_O}	Magnetizing inductances at each winding of ICTs for inner-circulating current suppression	13.7 µH~13.9 µH
L_{leak_O}	Leakage inductances at each winding of ICTs for inner-circulating current suppression	1.82 µH~2.07 µH
r_{ICT_O}	Parasitic resistance at each winding of ICTs for inner-circulating current suppression	18.7 mΩ~20.6 mΩ
r_{DS}	Parasitic resistance of the MOSFET	25 mΩ
Q_g	Charge at the MOSFET gate	161 nC
t_r	Raising time of the MOSFET	32 ns
t_f	Falling time of the MOSFET	28 ns
V_F	Forward voltage drop of the rectifier at the receiving side	1.87 V
r_{CF}	Parasitic resistance of the rectifier filter capacitor	8 mΩ

Considering a high AC current and resulting high reactive voltage, 226 film capacitors, 1 nF each, were connected in parallel, then in series with other 226 ones, 1 nF each, to form a 113 nF compensated capacitance at both sides. At the receiving side, two DSEI2X101-12A rectifiers were used to construct a full-bridge rectifier. The main parameters are listed in Table II, where resistances, inductances, and capacitances were measured with an Agilent E4980A LCR meter at 85 kHz.

Because of the component propagation delays in the transmission pathway of the driver signal, the driver signals and the output voltages of the slave inverters will lag behind those of the master inverter at the initial status. In order to check the suppressing capability for circulating current due to phase out-sync, the output currents from the master inverter and one slave inverter are measured under initial phase out-sync, where the phase delay compensations are not employed. Under a common input DC voltage 100 V for inverters, the output voltages and currents are captured by a 4-channel oscilloscope, Tektronix DPO 2004B and shown in Fig. 8(a), where channel 3 and 2 show for the output voltage and current of the master inverter, while channel 4 and 1 show those of the slave inverter,

respectively. The waveforms for both slave inverters were almost the same; therefore those for another slave one are not presented. From the voltage waveforms of Fig. 8(a), one can observe that the voltage phase difference is about 12°, which is mainly attributed to the MAX485 transceivers in the driver signal pathway. The current difference between two inverters were below 0.5 A, which shows that the coupling inductors has good suppression capacity in terms of the outer-circulating current. Moreover, an experiment with a deliberate additional 5° (namely, 33 FPGA CLKs under 85 kHz operating frequency) delay besides the initial delay is applied to this slave inverter, was conducted to examine the currents. Fig. 8(b) shows that the current difference increases with the phase delay, but still remains a small one.

Additionally, output currents from various inverters show small phase difference for both cases of the initial driver signal delay and the deliberate 5° delay. As a result, the phase difference of output phases (namely, the current lags behind the corresponding voltage) is almost determined by the difference of the voltages while that of currents plays an ignorable role. Conversely, the relative magnitudes of output phases reflect their magnitudes of phase delays, which agrees with the conclusion of simulation in Section III.

(a)

(b)
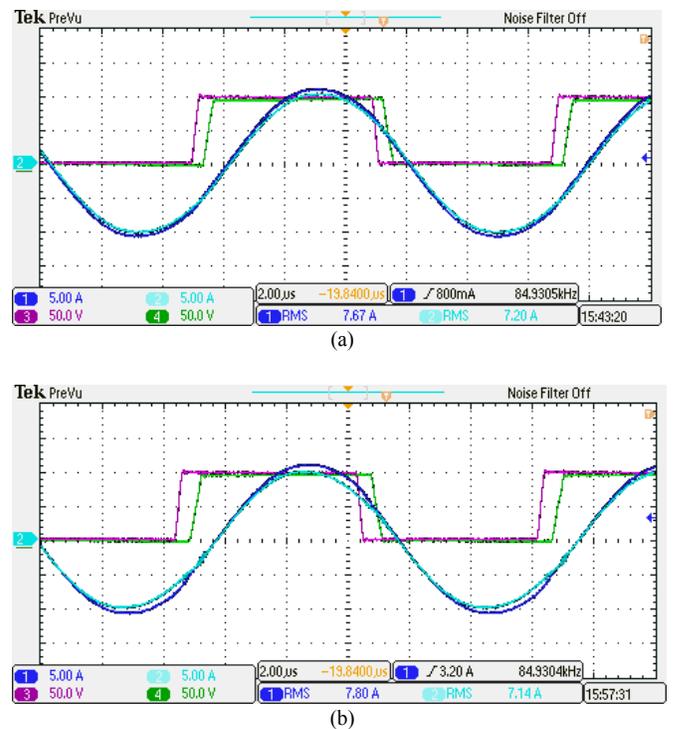
Fig. 8. Output voltages and currents without delay compensation of driver signal . (a) is for the initial phase out-sync and (b) is for an additional driver delay of 5° besides the initial one.

D. Experiment for Phase Synchronization at Startup Stage

A comparator of TS3011 was employed to detect the zero-crossing for output phase measurement. It was found that the output of TS3011 was unstable under a small output current. Hence, the PI controllers remain deactivated till an input DC voltage was above 103 V. For the DC voltage from 100 V to

105 V, both PI controllers work together to regulate the phases of output voltages as soon as detecting a DC voltage above 103 V.

The PI parameters of the prototype were the same as mentioned in Section IV.B, namely, $K_p = 0.25$, $K_i = 0.06$ and a sampling rate of 1 kHz. The output phases, their average and compensated phases are sampled and stored by corresponding ARMs and uploaded to a private computer with RS232 communication if required. For the initial case, the measured output phases of the master inverter and two slave ones were 250, 188 and 194 CLKs, respectively. The measured delay compensations of two slave inverters after synchronization were $\phi_{c2} = -75$ and $\phi_{c3} = -74$ CLKs, respectively. As a result, the practical compensations executed by the FPGA were $\Delta\phi_{c2}=2272$ and $\Delta\phi_{c3}=2273$ considering 2π (namely, 2347 CLKs at 85 kHz) is added for minus compensations, respectively. In fact, the compensated CLKs of -75 can also be expressed by -11.5° considering the period of 2347 CLKs at 85 kHz, which had good agreement with the measured delay of 12° shown in Fig. 8(a). This verifies that the PI controller can trace the phase delay correctly.

For the case of a deliberate 5° (namely, 33 CLKs) delay besides the initial one, the measured output phases of the master inverter and two slave ones were 246, 165, and 203 CLKs, respectively. The measured delay compensations of two slave inverters after synchronization were $\phi_{c2} = -108$ and $\phi_{c3} = -74$ CLKs, respectively. As a result, the practical compensations executed by the FPGA were $\Delta\phi_{c2}=2239$ and $\Delta\phi_{c3}=2273$, respectively. Considering the delay of 16.5° (a initial delay of 11.5° plus a deliberate 5°) equals to 108 CLKs at 85 kHz, one can see that PI controller can compensate the delay correctly.

Fig. 9 illustrates the regulation process of the phase synchronization for the startup stage while DC voltages is raised from 100 V to 105 V, where (a) is for the case of initial delay, (b) for the deliberate 5° delay besides the initial one and (c) for the waveforms after phase synchronization. One can see that the phase regulations were finished within a short time (i.e., less than 0.3 s). Fig. 9(a) and (b) shows good agreements with simulated results by Simulink shown in Fig. 5(a) and (b), respectively.

(e)
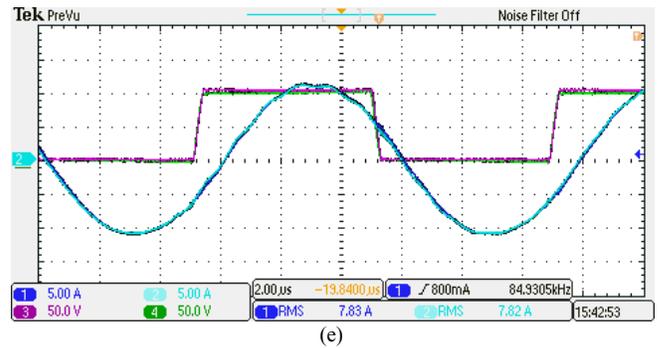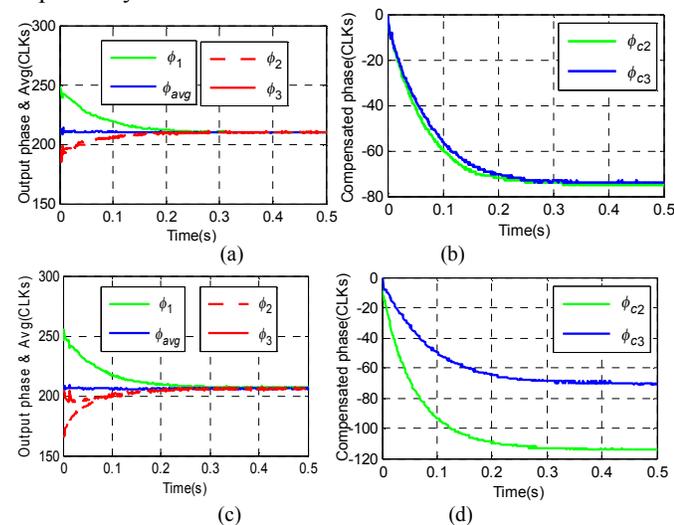
Fig. 9 Measured regulation process and result of the phase synchronization for the startup stage. (a) and (b) are the output phases and compensation for the initial delay case, while (c) and (d) for the a deliberate 5° (namely, 33 CLKs) delay besides the initial one, respectively. (e) Output voltages and currents of master inverter and one of slave inverters after synchronization. Note that all phases and delay compensation are under CLKs unit, whose values are about 6.5 times of those under the degree unit under 85 kHz.

After the phase synchronization, the input voltage for all inverters are regulated to 700 V, which leads to an input DC current of 53.3 A. The output voltages and currents of the master inverter and one slave inverter were captured and shown in Fig. 10. One can see that these plots show good agreement between both the amplitudes and the phases of voltages and currents. The measured voltage at the 10.5 Ω resistance load is 607 V, which means a received power of 35.1 kW. The measured DC-DC efficiency was 94% which is defined by the power consumed in the load resistance divided by that outputted from the DC voltage modules.
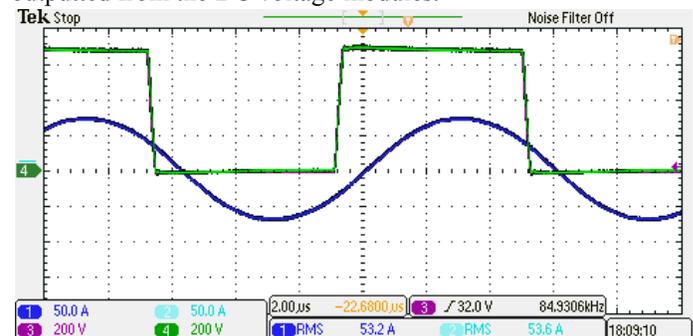
Fig. 10. Output voltages and currents of inverters with 700 V input DC voltage

Practically, the loss at the primary side can be evaluated based on the measured current, impedance angles and parameters listed in Tab. II [21] by

$$P_{lossP} = P_{toff} + P_{rDS} + P_{r\_ICT\_I} + P_{r\_ICT\_O} + P_{rLP} + P_{rCP} \quad (23)$$

where P_{toff}, and P_{rDS} are losses in all MOSFETs due to turn-off and on-state resistance, $P_{r\_ICT\_I}$, and $P_{r\_ICT\_O}$ are losses in inner ICTs and outer ICTs due to parasitic resistance, P_{rLP} and P_{rCP} are losses in the resonant inductor and the capacitor at the primary side, respectively. These losses can be calculated by[21]

(a)

(b)

(c)

(d)

$$P_{toff} = \frac{\omega(t_r/3 + t_f/2)V_I i_O \sin\theta}{2\pi}$$

$$P_{rDS} = 6(i_O/12)^2 r_{DS}$$

$$P_{r\_ICT\_I} = 12(i_O/12)^2 r_{ICT\_I}$$

$$P_{r\_ICT\_O} = 3(i_O/3)^2 r_{ICT\_O} \qquad . \qquad (24)$$

$$P_{rLP} = i_O^2 r_{LP}/2$$

$$P_{rCP} = i_O^2 r_{CP}/2$$

In terms of the receiving side, its total loss is

$$P_{lossS} = P_{VF} + P_{CF} + P_{rLS} + P_{rCS} \quad , \qquad (25)$$

where P_{VF}, P_{CF}, P_{rLS} and P_{rCS} are the losses in the rectifier, the filter capacitor , the resonant inductor and the resonant capacitor which can be calculated respectively by

$$P_{VF} = \sqrt{2}V_F i_S$$

$$P_{CF} = \frac{i_S^2 r_{CF}}{2}(\frac{\pi^2}{8} - 1) \qquad . \qquad (26)$$

$$P_{rLS} = i_S^2 r_{LS}/2$$

$$P_{rCS} = i_S^2 r_{CS}/2$$

TABLE III
EVALUATED LOSSES IN VARIOUS COMPONENTS

symbol	Losses due to	value	Accounting for
P_{rLP}	loss in the resonant inductor at the primary side	437.66 W	31.64%
$P_{r\_ICT\_O}$	losses in all outer ICTs due to parasitic resistance	259.95 W	18.79%
P_{VF}	loss in the rectifier due to forward voltage drop	239.19 w	17.29%
P_{toff}	losses in all MOSFETs due to turn-off	107.51 W	7.77%
P_{rLS}	loss in the resonant inductor at the secondary side	102.25 W	7.39%
$P_{r\_ICT\_I}$	losses in all inner ICTs due to parasitic resistance	99.47 W	7.19%
P_{rDS}	loss in all MOSFETs due to on-state resistance	41.45 W	3.00%
P_{CF}	Loss in the resonant capacitor at the sending side	48.01 W	3.47%
P_{rCP}	loss in the filter capacitor at the primary side	39.78 W	2.88%
P_{rCS}	loss in the resonant capacitor at the secondary side	8.18 W	0.59%

The measured overall output current amplitude at the primary side is $i_O = 199.5$ A, impedance angle that the current lags behind the voltage of the inverter is $\theta = 35.8°$, the current amplitude at the secondary side is $i_S = 91.2$ A and the current RMS through the 10.5 Ω load resistance is $I_{load} = 57.8$ A, respectively. As a result, losses in various components can be obtained based on these measured values and parameters listed in Tab. II (assuming $r_{ICT\_I} = 30$ mΩ and $r_{ICT\_O} = 19.6$ mΩ, respectively). The loss break down calculated by (23) through (26) is listed in Tab.III. The total loss is 1.39 kW which accounts for about 4% of the overall power. There is about 2% difference between the measured 94% overall efficiency.

Considering the ignored core loss in ICT windings and measuring errors of the currents, voltages and impedance angles, the evaluated loss breakdown is reasonable. Besides, one can see that loss in resonant inductor at the primary side accounts for the highest percentage, which means that a proper designed inductor with a lower parasitic resistance is the future direction to achieve higher efficiency.

E. Experiment for Phase Synchronization with Variable Operating Frequency

Assuming the time delay of the signal pathway is constant, the delay expressed by phase angle varies with the operating frequency. Additionally, the frequency variation leads to a different final output phase for all inverter after synchronization. Considering the inductive loads for most IPT applications, the output phase and compensation will increase with the operating frequency. When the frequency is increased from 85 kHz to 88 kHz (namely, increase by 3.53%), the compensated CLKs will also increase by 3.53% in theory. In short, the compensated CLKs have to be regulated according to the frequency dynamically. Fig. 11 illustrates the phase regulation process, where the frequency increases from 85 kHz to 88 kHz. The final measured compensated CLKs are $\phi_{c2} = -78$ and $\phi_{c3} = -77$, respectively, which is about 3.53% increase compared with the original compensated ones, namely -75 and -74, respectively. As a result, the output phases arrive at a stable status within a few ms because a small compensation change is needed. The output voltages and currents after synchronization with the frequency change are not presented because they are almost the same with those in Fig. 9(e), except the output phases and magnitudes.
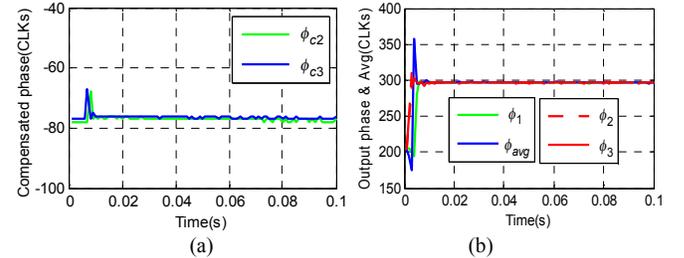
Fig. 11. Measured regulation process under frequency varying from 85 kHz to 88 kHz. (a) Output phases. (b)Compensated CLKs of slave inverters.

F. Experiment for Phase Synchronization with Variable Load

Load variation is another possible disturbance besides frequency change. Fig. 12 depicts the regulation process when the load varies from 10 Ω to 15 Ω. The measured compensated CLKs after synchronization were the same as those before load change, namely, $\phi_{c2} = -75$ and $\phi_{c3} = -74$. This is because the operating frequency remains constant, which requires constant compensated CLKs regardless of the load. Additionally, there is an unexpected sharp increase at the beginning of the regulation process in terms of the compensated CLKs. This is attributed to the communication delay of CAN, which imposes an older average output phase to the PI controller. As a result, a wrong error between the average and the measured output

phase leads to an unexpected sharp increase of the compensated CLKs.

In order to avoid the violent fluctuations of the output phases, the compensation regulation can be suspended for a few ms when a sharp change of output phase is detected. Fig. 12(c) and (d) depicts the results with suspended compensation, respectively. One can see that smaller fluctuations are obtained. The suspended action isn't applied to the case of frequency change. Practically, the controller can detect the frequency change immediately from the input driver pulse signal.
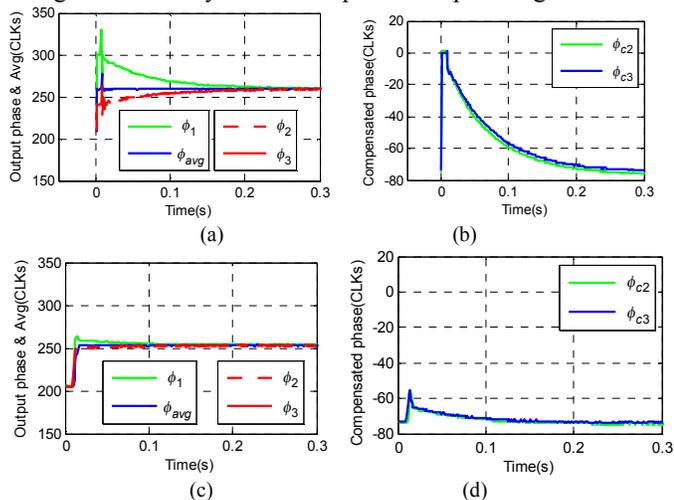
Fig. 12. Phase regulation process under load varying from $10\,\Omega$ to $15\,\Omega$. (a) and (b) are output phases and corresponding compensated CLKs of slave inverters with immediate compensating while (c) and (d) with a regulation suspend of 5 ms after a sharp change of output phase is detected.

VI. CONCLUSIONS

The paper has proposed a novel parallel multi-inverter system with modular inverter for high power IPT applications. Different numbers of slave units can be selected according to the required level of the output current and power, which provides great flexibility for IPT systems with different power requirements. The proposed inverter has good suppression capability for the outer-modular circulating current. A PI controller has been designed, built, and tested to synchronize the output voltages of inverters. Some other significant conclusions can be drawn as follows.

1) Each modular inverter in the parallel multi-inverter system has the same hardware configuration; hence it can operate independently or in parallel multi-inverter schemes, which results in high modularity.

2) For a proper magnetizing inductance L_M, the deviation between the output phase of an inverter and the average phase value of all inverters reflects the phase status of the inverter output voltage. If the output phase is lower than the average of all output phases, the output voltage necessarily lags behind the others, and *vice versa*. This approach provides a possibility for synchronization regulation of the output voltage based on the error between the output phase and the phase average value of all inverters.

3) The required magnetizing inductance L_M increases with the number of parallel inverters in order to correctly

reflect the phase status of the inverter output voltage via inverter output phase.

4) For the proposed main-slave phase synchronization control scheme, the paralleled inverters can achieve phase synchronization with the proposed PI controllers in a short time interval even under disturbances of frequency variation or load change.

REFERENCES

[1] J. Kim, B. Lee, J. Lee, S. Lee, C. Park, S. Jung, S. Lee, K. Yi, and J. Baek, "Development of 1MW inductive powertTransfer system for a high speed train, " *IEEE Trans. Ind. Electron.*, vol. 62, no. 10, pp. 6242–6250, Oct. 2015.

[2] R. Bosshard and J. W. Kolar, "Multi-objective optimization of 50 kW 85 kHz IPT system for public transport," *IEEE J. Emerging Sel. Topics Power Electron.*, vol. 4, no. 4, pp. 1370–1382, Dec. 2016

[3] J. Shin et al., "Design and implementation of shaped magnetic-resonance based wireless power transfer system for roadway-powered moving electric vehicles," *IEEE Trans. Ind. Electron.*, vol. 61, no. 3, pp. 1179–1192, Mar. 2014.

[4] Q. Deng, J. Liu, D. Czarkowski, M. Bojarski, E. Asa, and F. D. Leon, ``Design of a wireless charging system with a phase-controlled inverter for electric vehicles under varying parameters", *IET Power Electron.*, vol. 9, no. 13, pp. 2461 – 2470, Oct. 2016.

[5] R. Bosshard and J. W. Kolar, "All-SiC 9.5 kW/dm 3 on-board power electronics for 50 kW/85 kHz automotive IPT system," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 1, pp. 419-431, Mar. 2017.

[6] J. M. Miller, A. Daga "Elements of wireless power transfer essential to high power charging of heavy duty vehicles," *IEEE Trans. Transp. Electrif.*, vol. 1, no. 1, pp. 26-39, Jun. 2015.

[7] B. X. Nguyen, W. Peng, and D. M. Vilathgamuwa,"Multilevel converter topologies based high power inductive power transfer systems, "*in Proc. IEEE Int. Conf. Sustainable Energy Technologies (ICSET)*, Nov. 2016, pp. 264–269.

[8] H. R. Rahnamae, D. J. Thrimawithana, and U. K. Madawala, "MOSFET based Multilevel converter for IPT systems," *in Proc. IEEE Int. Conf. Ind. Technol.*, Feb. 2014, pp. 295–300.

[9] W. Chen, X. Jiang, W. Cao, et.al., "A fully modular control strategy for input-series output-parallel (ISOP) inverter system based on positive output-voltage-amplitude gradient," *IEEE Trans. Power Electron.*, vol. 33, no.4, pp. 2878-2887, Apr. 2018.

[10] T. Fang, L. Shen, W. He, and X. Ruan, "Distributed control and redundant technique to achieve superior reliability for fully modular input-series-output-parallel inverter system," *IEEE Trans. Power Electron.*, vol. 32, no.1, pp. 723-735, Jan.2017

[11] D. Sha, G. Xu, and X. Liao, "Control strategy for input-series-output-series high-frequency AC-link inverters," *IEEE Trans. Power Electron.*, vol. 28, no.11, pp. 5283-5292, Nov. 2007.

[12] Y. Chen, J. M Guerrero, Z. Shuai, et al. "Fast reactive power sharing, circulating current and resonance suppression for parallel inverters using resistive-capacitive output impedance," *IEEE Trans. Power Electron.*, vol. 31, no. 8, pp. 5524-5537, AUG. 2016.

[13] Z. Chen, X. Pei, M. Yang, *et al.* "An adaptive virtual resistor (AVR) control strategy for low-voltage parallel inverters," *IEEE Trans. Power Electron.,* (to be published).

[14] Y. Shi, W. Wu, H. Wang, Y. Du, J Su. "The parallel multi-inverter system based on the voltage-type droop control method," *IEEE J. Emerging Sel. Topics Power Electron.*, vol. 4, no. 4, pp. 1332-1341, Dec. 2016.

[15] X. Zhang, W. Li, Y. Xiao, *et al.* "Analysis and suppression of circulating current caused by carrier phase difference in parallel voltage source inverters with SVPWM," *IEEE Trans. Power Electron.,* (to be published).

[16] X. Wei, G. Zhu, J. Lu, X. Xu. "Instantaneous current-sharing control scheme of multi-inverter modules in parallel based on virtual circulating impedance," *IET Power Electron.*, vol. 9, no. 5, pp. 960-968, Oct. 2016.

[17] T. F. Wu, Y. E. Wu, H. M. Hsieh, and Y. K. Chen, "Current weighting distribution control strategy for multi-inverter systems to achieve current

sharing," *IEEE Trans. Power Electron.*, vol. 22, no.1, pp.160-168, Jan. 2007

[18] X Sun, L. K Wong, Y. S Lee, and D Xu, "Design and analysis of an optimal controller for parallel multi-inverter systems," *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol.53, no. 1, pp. 56-61, Jan. 2006.

[19] Y. Li, R. Mai, L. Lu, and Z. He, "Active and reactive currents decomposition based control of angle and magnitude of current for a parallel muti-inverter IPT system," *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 1602–1614, Feb. 2017.

[20] H. Hao, G. Covic, and J. Boys, "A parallel topology for inductive power transfer power supplies," *IEEE Trans. Power Electron.,* vol. 29, no. 3, pp. 1140–1151, Mar. 2014.

[21] Q. Deng, J. Liu, D. Czarkowski, *et al*., "An inductive power transfer system supplied by a multiphase parallel inverter*," IEEE Trans. Ind. Electron.,* vol. 64, no. 9, pp. 7039–7048, May 2017.

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