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A study of zero-if double-balanced mixer for wimax receivers

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ABSTRACT

Differential approach is becoming highly preferred in radio frequency integrated circuit (RFIC) design due to its advantages, particularly its high immunity to common-mode noises, satisfactory rejection of parasitic coupling, and increased dynamic range. One particular RF front-end building block that is often designed as differential circuit is the mixer. This paper presents a study and design of a differential mixer, particularly the double-balanced mixer implemented on a zero-IF (zero-intermediate frequency) or direct-conversion architecture in a standard 90 nm complementary metal-oxide semiconductor (CMOS) process operating at frequency of 5 GHz, which is a typical frequency for worldwide interoperability for microwave access (WiMAX) receiver. Impedance matching was necessary to fully optimize the mixer design. The zero-IF double-balanced mixer design achieved conversion gain of 11.46 dB and noise figure of 16.53 dB, comparable to other mixer designs.

1. Introduction

Receiver front-end of a radio frequency (RF) system is of particular interest to many integrated circuit (IC) designers and researchers as it proves to be the most critical part in many communication systems and wireless applications such as wireless fidelity (WiFi), bluetooth, long-term evolution (LTE), and worldwide interoperability for microwave access (WiMAX). The block diagram of a typical receiver is shown in Fig. 1.

Mixer is one of the key front-end building blocks in an RF receiver. It is also called a converter because it converts RF signals into a lower intermediate frequency (IF) by mixing with an offset local oscillator (LO). Depending on the receiver requirements, mixers must undergo a careful design process since a lot of tradeoffs among different performance parameters must be considered and understood. Ultimately, the objective is to study and design a zero-IF double-balanced mixer implemented in a standard 90 nm complementary metal-oxide semiconductor (CMOS) process. Operating frequency is set to 5 GHz, which is a typical frequency for a WiMAX receiver.

2. Background

RF receivers can be categorized as superheterodyne (high-IF), low-IF, and zero-IF or homodyne or direct-conversion based on the resulting IF signal they operate. For the zero-IF receiver, IF is designed to be centered at frequency zero, meaning the LO frequency is equal to the input RF frequency. Image signal is avoided and the analog filtering problem can be easily handled. With zero IF, the desired signal is translated directly to the baseband, allowing analog-to-digital converter (ADC) and digital signal processing (DSP) circuits to perform modulation and other ancillary functions [1, 2]. This eliminates the need for highly complex filters since channel selection only requires a low-pass filter (LPF) as shown in Fig. 2 with sharp cutoff characteristics, and thus allowing the possibility of monolithic integration. With this, smaller and cheaper receivers with low power consumption may be realized for various wireless applications like Bluetooth, WiFi, and WiMAX. Many of the implemented receivers in WiMAX [3, 4, 5] use the zero-IF architecture since the LPFs make sure that the closely-spaced carrier signals do not cause interference with each other.

Designing a mixer must take into account the many trade-offs among the performance parameters. Thus, a careful study of these important parameters must be done in order to design fully-functional mixers. A mixer's efficiency on frequency conversion from RF to IF is characterized by conversion loss or gain. It is the ratio of the desired IF output to the value of the RF input. Conversion gain (*CG*) may be expressed in voltage or power. In cases when the conversion gain is less than unity or 0 dB, it is aptly termed as a conversion loss.

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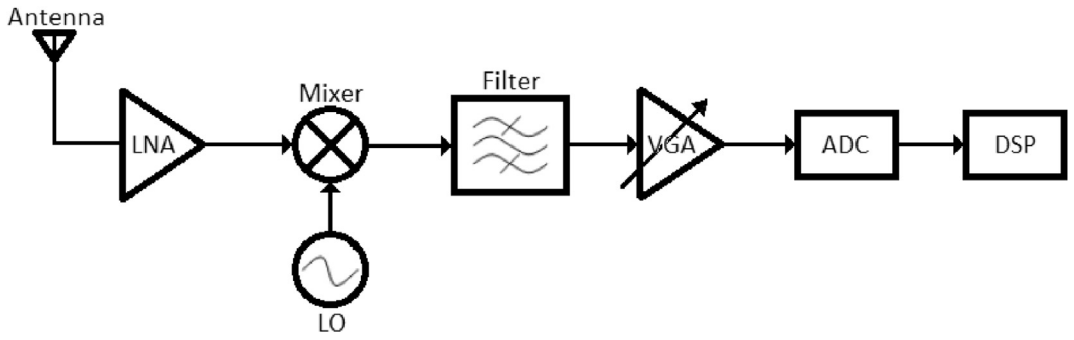

Fig. 1. Block diagram of a typical receiver.

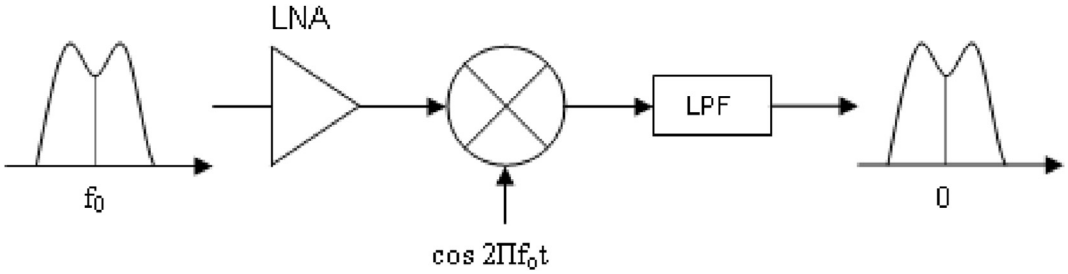

Fig. 2. Zero-IF receiver.

$$CG_{\text{voltage}} = 20\log\frac{V_{IF}}{V_{RF}} \quad (1)$$

$$CG_{\text{power}} = 10\log\frac{P_{IF}}{P_{RF}} \quad (2)$$

V_{IF} and V_{RF} are the root mean square (RMS) voltages of the IF and RF signals, respectively, while P_{IF} and P_{RF} are the equivalent power of the IF and RF signals, respectively. Conversion gain is preferred over conversion loss because of the benefit of amplification along with frequency translation. However, it should be noted that conversion gain directly affects the noise figure and linearity of the overall receiver. Hence, design tradeoffs concerning these parameters are inevitable.

Another important mixer parameter is the noise figure (*NF*). It is a measure of the amount of signal-to-noise-ratio (*SNR*) degradation introduced by the mixer as seen at the output. Eq. (3) shows the relation between the *SNR* at the input port and the *SNR* at the output port of the mixer, often expressed in dB.

$$NF = 10\log\left(\frac{SNR_{\text{IN}}}{SNR_{\text{OUT}}}\right) \quad (3)$$

Noise figures of mixers tend to be higher than amplifiers (e.g. low-noise amplifiers, power amplifiers) because of the contribution of noise from other frequencies (apart from input RF signal) that can mix down to the IF. This considerable noise in mixers is the main reason why low-noise amplifiers (LNA) are used in the front-end of a receiver [6].

The selection of mixer architecture depends on the application and the requirements for the different design parameters. The dynamic range of most RF receivers is often limited by the first down-conversion mixer. This leads to many tradeoffs among the performance parameters such as conversion gain, noise figure, linearity and isolation. Integrated mixers are preferred over their discrete counterparts because they can offer high level integration with cost, area, and power savings [7].

Nowadays, the most popular solution for the mixer is based on the double-balanced topology. It operates with differential LO and RF inputs. In this topology, LO products are prevented from getting to the output by combining two single-balanced mixers. As shown in Fig. 3, the two single-balanced mixers are connected in anti-parallel as far as the LO is concerned, but in parallel for the RF signal. Thus, the LO terms sum to zero in the output, whereas the converted RF signal is doubled in the output [6]. This is most desirable for high port-to-port isolation and spurious output rejection applications.

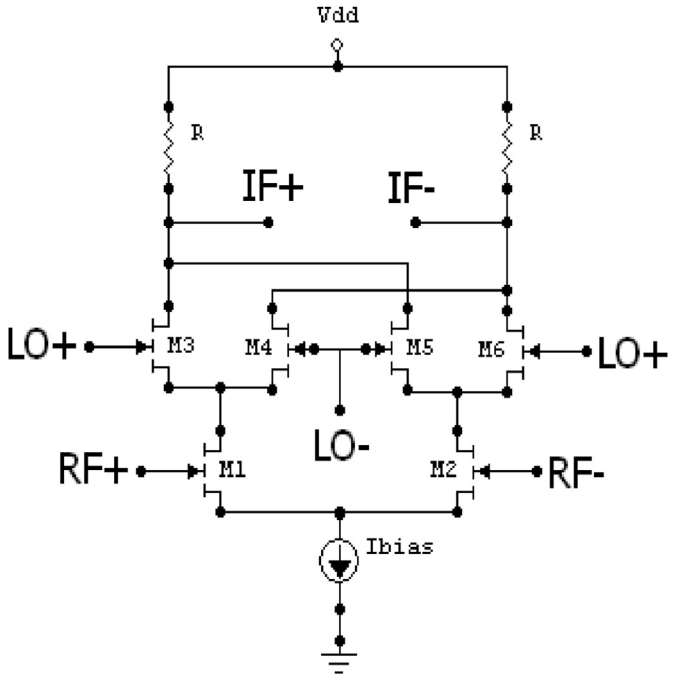

Fig. 3. Double-balanced mixer.

As earlier mentioned, the goal of the paper is to study and design a zero-IF double-balanced mixer implemented in a standard 90 nm CMOS process, operating at frequency of 5 GHz which is a typical frequency for a WiMAX receiver. The target specifications of the figures of merit or the critical parameters are based on the performance comparison in terms of conversion gain and noise figure of past researches on direct-conversion

active mixer topologies given in Table 1.

3. Methodology

The topology of double-balanced mixer can provide high conversion gain, very low noise figure, and high degree of LO-IF isolation. The main disadvantage of this topology is its physical implementation. A balun transformer is required to convert the single-ended input to a differential RF input signal of the mixer. Transformers with very low insertion loss are difficult to realize in monolithic integration, hence this forces the use of an off-chip transformer which occupies more board space and cost [11].

It is of high importance to determine the proper biasing and sizing of all the transistors such that RF transistors (M1-M2) will operate in the saturation region while the LO transistors (M3-M6) operate near the boundary of the saturation and linear regions. The mixer design used *nsvt* (NMOS standard Vt) which is the typical model for the transistor. Shown in Fig. 4 is the schematic design of the double-balanced mixer.

One way to increase the performance of the mixer in terms of conversion gain and noise figure is to apply impedance matching in the circuit. Z_{11} and Z_{22} can be obtained using *sp*-analysis (s-parameter analysis) which is swept from $f_1 = 700$ MHz to $f_2 = 6$ GHz. Actual inductor and capacitor values at frequency of 5 GHz can be computed from the L-network reactances.

To supply differential LO input to the mixer, a port *PORT*2 with a matching resistor (set to 50Ω) is used which is then fed into an ideal passive balun to convert the single-ended signal into differential. For the differential RF input of the mixer, same setup as the LO is used with *PORT*1. To use the differential output for measurements, matching the IF output port *PORT*3 to the output impedance of the mixer is necessary. *PORT*1 is set to DC source type with *pacmag* (*periodic ac magnitude*) set to 1. *PORT*3, which is the IF port, is set also to DC source type. The only large signal is from *PORT*2 which is a sine wave with $f_{LO} = 5$ GHz and $P_{LO} = 0$ dBm.

For the impedance matching, the input matching network is applied before the differential RF input of the mixer instead of placing it before the balun. This will result to an adjustment on the value of L_1, which will decrease, since the balun circuit has self-inductance. The adjusted value of L_1 can be determined using the *sp*-analysis swept from $f_1 = 700$ MHz to $f_2 = 6$ GHz. Moreover, inductors with small inductances are more realizable in actual designs than their larger counterparts. The final values of the L-matching network are summarized in Table 2.

Software design tools *ASITIC* (analysis and simulation of spiral inductors and transformers for ICs) [12, 13] *and SpiralCalc* (integrated spiral inductor calculator) [14, 15] are used for the design of the inductors. Table 3 shows the design parameters obtained for the design of the spiral inductors using *ASITIC* while Table 4 shows that of using *SpiralCalc*.

In *ASITIC*, the spiral inductors are designed such that desired inductances are achieved and the Q-factors are optimized with eddy-current option enabled to include the effects of substrate induced eddy current losses. L_1 have smaller Q-factor than L_2 because of its high inductance value. For the inductor design using *SpiralCalc*, same parameter values from the *ASITIC* parameters are used except for the metal width and the number of turns of the spiral inductor. These parameters are tweaked such that the desired inductances are achieved for the inductors.

The *n2port* from the *analogLib* library is used as a model block for all the *ASITIC* inductors. *Touchstone* format of S-parameter file is used as file input of the n2port component since the actual S-parameters using *ASITIC* are given in *touchstone* format. The figures of merit such as

Table 1
Performance comparison.

Paper	RF (GHz)	Conversion Gain (dB)	Noise Figure (dB)	Topology
[4]	2–11	21.5–22.8	21.5–25.8	Double-balanced
[5]	3.4–3.85	10	10	Single-balanced
[8]	2	19.5	10.2	BiCMOS Double-balanced
[9]	20–40	16	–	BiCMOS Single-balanced
[10]	5.2	9.3	10.5	Double-balanced

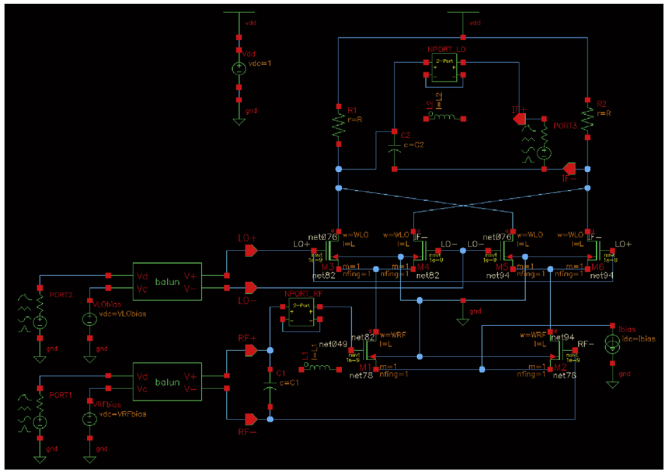

Fig. 4. Schematic design of double-balanced mixer.

Table 2
Final values of L-Network elements.

L and *C*	Value
L_1	12.70 nH
C_1	1.12 pF
L_2	1.33 nH
C_2	267.13 fF

Table 3
Inductor design using ASITIC.

Parameters	Inductors	
	L_1	L_2
Desired L	12.7 nH	1.328515 nH
No. of sides	4	8
Length, D	300 μm	190 μm
Metal width, W	10.886 μm	10.901775 μm
Spacing, S	1	1
No. of turns, N	4.25	2.5
Metal layer	7	7
Inductance, L	12.711454 nH	1.328515 nH
Q-factor, Q	2.32165	5.693986

Table 4
Inductor design using SpiralCalc.

Parameters	Inductors	
	L_1	L_2
Desired L	12.7 nH	1.33 nH
No. of sides	4	8
Length, D	300 μm	190 μm
Metal width, W	11.2 μm	10 μm
Spacing, S	1	1
No. of turns, N	6	2
Inductance, L:		
Modified Wheeler	12.885 μm	1.326 μm
Current Sheet	12.739 μm	1.326 μm
Monomial Fit	12.624 μm	1.394 μm

conversion gain and noise figure are determined using *SpectreRF* [16] in the *Analog Design Environment* of Cadence Virtuoso [17] software.

Complex tradeoffs among technology specifications and design parameters exist and should be carefully handled when designing an inductor, to optimize the quality and its performance. It is worth noting that inductors may shift to capacitor operation at frequencies above resonance. Thus, it is crucial that inductors be designed for their effective frequency range of operation, satisfying the requirements of the end-product application [18].

4. Results and discussion

A double-balanced mixer's frequency converting action is characterized by conversion gain or loss. Voltage conversion gain is the ratio of the RMS voltages of the IF and RF signals. The formulae for conversion gain are also given in Eq. (1). The variations of conversion gain with the power of LO signal (P_{LO}) can be measured using *swept PSS (periodic steady-state) analysis* with *PAC (periodic AC) analysis*. The *PAC analysis* will then compute the voltage conversion gain in dB20 of the whole circuit with *PORT*3 as the output port (with output harmonic of 0, which is 5 GHz) and *PORT*1 as the input port (with input harmonic of −1, which is 0 GHz). Setting the input port to RF + port, which is located after the balun circuit, will compute the voltage conversion gain of the mixer only. Simulation plots of the conversion gain swept from $P_{LO} = -10$ dBm to $P_{LO} = 30$ dBm are shown in Figs. 5, 6, and 7.

Based on the conversion gain simulation results, input and output impedance matching contribute to better conversion gain performance. Moreover, using ideal inductors for impedance matching produced better performance as compared to using non-ideal ASITIC inductors through the n2port. It can be observed from the simulation plots that the conversion gain of the mixer only is higher than the conversion gain of the whole circuit consisting of the mixer and the balun. This is because the balun in the circuit, which is a passive balun, has insertion loss and thus incapable of producing gain. When a passive balun is cascaded with another block, the overall gain is degraded.

For the noise figure, *Pnoise* (*periodic noise*) *analysis* with *PSS analysis* is used. In addition, *PSP* (*periodic S-parameters*) *analysis* with *PSS analysis* can also be used to determine the noise figure of the circuit. Noise figure from a sweep range of −10 dBm to 30 dBm can now be determined and plotted using these analyses. The plots are shown in Figs. 8 and 9.

Input and output impedance matching also contribute to better noise performance of the circuit, as indicated in Figs. 8 and 9. It can be observed that using ideal inductors for impedance matching produced lower noise figure as compared to using non-ideal ASITIC inductors through the n2port model. The model block n2port introduces noise to the system, hence, adding to the total noise figure of the circuit. Table 5 shows a summary of simulation results for conversion gain and noise figure at $P_{LO} = 0$ dBm.

It is evident that input and output impedance matching contribute to better performance based on the figures of merit presented for the double-balanced mixer design. It is observed that the conversion gain of the zero-IF double-balanced mixer is higher than the conversion gain of the circuit consisting of the mixer and the balun. The reason is that the conversion gain performance at the system-level perspective is greatly influenced by the performance of the initial or preceding blocks, for this case the passive balun. Henceforth, it is of high importance to consider the contribution of the input or previous circuit (and as well as the output or succeeding circuit) in studying and designing the mixer.

5. Conclusions

A design of zero-IF double-balanced mixer was implemented and optimized on this study. Proper biasing and sizing of all the transistors were necessary to ensure the required mode of operation for all the transistors. Conversion gain and noise figure were determined to measure the mixer's performance. These performance parameters can be greatly enhanced by applying impedance matching in the circuit. The effect of the passive balun was also presented, showing the decrease in the conversion gain of the overall circuit. Ultimately, the zero-IF double-balance mixer design achieved conversion gain of 11.46 dB and noise figure of 16.53 dB (using Pnoise analysis) at 5 GHz, comparable to other mixer designs from past researches.

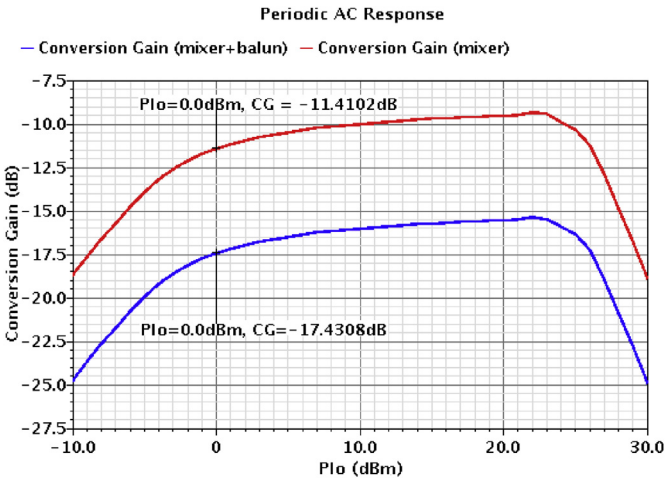

Fig. 5. Conversion gain (in dB) vs. P_{LO} of Design2 (w/o matching).

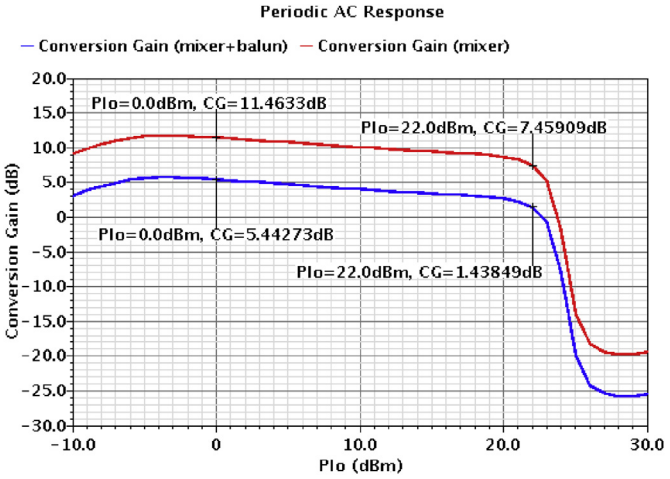

Fig. 6. Conversion gain (in dB) vs. P_{LO} of Design2 (ideal L).

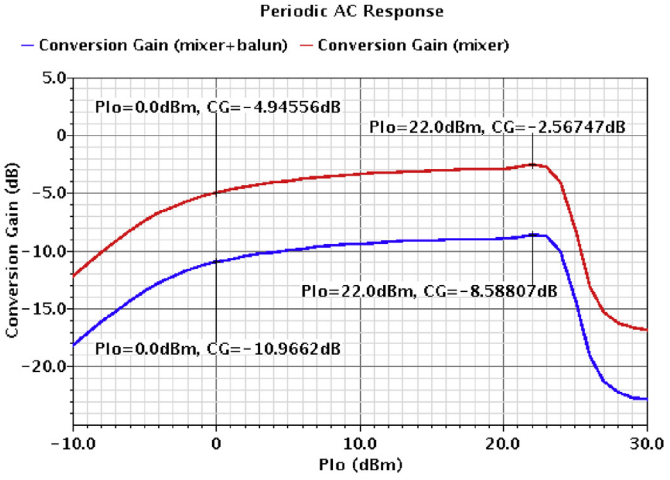

Fig. 7. Conversion gain (in dB) vs. P_{LO} of Design2 (*ASITIC* L).

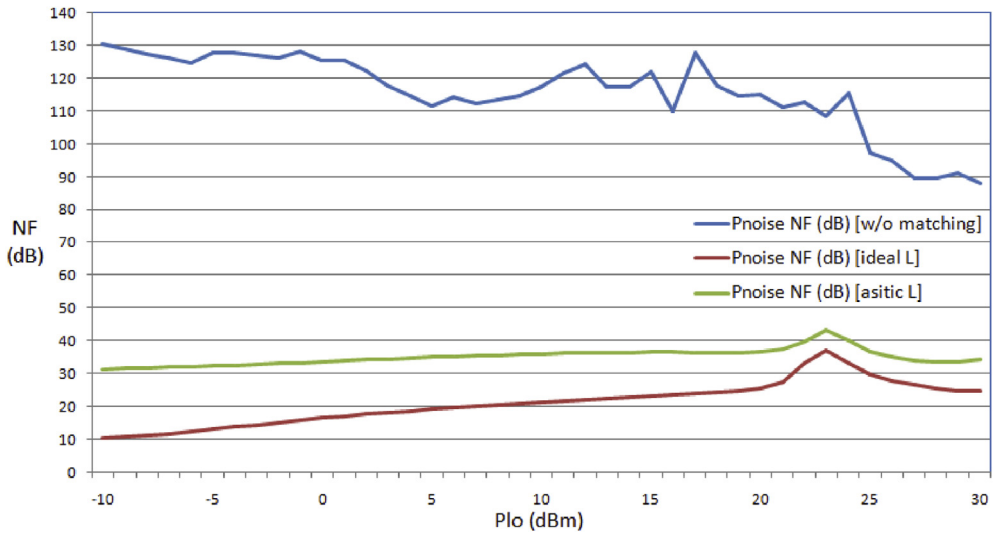

Fig. 8. Noise figure (in dB) vs. P_{LO} of Design2 (*Pnoise analysis*).

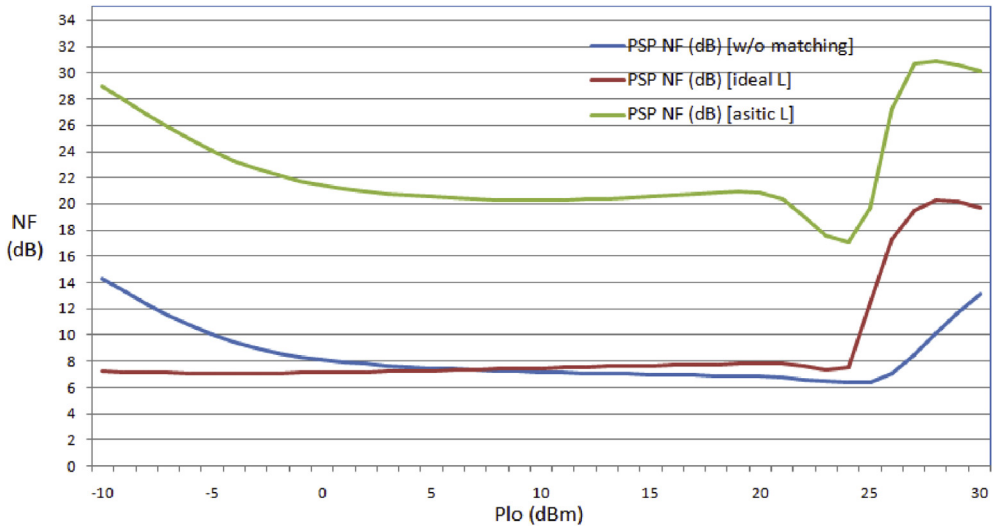

Fig. 9. Noise figure (in dB) vs. P_{LO} of Design2 (*PSP analysis*).

Table 5
Summary of simulation results (at PLO = 0).

Mixer Parameters	Value
CG (mixer + balun) [w/o matching]	−17.43 dB
CG (mixer) [w/o matching]	−11.41 dB
CG (mixer + balun) [ideal L]	5.44 dB
CG (mixer) [ideal L]	11.46 dB
CG (mixer + balun) [*ASITIC* L]	−10.97 dB
CG (mixer) [*ASITIC* L]	−4.95 dB
Pnoise NF [w/o matching]	125.36 dB
Pnoise NF [ideal L]	16.53 dB
Pnoise NF [*ASITIC* L]	33.71 dB
PSP NF [w/o matching]	8.13 dB
PSP NF [ideal L]	7.14 dB
PSP NF [ASITIC L]	21.44 dB

For future mixer studies, linearity could be further analyzed along with *CG* and *NF* parameters for complex tradeoffs, as done in [19, 20]. Moreover, active baluns [20, 21] could be used instead of passive baluns for monolithic design and implementation. Active baluns are capable of producing gain and if cascaded in a double-balanced mixer to supply the differential RF and LO inputs, the overall performance of the mixer can be improved. Although active baluns are unidirectional converters, they are also used for their large bandwidth, which is beyond what non-ideal passive baluns can provide.

Declarations

Author contribution statement

Frederick Ray I. Gomez: Conceived and designed the experiments; Performed the experiments; Analyzed and interpreted the data; Contributed reagents, materials, analysis tools or data; Wrote the paper.

Maria Theresa G. De Leon: Conceived and designed the experiments; Analyzed and interpreted the data; Contributed reagents, materials, analysis tools or data.

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Competing interest statement

The authors declare no conflict of interest.

Additional information

No additional information is available for this paper.

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References

[1] B. Razavi, RF Microelectronics, Prentice Hall Press, Upper Saddle River, New Jersey, USA, 1998.
[2] W. Namgoong, T. Meng, Direct-conversion RF receiver design, IEEE Trans. Commun. 49 (3) (March 2001).
[3] Y. Zhou, C.P. Yoong, L.S. Weng, Y.J. Khoi, M.C.Y. Wah, K.A.C. Moy, D.W.T. Fatt, A 5 GHz dual-mode WiMAX/WLAN direct-conversion receiver, in: IEEE International Symposium on Circuits and Systems, May 2006.
[4] J.Y. Lyu, Z.M. Lin, A 2~11 GHz direct-conversion mixer for WiMAX applications, in: TENCON 2007 – IEEE Region 10 Conference, pp. 1–4, October 2007.
[5] J.G. Atallah, S. Rodriguez, L.R. Zeng, M. Ismail, A direct conversion WiMAX RF receiver front-end in CMOS technology, in: International Symposium on Signals, Circuits and Systems, vol. 1, July 2007.
[6] T. Lee, The Design of CMOS Radio-Frequency Integrated Circuits, Cambridge University Press, Cambridge, 1998.
[7] G. Watanabe, H. Lau, J. Schoepf, Integrated Mixer Design, Motorola Inc., Semiconductor Products Sector, Arizona, USA, 2007.
[8] T. Tikka, J. Ryynanen, M. Hotti, K. Halonen, "Design of a high linearity mixer for direct-conversion base-station receiver," *in Proc*, in: IEEE International Symposium on Circuits and Systems, 2006.
[9] K.W. Hamed, A.P. Freundorfer, Y.M.M. Antar, A monolithic double-balanced direct conversion mixer with an integrated wideband passive balun, IEEE J. Solid State Circuits 40 (3) (March 2005).
[10] J. Park, C.-H. Lee, B.-S. Kim, J. Laskar, Design and analysis of low flicker-noise CMOS mixers for direct-conversion receivers, IEEE Trans. Microw. Theory Tech. 54 (12) (December 2006).
[11] M. Voltti, T. Koivisto, E. Tiiliharju, Comparison of active and passive mixers, in: 18th European Conference on Circuit Theory and Design, pp. 890–893, August 2007.
[12] A.M. Niknejad, R.G. Meyer, Analysis and optimization of monolithic inductors and transformers for RF ICs, in: Proc. Custom Integrated Circuits Conference, Santa Clara, CA, pp. 375–378, May 1997.
[13] A.M. Niknejad, R.G. Meyer, ASITIC for Windows NT/2000, Research in RFIC Design, 2000, http://rfic.eecs.berkeley.edu/~niknejad/Asitic/grackle/cygwin_info.html.
[14] Stanford Microwave Integrated Circuits Laboratory. Integrated Spiral Inductor Calculator, http://www-smirc.stanford.edu/spiralCalc.html.
[15] S.S. Mohan, M. Hershenson, S.P. Boyd, T.H. Lee, Simple accurate expressions for planar spiral inductances, IEEE J. Solid State Circuits, pp. 1419–1424 (October 1999).
[16] Cadence Design Systems, Inc., Mixer Design Using SpectreRF, Application Note, product version 5.0, June 2004.
[17] Cadence Design Systems, Inc. Custom IC/Analog/RF Design – Circuit Design. https://www.cadence.com/content/cadence-www/global/en_US/home/tools/custom-ic-analog-rf-design/circuit-design.html.
[18] F.R. Gomez, A fundamental approach for design and optimization of a spiral inductor, J. Electr. Eng. 6 (4) (September 2018) 256–260. David Publishing Co.
[19] D. Fu, L. Huang, H. Du, H. Yuan, A 0.18μm CMOS high linearity flat conversion gain down-conversion mixer for UWB receiver, in: 9th International Conference on Solid-State and Integrated-Circuit Technology, October 2008.
[20] P.Z. Rao, T.Y. Chang, C.P. Liang, S.J. Chung, An ultra-wideband high-linearity CMOS mixer with new wideband active baluns, IEEE Trans. Microw. Theory Tech. 57 (9) (September 2009), pp. 2184–2192.
[21] F.R. Gomez, M.T. De Leon, C.R. Roque, Active balun circuits for WiMAX receiver front-end, in: TENCON 2010 – IEEE Region 10 Conference, pp. 1156–1161, November 2010.