

Power quality improvement of a class of reduced device count inverter



Issam A. Smadi*, Saher Albatran, Mohammad A. Alsyouf

Department of Electrical Engineering, Faculty of Engineering, Jordan University of Science and Technology, Irbid, Jordan

ARTICLE INFO

Keywords:

Power quality
Harmonic mitigation
Pulsewidth modulation
Total harmonic distortion
Particle swarm optimization

ABSTRACT

This paper presents a method to improve the power quality of a class of shared inverter topologies utilizing optimal sorting and the offsetting pulsewidth modulation (PWM) method. For the $(3n+3)$ -switch converter topologies, a PWM procedure with two degrees of freedom is proposed to enhance the quality at the power side of the shared loads without adding more passive elements. Moreover, the two degrees of freedom are analyzed and optimized to improve the power quality of the output current of the shared loads. The optimization is achieved using particle swarm optimization (PSO) method in which three objective functions are formulated, each of which impacts the power quality at the shared load sides. The objective functions are: the total harmonic distortion (THD), the scaled total harmonic distortion (STHD), and the summation of the eleventh order of harmonics (SFEH) of the current of the shared loads. A case study that compares the PSO results with the conventional results is investigated to highlight the effectiveness of the proposed procedure. Furthermore, a test bed is built and the proposed procedure is experimentally investigated, verified, and compared to the simulation.

1. Introduction

Increasing the utilization of nonlinear loads in industry tools and household appliances that are driven by power electronics, and which produce harmonic currents, affects the power quality. Therefore, from a practical and industrial point of view, it is preferable to improve the quality of the power of the electrical load without increasing the cost, size, or complexity of the power electronics devices [1–3]. Harmonic mitigation can contribute in improving the power quality. Thus, many harmonic mitigation strategies have been proposed and implemented in the literature [4–7]. The main target of these studies was to maintain the total harmonic distortion (THD) of the phase current below a recommended level to avoid harmonic related problems. Although power quality improvement equipment such as passive filters [8], active filters [9], and hybrid filters [10,11] are commonly used to eliminate the harmonics, the use of such equipment may increase the size or cost of the system.

On the other hand, different modulation techniques can be used to mitigate the harmonics [4–6]. To meet the power quality standards for cascaded H-bridge converter with variable DC-link, the authors in [12] employed an optimal selective harmonic reduction pulsewidth modulation (PWM) technique. Moreover, to improve the performance of a cascaded H-bridge multilevel active rectifier, the authors in [13] proposed a current reference based selective harmonic reduction PWM technique to satisfy current harmonic limits by analyzing and designing switching frequency and coupling inductance. A non-selective harmonic compensation method is introduced in [14] for a grid connected voltage source inverter (VSI), adopting a slide mode current harmonic controller. Due to the utilization of the sliding mode control theory, a fast-dynamic response with good disturbance rejection was achieved. The

* Corresponding author.

E-mail address: iasmadi@just.edu.jo (I.A. Smadi).

<https://doi.org/10.1016/j.simpat.2019.101939>

Received 28 January 2019; Received in revised form 23 May 2019; Accepted 6 June 2019

Available online 07 June 2019

1569-190X/ © 2019 Elsevier B.V. All rights reserved.

work in [15] proposed modulation procedures to optimize the performance of the nine-switch converter in the cases of common frequency and variable frequency modes. To minimize the dominant harmonics around the switching frequency, the authors in [16] proposed a level shifting space vector pulse width modulation (SVPWM). The shift was linked to the modulation indices to optimize the converter performance. A phase and level shifting PWM have been compared in [17] for dual loads of adjustable speed drive and a static load. Based on critical operating point theory, the work in [18] proposed a phase shift method PWM to mitigate output current and voltage distortion problems.

The nine-switch converter is a subset of the generalized $(3n+3)$ -switch converter [19–21] when the number of connected loads “ n ” is 2. The generalized $(3n+3)$ switch converter is an example of a reduced device count power electronics converter that is capable of driving n -three phase loads independently. In this paper, an optimal two degrees of freedom PWM technique is proposed for the generalized $(3n+3)$ -switch converter. The aim is to enhance the quality at the power side of the connected loads as measured by three objective functions. The objective functions are: the THD, the scaled total harmonic distortion (STHD), and the summation of the first eleventh order of harmonics (SFEH) of the current of the shared loads. The presented generalized PWM has indexing as a first degree of freedom (DOF) and leveling as the second DOF. The first DOF is concerned with the physical location of the connected loads. When the loads are not identical, the load connection has a relation with the current harmonics. Therefore, in the design stage, this paper recommend where to optimally link the loads with the ports of the converter. The second DOF is optimized by employing the particle swarm optimization (PSO) method. PSO is one of the superior stochastic optimization methods, and it has been proven to be effective in countless optimization problems. For example, [23] employed PSO for harmonic minimization in multilevel inverters. The theory behind the PSO can be found in [24]. The primary results of the sorting and offsetting of the generalized $(3n+3)$ switch converter are presented in [22]. However, neither the dead time effect, nor the optimization procedure, nor the experimental validation have been discussed nor done. The main contribution of this paper is to propose an optimal two degrees of freedom sinusoidal and non-sinusoidal PWM for power quality enhancement of a generalized $(3n+3)$ switch converter, and to validate it experimentally.

The structure of this paper is as follows. The generalized $(3n+3)$ converter topology and operation are briefly reviewed in Section 2. Comprehensive mathematical formulation of the proposed two degrees of freedom PWM is presented in Section 3. Section 4 presents the simulation results. Section 5 presents discussion of the experimental validation of the proposed work. Finally, Section 6 concludes the paper.

2. Generalized $(3n+3)$ converter topology and operation

The power circuit of the generalized $(3n+3)$ -switch inverter driving n loads is shown in Fig. 1. When the number of the connected loads ‘ n ’ is equal to two, the converter matches the well-known nine-switch converter, and when ‘ n ’ is equal to three, the converter becomes a twelve switch converter, as shown in Fig. 2.

The converter has three legs with $(n+1)$ switch in each leg. Each leg must obey $\sum_{i=1}^{n+1} S_i^j = 1$ for $j = \{u \ v \ w\}$ to avoid shoot-through. The index i decides the physical connection of the load, i.e., the port where the load is connected to the converter, and S_i^j is the status of switch i in the leg j . In Fig. 1, load one is connected to port one, load two is connected to port two and so on. Although this arrangement is fixed, this paper will discuss the impact of the loads arrangement on harmonics mitigation and provide a method to select the optimal arrangement in the design stage. This will gain more benefits if the loads are not the same and/or the reference signal of the loads are not the same.

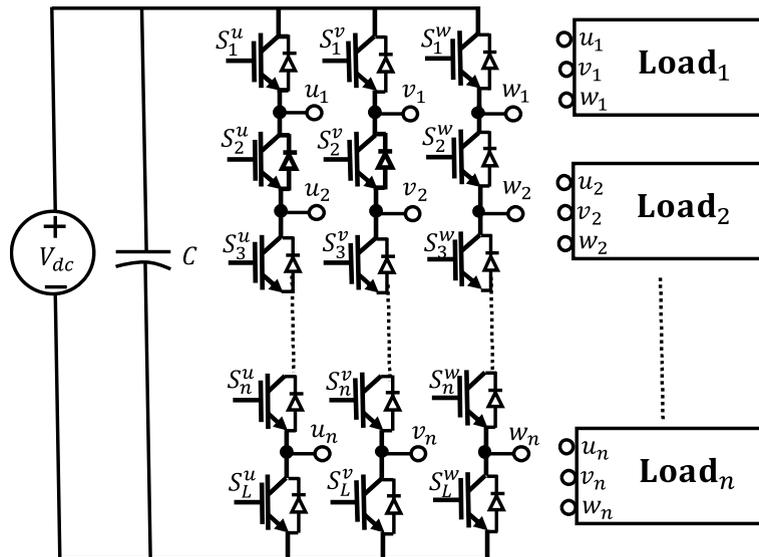


Fig. 1. The power circuit of the generalized $(3n+3)$ -switch inverter.

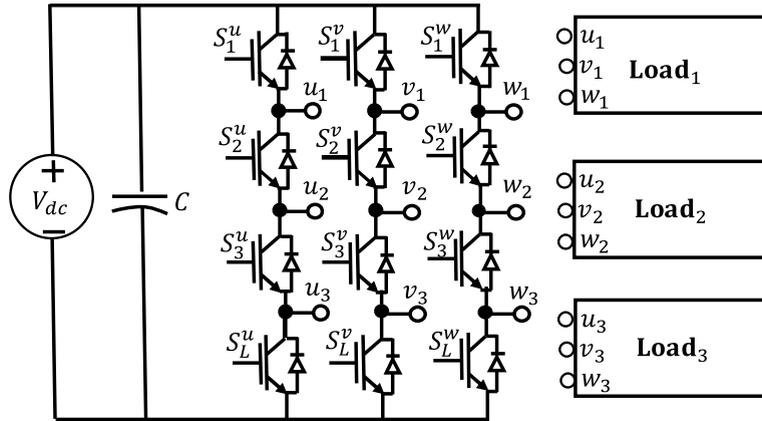


Fig. 2. The $(3n+3)$ -switch inverter when the number of connected loads is equal to 3.

As an example of the principle of operation of the generalized $(3n+3)$ -switch inverter and for n is equal to three, Figs. 3 to 5, shows the mode of operations and the independent load sharing. Fig. 3 depicts the case when only the first load is active, while Fig. 4 depicts the case when the second load is the only active load, and Fig. 5 depicts the case when the third load is the only active load.

3. Generalized sinusoidal and non-sinusoidal PWM method

Using the carrier signal to normalize all of the load voltage references, as shown in Figs. 6 and 7, the per-unit voltage references, for $i = \{1 \dots n\}$, of the connected loads can be written as:

$$\begin{bmatrix} v_{ui} \\ v_{vi} \\ v_{wi} \end{bmatrix} = m_i \begin{bmatrix} \sin(\omega_i t + \varphi_i) \\ \sin(\omega_i t - \frac{2\pi}{3} + \varphi_i) \\ \sin(\omega_i t + \frac{2\pi}{3} + \varphi_i) \end{bmatrix} \tag{1}$$

where m_i , ω_i , and φ_i are the initial modulation index, angular frequency, and the phase of the connected load, respectively. The term “initial” is introduced here as introductory to the inherit problem in the shared topologies. The solution of this case for both linear and overmodulation operation is discussed throughout this work.

Defining the maximum modulation index in the linear PWM region to be m_{max} which can be either 1.15 for non-sinusoidal PWM like zero-injected PWM, third harmonic injected pulse width modulation (THIPWM), and space vector pulse width modulation (SVPWM), or 1.0 for sinusoidal pulse width modulation (SPWM).

The total sum of the loads modulation indices will decide if the converter functions in the linear or overmodulation regions. Therefore, the dc-voltage utilization between the loads must be optimally distributed, especially if the overmodulation is not viable option. This will be done in this section.

Toward that end, the modulation indices are modified as follows: let the sum of the original modulation indices is $m_t = \sum_{i=1}^n m_i$, and define a logical operator γ as a representation of the linear ($\gamma = 1$) and the overmodulation region ($\gamma = 0$), respectively. That is:

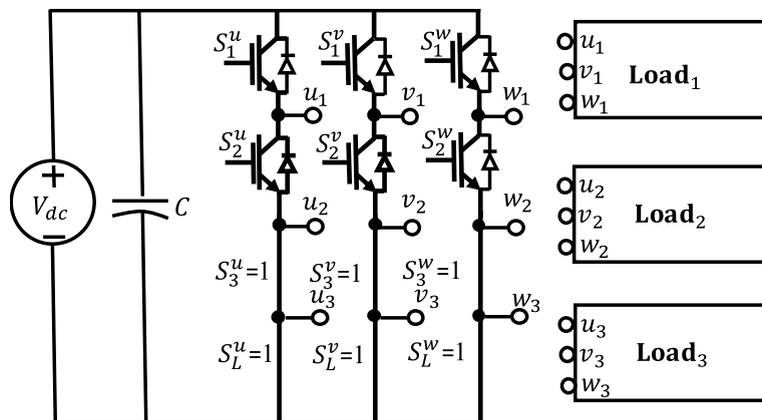


Fig. 3. Converter number one is active and converters number two and three are inactive.

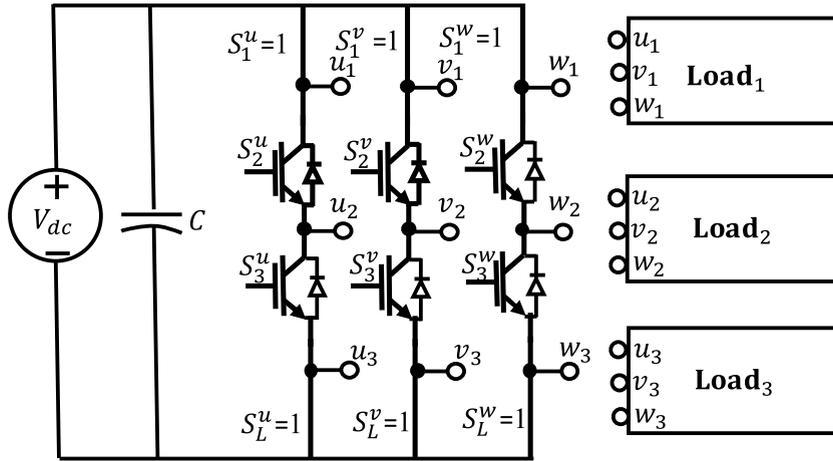


Fig. 4. Converter number two is active and converters number one and three are inactive.

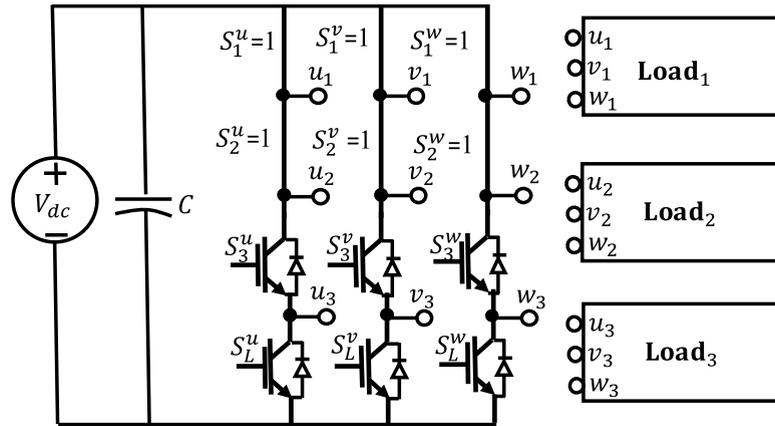


Fig. 5. Converter number three is active and converters number one and two are inactive.

$$\gamma = \begin{cases} 1 & \text{if } m_t \leq m_{max} \\ 0 & \text{if } m_t > m_{max} \end{cases} \quad (2)$$

For $i = \{1 \dots n\}$, the modified references can be formulated as

$$m_i^* = \frac{m_i}{m_{max} \times m_t} \times (\gamma \times m_t + 1 - \gamma) \quad (3)$$

$$m_t^* = \sum_{i=1}^n m_i^* \quad (4)$$

where, m_t^* is the sum of the modified modulation indices. From Eq (3) and for linear modulation, $m_i^* = m_i$ and $m_t^* = m_t$. The linear modulation case agrees with the classical modulation strategies [19–21]. However, one of the shortcoming of the classical methods is that they are not applicable for overmodulation. Nevertheless, the proposed modulation strategy is valid for all modulation regions including the overmodulation. To successfully run the $(3n + 3)$ -switch inverter and to avert any overlapping between switches, an offsets must be combined with the reference signals. The calculation of these offsets is more complicated than the nine-switch converter [15–19]. The classical offsetting is adopted to formulate the offsets for the generalized $(3n + 3)$ -switch inverter. For each load reference, the offset (os), for $i = \{1 \dots n\}$ is calculated as:

$$os_i = m_t^* - \left(m_i^* + 2 \sum_{j=1}^{i-1} m_j^* \right) \quad (5)$$

If the difference between m_{max} and m_t^* is positive, i.e., $m_{max} - m_t^* > 0$, then a factor of this difference can be utilized to modify the modulated signal by shifting up or down subset of the modulation signals or all of them. This factor (Δm) is given by:

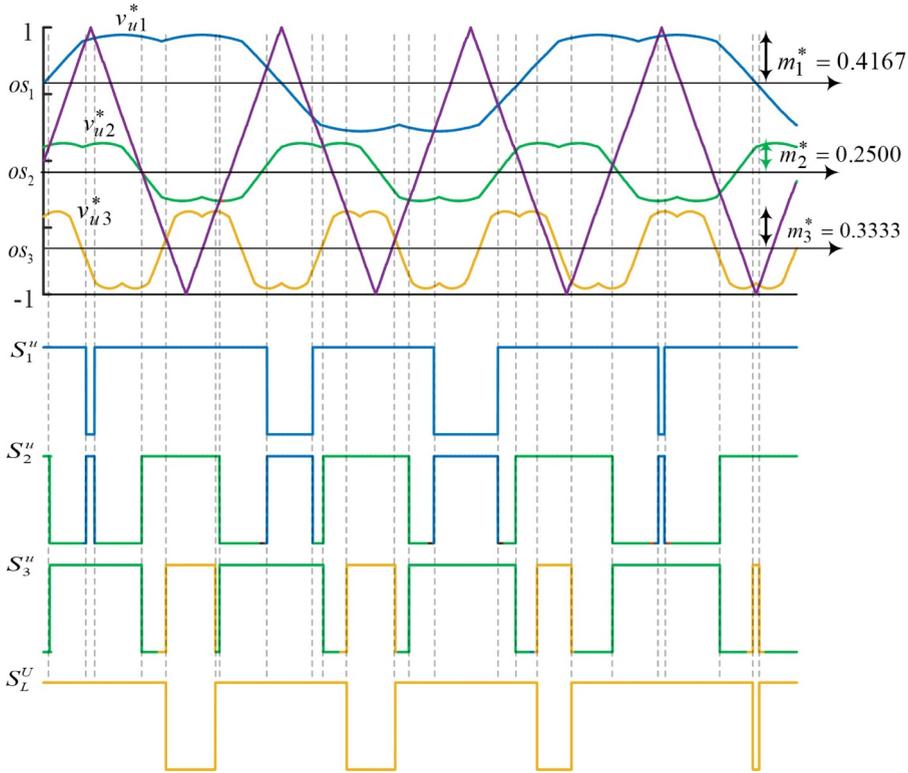


Fig. 6. Example for non-sinusoidal PWM when $m_1 = 0.5$, $m_2 = 0.3$, $m_3 = 0.4$, $\gamma = 0$, and $\Delta m = 0$.

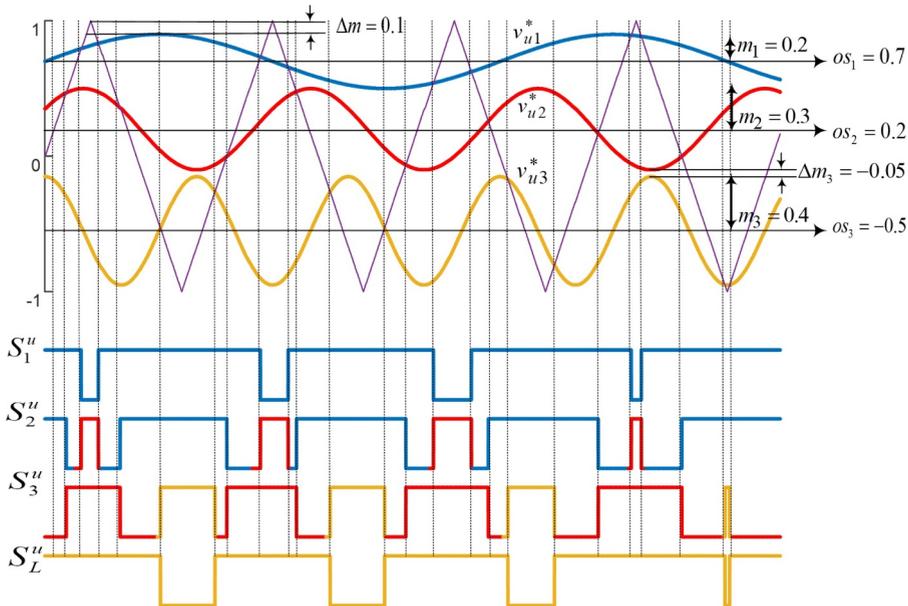


Fig. 7. Example for a sinusoidal PWM when $m_1 = 0.2$, $m_2 = 0.3$, $m_3 = 0.4$, $\gamma = 1$, $\Delta m_{max} = 0.1$, $\Delta m_1 = \Delta m_2 = 0$, and $\Delta m_3 = -0.05$.

$$\Delta m = \alpha(m_{max} - m_i^*) \tag{6}$$

Δm can be considered as an innovative DOF in the presented technique that is used to enhance the power quality. $-1 \leq \alpha \leq 1$ and the value of α is subjected to the logical constraint where no overlap between the modulating signals is permissible. This introduced DOF Δm can be utilized to any share with each modulating signal as Δm_i . For example, $\sum_{i=1}^n \Delta m_i \leq 2\Delta m$ with no intersection between the loads references, and $\Delta m_i = \alpha_i \times \Delta m$. Adopting the new proposed DOF, the offsets for the generalized $(3n + 3)$ -switch inverter can be mathematically included for $i = \{1 \dots n\}$ as:

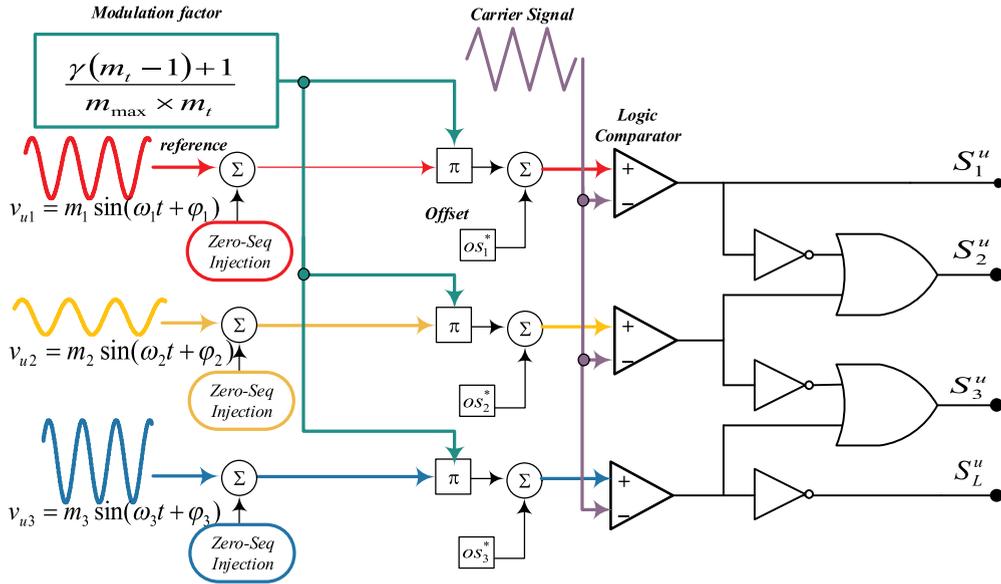


Fig. 8. $(3n+3)$ -switch inverter when $n = 3$: a non-sinusoidal pulse generation.

$$os_i^* = m_i^* - \left(m_i^* + 2 \sum_{j=1}^{i-1} m_j^* \right) + \Delta m_i \tag{7}$$

$$os_i^* = m_i^* - \left(m_i^* + 2 \sum_{j=1}^{i-1} m_j^* \right) + \alpha_i \times (m_{max} - m_i^*) \tag{8}$$

To this end, utilizing the modified offset (os_i^*), the loads reference signals for $i = \{1 \dots n\}$ in all modulation region can be written as:

$$\begin{bmatrix} v_{ui}^* \\ v_{vi}^* \\ v_{wi}^* \end{bmatrix} = m_i^* \begin{bmatrix} \sin(\omega_i t + \varphi_i) \\ \sin(\omega_i t - \frac{2\pi}{3} + \varphi_i) \\ \sin(\omega_i t + \frac{2\pi}{3} + \varphi_i) \end{bmatrix} + \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} os_i^* \tag{9}$$

If the number of the connected loads (n) is equal to three, the switches associated with the u -leg are gated as shown in Figs. 6 and 7 employing non-sinusoidal and sinusoidal PWM method, respectively. A non-sinusoidal PWM is used in Fig. 6 with $m_1 = 0.5$, $m_2 = 0.3$, and $m_3 = 0.4$, thus $m_t = 1.2 > 1.15$. Therefore, the voltage utilization in the case of overmodulation is adopted as in Eq. (3) which yields $m_1^* = 0.4167$, $m_2^* = 0.25$, and $m_3^* = 0.3333$. Fig. 7 depicts the case when SPWM is adopted with $m_1 = 0.2$, $m_2 = 0.3$, and $m_3 = 0.4$. In this case, $\Delta m_{max} = 1 - \sum_{i=1}^3 m_i = 0.1$, and the reference of the 3rd load is moved down by -0.05 , i.e., $\alpha_3 = -0.5$ and $\Delta m_3 = 0.1$.

Fig. 8 depicts an example for pulse gating adopting the proposed non-sinusoidal PWM (zero-injected PWM) with extra DOF for a $(3n+3)$ -switch inverter in the case of $n = 3$. The figure shows u -leg pulse generation, leg v and w pulses are shifted by $-\frac{2\pi}{3}$ and $\frac{2\pi}{3}$, respectively.

4. Particle swarm optimization for the optimal selection of sorting and offsetting

An extra DOF has been added to the proposed PWM strategy by introducing Δm term, this term doesn't add any complexity or cost to the proposed PWM. However, it can be used to enhance the quality of the power at the load side.

The optimal selection of this term and its impact on the power quality of the connected loads, as measured by three harmonic related objective functions will be discussed and investigated in this section. Three objective functions are nominated for this purpose, the first one, Eq. (10), is the THD, the second one, Eq. (11), is the STHD, and the third one, Eq. (12), is the SFEH of the current of the shared loads.

$$obj_1 = \sum_{i=1}^n \frac{\sqrt{\sum_{j=1}^{f_{max}} I_{ij}^2}}{I_{i1}} \tag{10}$$

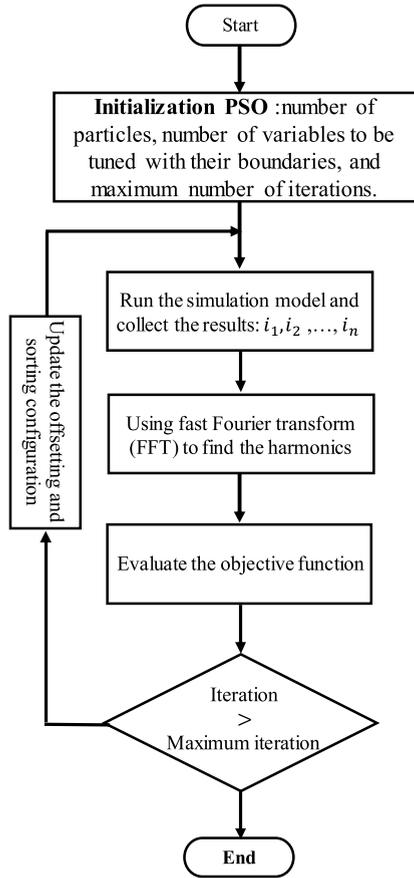


Fig. 9. Flow chart of optimal sorting and offsetting based on PSO.

$$obj_2 = \sum_{i=1}^n \sqrt{\sum_{j=1}^{f_{max}} I_{ij}^2} \tag{11}$$

$$obj_3 = \sum_{i=1}^n \frac{\sqrt{\sum_{j=1}^{11} I_{ij}^2}}{I_{i1}} \tag{12}$$

where $f_{max} = 2f_s$ in this work, f_s is the switching frequency, I_{i1} is the fundamental component of the i^{th} load current, and I_{ij} is the j^{th} harmonic of the i^{th} load current.

The first objective function is suitable when the THD of any load is more important, regardless of amount of its power consumption. On the other hand, if the power consumption of the load is of interest and has higher priority, then the second objective function is preferable. The last objective function gives more attention to the low order harmonics up to the eleventh one, this coincides with the IEEE-519 harmonic standard.

To this end, the power quality of the connected loads will be improved as a result of the minimization of the above objective functions. Therefore, PSO is employed to find the optimal offsetting values and the optimal sorting configuration that will minimize any of the aforementioned objective functions. The optimization problem in Eqs. (10)–(12) is carried out using PSO. A generalized summary of PSO is shown in Fig. 9 as a flow chart.

The offsetting values are adjusted, by updating the position (os_j) and velocity (v_j) of each particle, employing Eqs. (13) and (14) until the termination criterion is met [24,25].

$$v_j(i + 1) = \omega \times v_j(i) + \gamma_1 \times \alpha_1 \times (Pb_j(i) - os_j(i)) + \gamma_2 \times \alpha_2 \times (Gb(i) - os_j(i)) \tag{13}$$

$$os_j(i + 1) = os_j(i) + v_j(i + 1) \tag{14}$$

where ω is inertia factor $\in [0.4, 1.2]$, γ_1 and γ_2 are acceleration factors $\in [0, 2]$, and α_1, α_2 are two uniform random numbers $\in [0, 1]$ regenerated every velocity update. i is the iteration number, j is the particle index, $Pb_j(i)$ is the local best, and $Gb(i)$ is the so far global best offset value.

The PSO parameters ($\omega, \gamma_1,$ and γ_2) have an impact on the solution convergence in which lower value of ω , accelerate solution

Table 1
PSO parameters.

Parameters	Values
Swarm size (n_s)	20
Inertia factor (ω)	As in Eq. (15)
Cognitive factor (γ_1)	1.6
Social factor (γ_2)	1.7
Number of iterations (i_m)	200

convergence, while higher value promote exploring the search space. γ_1 decides the confidence of a particle in the personal attractor, while γ_2 is related to the global attractor confidence.

In this study, ω has the following relation

$$\omega = 0.9 - 0.25 \times i/i_m \quad (15)$$

where i_m is the number of iterations. This selection allows the particles to explore in the initial search steps, while favoring exploitation as optimization progress. Moreover, γ_1 and γ_2 are chosen to be 1.6 and 1.7, respectively. It is easy to show that, such PSO parameters selection obeys $\omega > 0.5(\gamma_1 + \gamma_2) - 1$, which guarantees particle trajectories convergent [25]. Furthermore, the swarm size (n_s) and the number of iterations (i_m) affect the solution, a good choice of n_s is in between [10, 30]. A summary of PSO parameters selection including the swarm size and number of iterations with their impact on the solution convergence is discussed in [25]. In this work, the used PSO parameters are given in Table 1.

5. Simulation

The proposed two degrees of freedom PWM scheme is numerically verified in this section when the number of connected loads is three. The same lines are applicable for n -loads, without loss of generality. The data that are used in the simulation are listed in Table 2, considering RL -loads. The adopted data matches the experimental setup that is used to experimentally validate the proposed procedure in the next section.

Six possible arrangements of the loads are listed in Table 3, if load sorting is applicable which is the case during the design stage.

For each of the six loads configuration listed in Table 3, a PSO algorithm shown in Fig. 9 is adopted to search for the optimal sorting and/or offsetting, when applicable, at which one of the three objective functions (obj_1, obj_2, obj_3) is minimum. Furthermore, the effect of the dead-time is taken into account to make the simulation close enough to the experimental conditions.

Without loss of generality, the reference voltages expressed in Eq. (16) is considered in presenting the idea.

Table 2
Simulation parameters.

Parameters	Values
DC voltage	60 V
Switching frequency	10 kHz
Sampling time	1 μ s
Dead time	2 μ s
R_{Load} for all loads	3.4 Ω
L_{Load1}	1 mH
L_{Load2}	0.5 mH
L_{Load3}	1.8 mH

Table 3
Possible loads arrangement.

Configuration number	Physical load-port connection		
	Port ₁	Port ₂	Port ₃
123	Load ₁	Load ₂	Load ₃
132	Load ₁	Load ₃	Load ₂
213	Load ₂	Load ₁	Load ₃
231	Load ₂	Load ₃	Load ₁
312	Load ₃	Load ₁	Load ₂
321	Load ₃	Load ₂	Load ₁

Table 4The results for obj_1 for sorting only case and classical offsetting.

Configuration	THD _{L1}	THD _{L2}	THD _{L3}	THD
123	7.2904	10.0714	5.0043	22.3661
132	7.2899	3.6488	15.4198	26.3585
312	15.6887	4.9981	5.0345	25.7213
213	15.5932	3.7605	7.1796	26.5333
231	5.2143	4.9929	15.4764	25.6836
321	5.3158	10.1372	7.1801	22.6331

Table 5The results for obj_2 objective function for sorting only and classical offsetting.

Configuration	STHD _{L1}	STHD _{L2}	STHD _{L3}	STHD
123	21.5971	21.4237	10.0689	53.0897
132	21.5964	7.2796	32.8943	61.7703
312	33.2554	14.6985	10.0849	58.0388
213	33.0856	7.5256	21.2734	61.8846
231	10.3974	14.6927	33.1030	58.1931
321	10.6584	21.4594	21.2742	53.3920

Table 6The results for obj_3 objective function for sorting only and classical offsetting.

Configuration	SFEH _{L1}	SFEH _{L2}	SFEH _{L3}	SFEH
123	2.4936	4.5400	1.8841	8.9177
132	2.4934	2.0427	3.9887	8.5248
312	4.5169	2.7756	1.8845	9.1770
213	4.2245	2.0005	2.5045	8.7295
231	2.1809	2.7492	4.2595	9.1896
321	2.3587	4.7409	2.5045	9.6041

Table 7The results for obj_1 for sorting and leveling.

Configuration	THD _{L1}	THD _{L2}	THD _{L3}	THD	os_1^*	os_2^*	os_3^*
123	7.0163	9.7598	4.8518	21.6279	0.5854	-0.0870	-0.6724
132	6.8730	3.7955	14.7540	25.4225	0.5731	-0.0870	-0.6600
213	14.6061	4.9406	4.9654	24.5121	0.6529	0.0000	-0.6529
231	14.6909	3.3748	6.8510	24.9167	0.6477	0.0870	-0.5608
312	4.8892	4.8588	14.7194	24.4673	0.6672	0.0000	-0.6672
321	4.8806	9.7780	7.0228	21.6814	0.6744	0.0870	-0.5875

Table 8The results for obj_3 for sorting and leveling.

Configuration	SFEH _{L1}	SFEH _{L2}	SFEH _{L3}	SFEH	os_1^*	os_2^*	os_3^*
123	1.83213	4.01194	1.87389	7.71796	0.5864	-0.0870	-0.6734
132	1.94908	1.97896	2.43518	6.36323	0.6501	-0.0870	-0.7371
213	2.33064	2.24668	1.89638	6.47370	0.7032	0	-0.7032
231	2.43342	1.62559	2.10025	6.15926	0.6570	0.0870	-0.5700
312	1.82958	2.27179	2.37515	6.47652	0.6570	0	-0.6570
321	1.91188	4.08835	1.85187	7.85209	0.6744	0.0870	-0.5875

Table 9
The results for obj_2 for sorting and leveling.

Configuration	STHD _{L,1}	STHD _{L,2}	STHD _{L,3}	STHD	os_1^*	os_2^*	os_3^*
123	20.1209	21.7094	9.6797	51.5101	0.5721	-0.0870	-0.6590
132	20.3973	7.7340	31.2498	59.3812	0.5731	-0.0870	-0.6600
213	31.1113	14.4473	9.7891	55.3477	0.6570	0.0000	-0.6570
231	31.0081	6.8759	20.3314	58.2155	0.6477	0.0870	-0.5608
312	9.6909	14.4339	31.1749	55.2997	0.6672	0.0000	-0.6672
321	9.8100	21.4352	20.3317	51.5769	0.6600	0.0870	-0.5731

$$\begin{bmatrix} v_{u1} \\ v_{u2} \\ v_{u3} \end{bmatrix} = \begin{bmatrix} 0.4 \sin(180\pi t) \\ 0.3 \sin(120\pi t) \\ 0.3 \sin(240\pi t) \end{bmatrix} \tag{16}$$

If SPWM is employed, sorting is only available option as the sum of the modulation indices is unity. This case represents the impact of the first DOF (sorting) while adopting the classical offsetting method. However, if non-sinusoidal PWM is employed, then sorting and offsetting are applicable. The results are shown in Tables 4–6 are for sorting only case utilizing SPWM.

Based on these results and considering the three objective functions, the configuration ‘123’ can be the optimal from minimizing

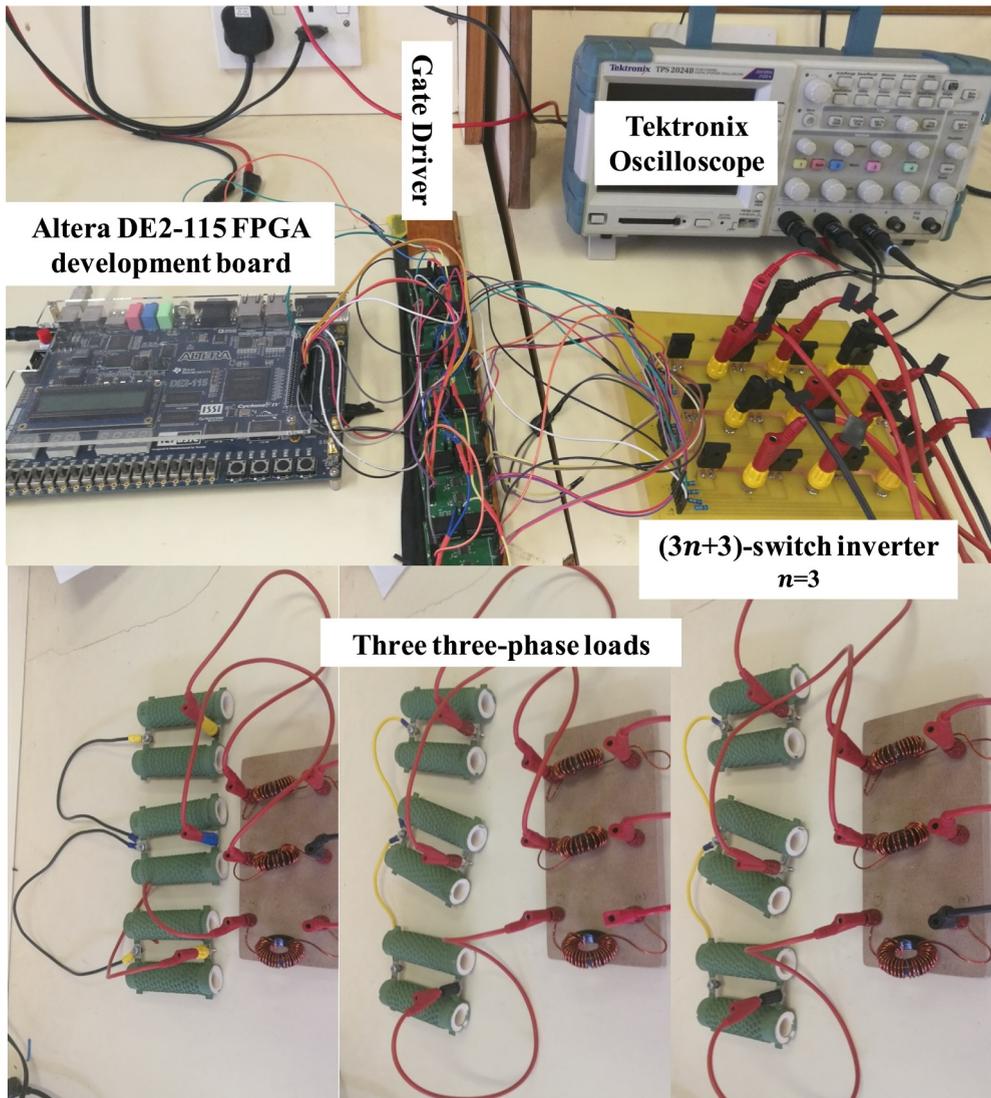


Fig. 10. The experimental test-bed.

Table 10
Experimental results utilizing obj_1 for optimal sorting and offsetting.

Configuration	THD _{L1}	THD _{L2}	THD _{L3}	THD
123	8.6069	11.0285	7.1983	26.8337
132	8.6967	6.3631	17.5334	32.5931
312	17.0231	7.2072	7.3786	31.6089
213	17.3655	6.0439	8.7984	32.2079
231	7.4201	7.2395	17.2048	31.8644
321	7.4161	11.0546	8.5478	27.0185

Table 11
Experimental results utilizing obj_3 for and optimal sorting and offsetting.

Configuration	SFEH _{L1}	SFEH _{L2}	SFEH _{L3}	SFEH
123	2.6597	4.4919	2.4317	9.5832
132	2.4633	3.0859	2.6174	8.1666
312	3.0627	2.5058	2.8536	8.4221
213	2.7268	2.2423	2.9468	7.9159
231	2.6597	2.8585	2.6284	8.1466
321	3.0728	4.3064	2.9906	10.3698

Table 12
Experimental results utilizing obj_2 for optimal sorting and offsetting.

Configuration	STHD _{L1}	STHD _{L2}	STHD _{L3}	STHD
123	23.0859	25.2061	10.7776	59.0697
132	23.3277	9.3644	36.5229	69.2150
312	34.4195	17.0989	11.8654	63.3837
213	34.5026	8.9750	23.4996	66.9772
231	11.8820	17.1762	34.6170	63.6752
321	10.9324	25.1971	22.1292	58.2586

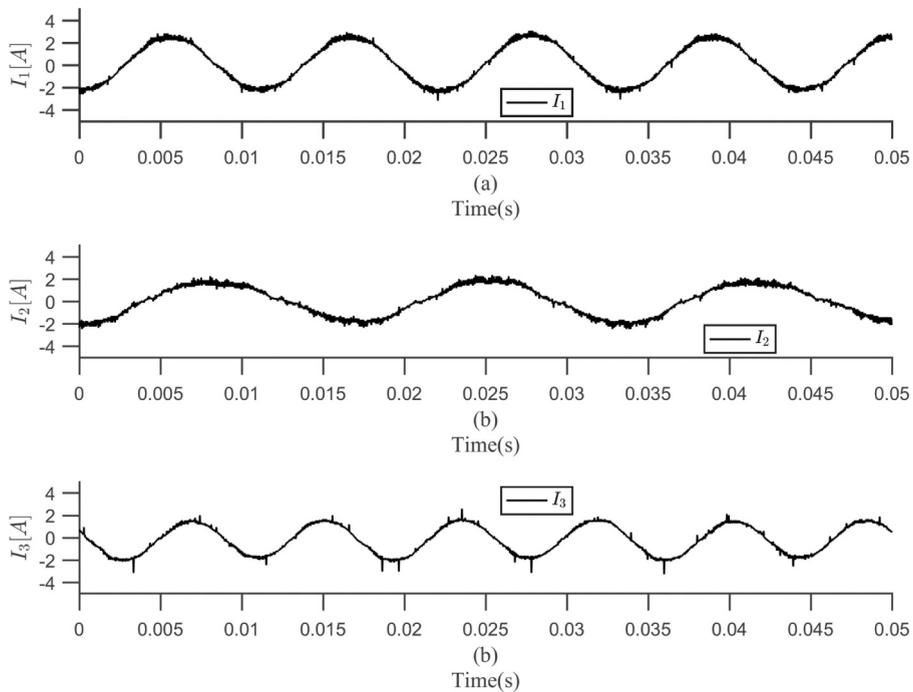


Fig. 11. Experimental results of u -phase currents waveforms of (16) for configuration ‘123’ of Table 10.

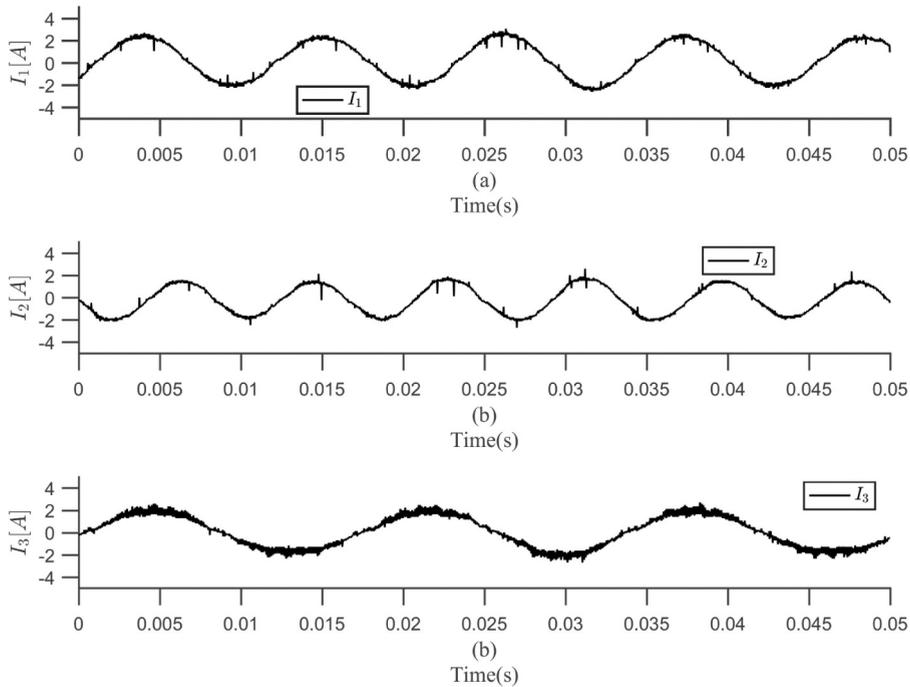


Fig. 12. Experimental results of u -phase currents waveforms of (16) for configuration '132' of Table 10.

THD or $STHD$ point of view. When minimizing the $SFEH$ has the highest priority, the configuration '132' is the optimal. These results highlight the impact of the sorting, which is the first DOF, on the output currents. The simulation results for optimal sorting and offsetting employing non-sinusoidal PWM are shown in Tables 7–9, respectively.

Comparing the results of the configuration '123', to those in Tables 4 and 5. The proposed optimal sorting and offsetting PWM achieved almost 3% mitigation in of THD and $STHD$ without any additional burden or cost. Moreover, all the harmonic indices are improved utilizing the optimal sorting and offsetting PWM compared to the results of optimal sorting only. The simulation results highlight the effect of offsetting and sorting the terminals and their modulating signals on their harmonic spectrums.

6. Experimental results

The proposed procedure is implemented in Altera® DE2-115 field-programmable-gate-array (FPGA) development board and used to control the converter. The experimental test-bed shown in Fig. 10, has the same nominal system parameters as listed in Table 2.

The experiment is conducted with references as in Eq. (16) and employing the presented two DOF PWM technique. The experimental results for the optimum sorting and offsetting PWM are shown in Tables 10–12, respectively.

Considering minimizing the THD , the nominated configuration is '123'. The second objective which is $SFEH$ gives the superiority to the configuration '213' while '321' is nominated when minimizing the $STHD$ is the goal.

The experimental results of u -phase current waveforms of Eq. (16) for configuration '123' and '132' in Table 10 are shown in Figs. 11 and 12, respectively.

Examining the experimental results and comparing them to the results obtained from the simulation verifies the proposed PWM and highlights the effectiveness that is achieved from the extra DOF in the presented PWM technique in enhancing the quality at the output-side without adding any passive elements.

7. Conclusion

For any converter from $(3n + 3)$ -family converter, an optimal two degrees of freedom PWM is proposed to enhance the quality of the shared loads measured by three harmonic related objective functions. The improvement in power quality was achieved without the need of any extra hardware or effort. Not only the proposed method achieves harmonics minimization but also provides a method to optimally distribute the dc-link voltage during linear and overmodulation regions. Comprehensive mathematical formulation of the proposed two degrees of freedom PWM is presented and the advantages of the two degrees of freedom PWM are highlighted using simulation and experimental case studies. The PSO is adopted to find the optimal offsetting and sorting if applicable. The proposed optimal sorting and offsetting PWM achieves about 3% mitigation in THD and $STHD$ without any additional overhead comparing to the classical offsetting method.

Acknowledgments

This research was supported by the deanship of research at Jordan University of Science and Technology (Grant number: 20180250).

References

- [1] Ewald Fuchs and Mohammad A. S. Masoum. (2015) Power quality in power systems and electrical machines (Second 2nd editioned.).
- [2] X Liang, Emerging power quality challenges due to integration of renewable energy sources, *IEEE Trans. Indust. Appl.* 53 (2017) 855–866, <https://doi.org/10.1109/tia.2016.2626253>.
- [3] R Lamedica, A Ruvio, P Ribeiro, M Regoli, A Simulink model to assess harmonic distortion in MV/LV distribution networks with time-varying nonlinear loads, *Simulat. Model. Pract. Theo.* 90 (2019) 64–80, <https://doi.org/10.1016/j.simpat.2018.10.012>.
- [4] A Mishra, P Tripathi, K Chatterjee, A review of harmonic elimination techniques in grid connected doubly fed induction generator based wind energy system, *Renew. Sustain. Energy Rev.* 89 (2018) 1–15, <https://doi.org/10.1016/j.rser.2018.02.039>.
- [5] Z Gao, Y Qiu, X Zhou, Y Ma, An overview on harmonic elimination, 2015 IEEE International Conference on Mechatronics and Automation (ICMA), 2015, <https://doi.org/10.1109/icma.2015.7237448>.
- [6] J Wells, X Geng, P Chapman, P Krein, B Nee, Modulation-Based Harmonic Elimination, *IEEE Trans. Power Electron.* 22 (2007) 336–340, <https://doi.org/10.1109/tpe.2006.888910>.
- [7] A Domijan, E Embriz-Santander, Harmonic mitigation techniques for the improvement of power quality of adjustable speed drives (ASDs), Fifth Annual Proceedings on Applied Power Electronics Conference and Exposition. 1990, <https://doi.org/10.1109/apec.1990.66401>.
- [8] X Guo, W Wu, H Gu, Modeling and simulation of direct output current control for LCL-interfaced grid-connected inverters with parallel passive damping, *Simulat. Model. Pract. Theo.* 18 (2010) 946–956, <https://doi.org/10.1016/j.simpat.2010.02.010>.
- [9] V Khadkikar, Enhancing electric power quality using UPQC: a comprehensive overview, *IEEE Trans. Power Electron.* 27 (2012) 2284–2297, <https://doi.org/10.1109/tpe.2011.2172001>.
- [10] T Demirdelen, R Kayaalp, M Tumay, Simulation modelling and analysis of modular cascaded multilevel converter based shunt hybrid active power filter for large scale photovoltaic system interconnection, *Simulat. Model. Pract. Theo.* 71 (2017) 27–44, <https://doi.org/10.1016/j.simpat.2016.11.003>.
- [11] B Singh, V Verma, A Chandra, K Al-Haddad, Hybrid filters for power quality improvement, *IEE Proceedings - Generation, Transmission and Distribution*, 152 2005, p. 365, , <https://doi.org/10.1049/ip-gtd.20045027>.
- [12] M Najjar, A Moeini, M Bakhshizadeh, F Blaabjerg, S Farhangi, Optimal selective harmonic mitigation technique on variable DC link cascaded H-bridge converter to meet power quality standards, *IEEE J. Emerg. Select. Topic. Power Electron.* 4 (2016) 1107–1116, <https://doi.org/10.1109/jestpe.2016.2555995>.
- [13] A Moeini, H Zhao, S Wang, A current-reference-based selective harmonic current mitigation PWM technique to improve the performance of cascaded H-bridge multilevel active rectifiers, *IEEE Trans. Indust. Electron.* 65 (2018) 727–737, <https://doi.org/10.1109/tie.2016.2630664>.
- [14] S Kang, K Kim, Sliding mode harmonic compensation strategy for power quality improvement of a grid-connected inverter under distorted grid condition, *IET Power Electron.* 8 (2015) 1461–1472, <https://doi.org/10.1049/iet-pel.2014.0833>.
- [15] F Gao, L Zhang, D Li, P Loh, Y Tang, H Gao, Optimal pulsewidth modulation of nine-switch converter, *IEEE Trans. Power Electron.* 25 (2010) 2331–2343, <https://doi.org/10.1109/tpe.2010.2047733>.
- [16] N Jarutus, Y Kumsuwan, Level-shift space vector pulse width modulation for a nine-switch inverter, 2015 12th International Conference on Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology (ECTI-CON). 2015, <https://doi.org/10.1109/ecticon.2015.7206987>.
- [17] N Jarutus, Y Kumsuwan, A comparison between level- and phase-shift space vector duty-cycle modulations using a nine-switch inverter for an ASD. 2015, 18th International Conference on Electrical Machines and Systems (ICEMS). 2015, <https://doi.org/10.1109/icems.2015.7385346>.
- [18] N Jarutus, Y Kumsuwan, A carrier-based phase-shift space vector modulation strategy for a nine-switch inverter, *IEEE Trans. Power Electron.* 32 (2017) 3425–3441, <https://doi.org/10.1109/tpe.2016.2587811>.
- [19] T Kominami, Y Fujimoto, Inverter with reduced switching-device count for independent AC motor control, *IECON 2007 - 33rd Annual Conference of the IEEE Industrial Electronics Society.* 2007, <https://doi.org/10.1109/iecon.2007.4460118>.
- [20] K Aganah, O Ojo, Generalized carrier-based PWM method for a 12-switch converter, *Open Eng.* (2016), <https://doi.org/10.1515/eng-2016-0022>.
- [21] K Aganah, O Ojo, Pulsed-width modulation technique for family of (3N + 3)-switch converters, 2014 IEEE Energy Conversion Congress and Exposition (ECCE). 2014, <https://doi.org/10.1109/ecce.2014.6953513>.
- [22] S Albatran, I Smadi, M Alsyouf, Selective harmonics reduction for 3(n + 1) switch inverter using optimal leveling and sorting PWM technique, *IECON 2017 - 43rd Annual Conference of the IEEE Industrial Electronics Society*, 2017, <https://doi.org/10.1109/iecon.2017.8216258>.
- [23] M Hagh, H Taghizadeh, K Razi, Harmonic minimization in multilevel inverters using modified species-based particle swarm optimization, *IEEE Trans. Power Electron.* 24 (2009) 2259–2267, <https://doi.org/10.1109/tpe.2009.2022166>.
- [24] Fukuyama Y Fundamentals of Particle Swarm Optimization Techniques. *Modern Heuristic Optimization Techniques* 71–87. doi: 10.1002/9780470225868.ch4.
- [25] A. Engelbrecht, *Computational Intelligence*, John Wiley & Sons, Chichester, 2008 Chapter 16.