Highly Efficient Single-Phase Buck-Boost Variable-Frequency AC-AC Converter with Inherent Commutation Capability

Saeed Sharifi, Mohammad Monfared, *Senior Member, IEEE*, Mohammad Babaei, and Alireza Pourfaraj

***Abstract*—This paper introduces a novel single-phase buck-boost (non-)inverting variable-frequency AC-AC converter that offers a higher efficiency compared to the competitors. This converter utilizes a lower number of semiconductors. A simple and flexible switching strategy is also proposed, which generates the desired output waveform avoiding unnecessary high-frequency switching operation of semiconductor devices. A high reliable operation due to the elimination of the input source shoot-through risk, an inherent commutation capability that mitigates the voltage spikes across the semiconductors, a lower semiconductors rating requirement, an improved input current waveform quality and a smaller required input filter inductor are the main advantages of the proposed converter. Thus, the proposed converter can be successfully applied to many industrial applications such as medium-frequency transformer-isolation (MFT) for traction and wind turbine converters, AC-DC high-voltage conversion based on Cockcroft-Walton circuit and induction heating systems. The theoretical achievements and claims are all confirmed through extensive experimental tests on a 200-W laboratory setup.**

***Index Terms*—Buck-boost, high efficiency, inherent commutation, variable-frequency.**

I. Introduction

MANY industrial applications such as the adjustable speed drives require AC-AC power conversion systems offering flexible output AC voltage properties. The most recently proposed direct AC-AC converters in [1]–[6], successfully provide a wide range gain buck-boost operation for simultaneous increase or decrease of the output voltage amplitude. These converters offer many advantages including snubber-less operation, inherent commutation, high-quality input current and output voltage waveforms and reliable and efficient operation. However, they do not have the ability to change the frequency of the output voltage waveform, which is already necessary for many industrial applications. On the other hand, the AC-DC-AC converters can generate any arbitrary waveform at the output through several power stages [7]–[10].

Manuscript received November 12, 2018; revised December 27, 2018 and February 17, 2019; accepted April 14, 2019.

The authors are with the Department of Electrical Engineering, Faculty of Engineering, Ferdowsi University of Mashhad, Mashhad 91779-48974, Iran (e-mail: saeed.sharifi@mail.um.ac.ir; m.monfared@um.ac.ir; mohammad.babaei@mail.um.ac.ir; alireza.pourfaraj@mail.um.ac.ir).

In addition, they need large DC-link capacitors and filter inductors, which increase their implementation cost, size and power loss. The other AC-AC converters with the ability to change the frequency are the matrix converters (MCs) that directly connect the input source to the output without needing large DC-link capacitors [11]–[14]. It is worth mentioning that the single-phase MCs, in contrary with the AC-DC-AC competitors, cannot generate pure sinusoidal output voltage waveforms, though they have recently found wide applications such as adjustable speed drives, aircraft power supplies and induction heating systems [15]–[17]. The first single-phase MC, proposed by Zuckerberger *et al*. in [18], can only decrease the voltage magnitude and increase its frequency with low power quality and harsh voltage spikes. In [19] and [20], a safe commutation strategy is proposed for the converter of [18]. However, the quality of waveforms is not yet acceptable. Some other single-phase MCs are presented in [15] and [20], which are not suitable for the applications requiring both step-up and step-down operation due to their limited gain range. In order to provide a wide gain range, the Z-source-based MC is proposed in [21], shown in Fig. 1(a), which offers the capability of simultaneous buck and boost operation. However, it requires a high number of energy storage components and ten semiconductors leading to low efficiency and high size and cost. Moreover, it suffers from a severe commutation problem leading to large voltage spikes.

In [22], a successful single-phase buck-boost MC that is shown in Fig. 1(b) is proposed, which avoids the shoot-through of the input voltage source even when all switches are turned ON. This MC can effectively operate in both inverting and non-inverting and both buck and boost modes with respect to the input voltage. It employs a lower number of semiconductors yet produces a discontinuous input current, which necessitates employing the input side filters. The complexity of the switching strategy, the need for a turn-OFF delay for safe commutation of the inductor current and the high number of conducting semiconductors at the same time that decreases the efficiency are some of the main drawbacks of the MC shown in Fig. 1(b).

To overcome the limitations and problems of the previous MCs, this paper proposes a novel single-phase variable-frequency AC-AC converter with remarkable features, especially compared to the successful MC of Fig. 1(b), as listed below:

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2019.2914644, IEEE Transactions on Industrial Electronics

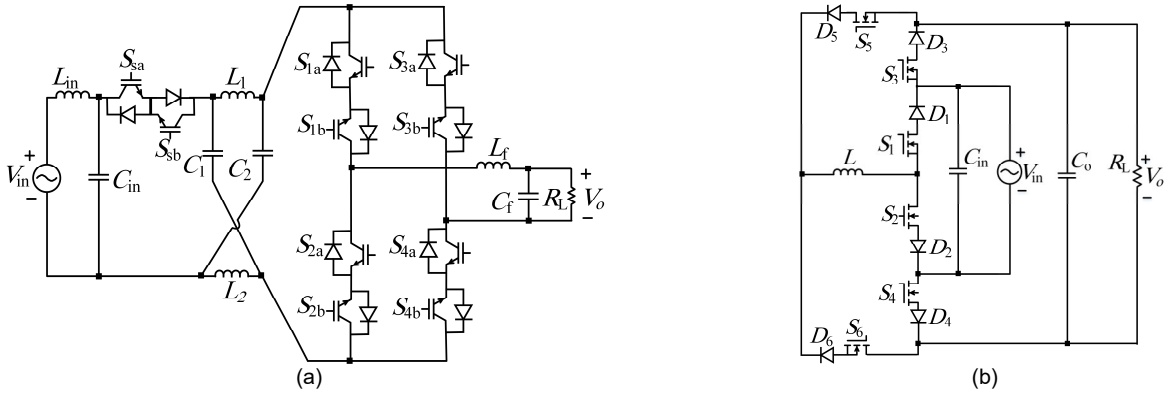

Fig. 1. Single-phase matrix converters with (a) the Z-source network of [21], and (b) six switch of [22].

- The proposed converter can operate in both buck and boost modes and also inverting and non-inverting modes with respect to the input voltage waveform;
- the total number of the semiconductors are lower, which lowers the cost of implementation and increases its power density;
- the number of semiconductors that simultaneously conduct in each mode of operation is decreased, also just one high-frequency semiconductor conducts during each mode, thus, the losses are decreased;
- a very simple and flexible switching strategy is proposed that reduces the complexity of its realization for obtaining various output frequencies;
- it offers inherent safe commutation capability, which immunes it from high voltage spikes across the semiconductors without the need for a commutation strategy, dead-times and snubber circuits. Also, it avoids the shoot-through of the input voltage source the same as the MC of Fig. 1(b);
- a quasi-continuous input current for the proposed converter, unlike the discontinuous waveform of the circuit of Fig. 1(b), improves the quality of the converter waveforms and also reduces the input filtering requirements.
- the proposed converter can be employed in a wide range of variable-frequency applications, especially those requiring a high-quality input current and mainly not sensitive to output waveforms quality, including the radio frequency induction heating, similar to [16] and [23], the Cockcroft-Walton voltage multiplier AC-DC conversion, similar to [24] and [20], the medium-frequency transformer-isolation for traction or wind turbine converters, similar to [25] and [26], the dynamic voltage restoring (DVR), similar to [27] and [28], etc.

The experiments on a 200-W laboratory prototype, followed by a comprehensive analysis confirming the superior performance of the proposed converter and the claimed features above.

II. Proposed Converter

The circuit diagram of the proposed buck-boost converter is shown in Fig. 2, which includes six switches S_1-S_6 and four diodes D_1-D_4. It also employs two bypass capacitors C_1 and C_2 and two inductors L_1 and L_2. The bypass capacitors provide a safe commutation path for the inductors currents and at the same time improve the input current continuity and also contribute to the load current, which eliminates the need for an output filter capacitor. In addition, the current loop constructed from the capacitors C_1 and C_2 and the input voltage supply is always electrically connected. Thus, these capacitors can effectively play the role of the input filter capacitor. Indeed, the capacitors C_{in} and C_o, shown in Fig. 2, are not necessary for the proper operation of the proposed converter and are only added as extra practical measures to effectively snub the transients, which may rarely occur in experiments and if they are removed, the quality of waveforms will not be affected. Besides, the inductors L_1 and L_2 share a common magnetic core, which lets considerably reduce the size of the required magnetic element. The switch S_1, the diodes D_2 and D_3 and the inductor L_1 construct the positive switching-cell, highlighted in red. Also, the switch S_2, the diodes D_1 and D_4, and the inductor L_2 create the negative switching-cell, highlighted in blue in Fig. 2. The positive and negative switching-cells are only active during the positive and negative half cycles of the input voltage, respectively. In addition, the part of the circuit already shadowed in gray is a low frequency unfolding switching-cell including the switches S_3-S_6.

The detailed operation principles and the switching strategy of the proposed converter are presented in the following.

A. Switching Strategy

Based on the desired output frequency, the switching strategy of the proposed converter is shown in Fig. 3. Three different frequencies including 30Hz, 60Hz and 120Hz for the output voltage waveform is depicted in this figure with assuming the input voltage frequency f_{in} = 60Hz. It is worth mentioning that the output waveform frequency can be arbitrary chosen regardless of the source frequency. Although, with the output frequencies being integer multiples or integer fractions of the input frequency, the output voltage waveform would be symmetric and thus have a higher quality. As seen in Fig. 3, the two switches S_1 and S_2 are PWM controlled through the comparison of a reference signal (*Ref.*) and a high-frequency triangular carrier waveform. The PWM stands for the pulse-width modulation. The two switches S_3 and S_6 are switched ON and OFF as the complementary of the other two switches S_4 and S_5. These low-frequency switches employ gating signals with the desired output frequency for folding the input voltage waveform. The generated output waveform by using this simple switching strategy is acceptable for those applications that are

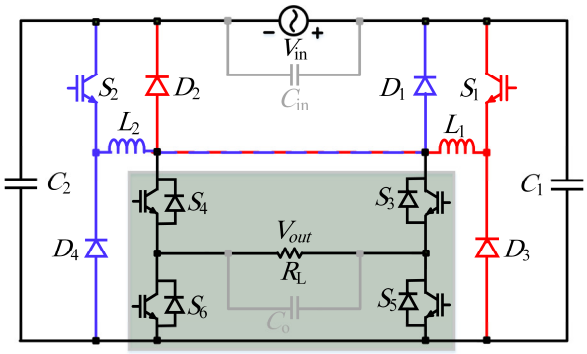

Fig. 2. Proposed single-phase buck-boost variable-frequency AC-AC converter.

not sensitive to the waveforms quality while the input waveform quality is a major concern such as those mentioned at the end of section I. Despite, due to employing two sub-circuits, being the positive (negative) switching-cell and the low-frequency switching-cell, the proposed converter has the potential to operate by more advanced switching strategies to generate high quality output waveforms required by for example an induction motor drive system.

The switching strategy of Fig. 3 can be clarified during each cycle of the output voltage waveform with the desired output frequency in two modes of operation. The operation of the proposed converter for the output frequency of 60Hz is presented in the following from which the other frequencies operation can be derived as well.

1) Positive Half Cycle of 60Hz Output Voltage

As shown in Fig. 3, the low frequency switches S_3 and S_6 are ON during the positive half cycle of the 60Hz output voltage waveform. As another solution, if the switches S_4 and S_5 turn ON instead of the switches S_3 and S_6, the output voltage waveform is out of phase with the input voltage leading to the inverting operation of the proposed converter.

a) Mode I: (DT_s)

As seen from Fig. 3, both switches S_1 and S_2 are fed from a same PWM gate signal with DT_s dwell time. Assuming that the input voltage is in its positive half cycle ($V_{in} > 0$), the switch S_1 conducts during this mode. The inductor L_1 charges from the source through S_1 and D_2, as shown in Fig. 4(a).

The switches S_3 and S_6 are both turned ON and conduct the load current provided by the bypass capacitors C_1 and C_2. In other words, the bypass capacitors discharge their stored energy into the load from the current path created by the switches S_1, S_3 and S_6 and the inductor L_1. Therefore, the required output filter capacitor is significantly reduced.

According to the equivalent circuit shown in Fig. 4(a), the voltage equations of this time interval can be written as,

$$V_{L1} = V_{in} \tag{1}$$

$$V_{C1} = V_{in} + V_{out} \tag{2}$$

$$V_{C2} = V_{out}\,. \tag{3}$$

b) Mode II: (1-D)T_s

The switch S_1 turns OFF after DT_s and thus the inductor L_1 current flows through the forward biased diode D_3 and the switches S_3 and S_6, which are still maintained ON. As shown in Fig. 4(b), the capacitor C_2 charges from the inductor L_1 through D_2 and D_3 while the capacitor C_1 regains its energy from the source through the same current path as that for the capacitor C_2. Considering the equivalent circuit of Fig. 4(b), the voltage equations of this time interval with (1-D)T_s dwell time are obtained as,

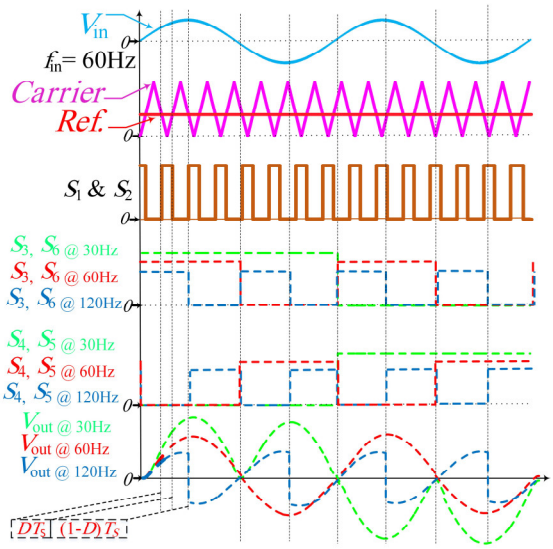

Fig. 3. Proposed simple switching strategy.

$$V_{L1} = V_{out} \tag{4}$$

$$V_{C1} = V_{in} + V_{out} \tag{5}$$

$$V_{C2} = V_{out}\,. \tag{6}$$

As obviously shown in Fig. 4(a) and (b), the diode D_2 conducts in both modes of operation. Thus, this diode is always forward biased and conducts during the whole input voltage positive half cycle.

2) Negative Half Cycle of 60Hz Output Voltage

The low frequency switches S_3 and S_6 turn OFF at the zero crossing of the output voltage waveform while the switches S_4 and S_5 receive the gate signal and consequently start conducting at this moment for whole the negative half cycle. Again, the buck-boost operation of the proposed converter can be described during two distinct modes of the negative half cycle.

a) Mode I: (DT_s)

According to Fig. 4(c), the inductor L_2 charges from the source through S_2 and D_1. Both bypass capacitors also provide the load current through S_4 and S_5. The voltage equations are the same as that for the mode I where the inductor L_1 charges during the input voltage positive half cycle.

b) Mode II: (1-D)T_s

The inductor L_2 discharges its stored energy into the load during this mode through the current path created by D_4, S_4 and S_5, as depicted in Fig. 4(d). Also, the diode D_1 maintains forward biased and thus conducts the charging current of the bypass capacitors. The voltage equations are the same as that for the mode II for discharging of L_1 into the load.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2019.2914644, IEEE Transactions on Industrial Electronics

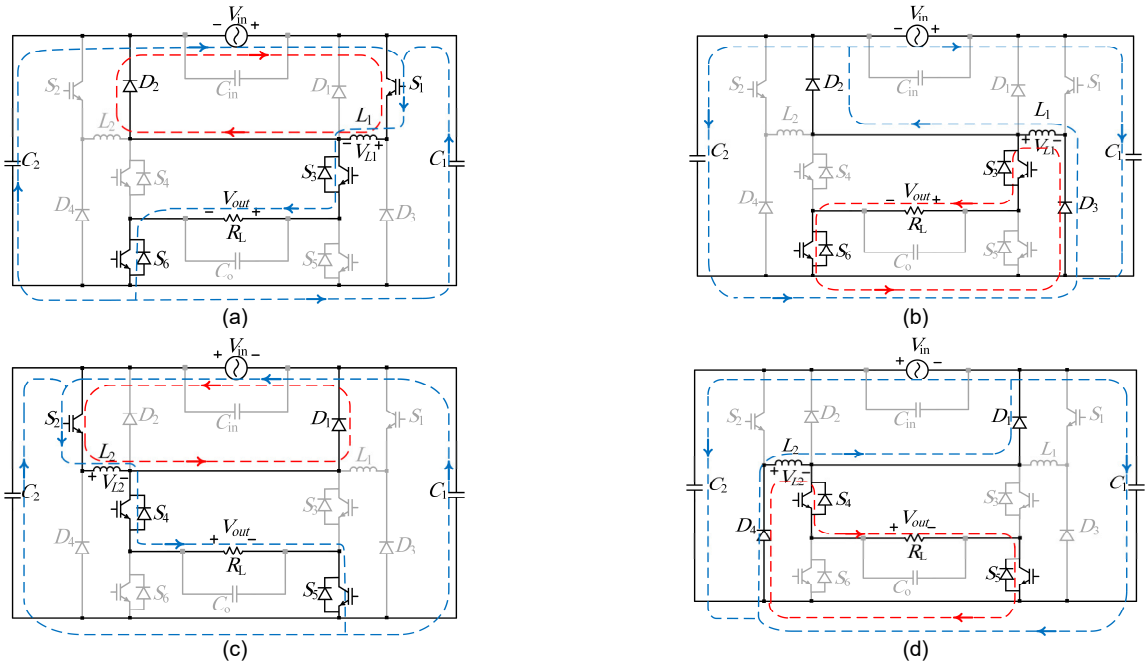

Fig. 4. Equivalent circuits of the proposed converter during input voltage positive half cycle in modes (a) I, and (b) II, and its negative half cycle in modes (c) I, and (d) II to generate 60Hz output voltage waveform.

It should be noted that D_1 and D_2 always conduct during the whole negative and the positive half cycle of the input voltage, respectively. This means that these diodes begin blocking just at the zero crossing of their currents, which significantly reduces the reverse recovery problem.

Finally, with applying the volt-second balance to the voltage across each inductor, the voltage gain equation of the proposed converter can be derived as (7), which is exactly the same as the gain equation of a conventional buck-boost converter.

$$V_{out} = \frac{D}{1-D} V_{in} \tag{7}$$

Other output frequencies can be simply obtained by changing the switching frequency of the low-frequency switching-cell while the operation of the high-frequency switching-cells remains unchanged. For example, as shown in Fig. 3, for 120Hz output frequency, the switches S_3 to S_6 operate at 120Hz. Thus, one can evidently conclude that the magnitude and frequency of the output voltage can be simultaneously and independently adjusted by the high and low-frequency switching-cells, respectively.

B. Inherent Commutation Capability

Most AC-AC converters suffer from harsh voltage spikes across their semiconductors due to the abruption of inductors currents. This problem is somehow dealt with by introducing an overlap period for the commutating switches or employing some more complicated safe commutation strategies or even additional snubber circuits to avoid any interruption in inductors currents. All these lead to a complex circuit topology and/or control technique and increase the cost and total losses. The proposed converter effectively takes benefits from the bypass parallel capacitors C_1 and C_2 as built-in clamping elements to provide an alternate path for the inductors currents once their corresponding switches are turned OFF. To more clarify the situation, assume that the switch S_1 turns OFF and mode II begins, shown in Fig. 4(b). If the switches S_3 and S_6 maintain OFF even after receiving the turn-ON command (which is due to their turn ON delay), the inductor L_1 current can still flow through the capacitor C_1 and diodes D_2 and D_3. So, no inductor current interruption occurs. However, if the capacitor C_1 was not in the circuit, then the inductor L_1 current would have been forced to zero suddenly, which would have led to a significant voltage spike across the switch S_1. Thus, with the proposed circuit configuration, the operation of the switches can be simple and safe without the need for the overlap time of the switching signals and any commutation strategy or snubber circuits. This feature of the proposed converter is called the inherent commutation capability.

C. Component Design

1) Passive Components:

The values of the inductors L_1 and L_2 are designed considering their maximum allowable current ripples ($\Delta I_{L1,2}$) from (8), where, T_s is the switching period and $\Delta I_{L1,2}$ can be considered as γ% of the peak inductors currents, given in (9).

$$L_{1,2} = \left(\frac{\sqrt{2}V_{in-(rms)}}{\Delta I_{L1,2}}\right) DT_s \tag{8}$$

$$\Delta I_{L1,2} = \gamma\%(I_{L1,2}) = \gamma\%\sqrt{2}\frac{I_{out-(rms)}}{1-D}. \tag{9}$$

Also, for the capacitors C_1 and C_2, one can calculate,

$$I_{C1} = I_{C2} = \frac{\sqrt{2}\, I_{out-(rms)}}{2} = \sqrt{2}\, I_{in-(rms)}\left(\frac{1-D}{2D}\right). \tag{10}$$

Then, assuming a same tolerable voltage ripple for both capacitors as α% of the peak voltages across them, the values of the capacitors can be obtained as,

$$C_1 = C_2 = \frac{(1-D)DT_s}{2\alpha\% V_{out-(rms)}} I_{in-(rms)}. \tag{11}$$

TABLE I
COMPARISON AMONG VARIOUS AC-AC CONVERTERS

Feature	Proposed Converter	Buck-Boost MC of [22]	Z-Source Buck-Boost MC of [21]	Boost MC of [20]	Buck MC of [19]	Buck-Boost AC-AC of [29]	Buck-Boost AC-AC of [30]
No. of switches	6 (S_1-S_6)	6 (S_1-S_6)	10 (S_1-S_{10})	8 (S_1-S_8)	8 (S_1-S_8)	4 (S_1-S_4)	4 (S_1-S_4)
No. of diodes	4 (D_1-D_4)	6 (D_1-D_6)	----	----	----	4 (D_1-D_4)	4 (D_1-D_4)
No. of inductors	2 (L_1,L_2)	1 (L)	2 (L_1,L_2)	1 (L_{in})	1 (L_f)	2 (L_1,L_2)	3 (CL_1,CL_2,L_f)
No. of magnetic cores	1	1	4	1	1	2	3
No. of high frequency semiconductors operating in each switching cycle	2	8	4	4	4	8	8
No. of semiconductors in current path in each mode of operation	4	6	10	4	6	4	4
No. of energy storing or bypass capacitors	2 (C_1,C_2)	----	2 (C_1,C_2)	----	----	2 (C_1,C_2)	2 (C_1,C_2)
Continuity of input current	Quasi-Continuous	Discontinuous	Discontinuous	Continuous	Discontinuous	Quasi-Continuous	Quasi-Continuous
Required input/output filter(s)	Small L_{in} filter	Bulky L_{in}, C_{in} & C_o filters	Bulky L_{in}, C_{in} & C_o filters	Small C_{in} & Bulky C_o filters	Bulky L_{in}, C_{in} & C_o filters	Moderate L_{in} & C_{in} filters	Moderate L_{in} & C_{in} filters
Voltage gain, V_{out}/V_{in}	$\frac{D}{1-D}$	$\frac{D}{1-D}$	$\frac{1-D}{1-2D}$	$\frac{1}{1-D}$	D	$\frac{D}{1-D}$	$\frac{D}{1-D}$
Total semiconductors current stress, $I^{tot}_{Stress-(peak)}/I_{out-(peak)}$	$\frac{8-2D}{1-D}$	$\frac{12}{1-D}$	$\frac{20}{1-D}$	$\frac{16}{1-D}$	$\frac{16}{1-D}$	$\frac{8}{1-D}$	$\frac{8}{1-D}+8I_c$
Buck-Boost operation	Yes	Yes	Yes	No	No	Yes	Yes
Inherent commutation	Yes	No	No	No	No	Yes	Yes
Need for snubber or additional soft commutation strategy	No	Yes	Yes	Yes	Yes	No	No
Current flow through body diode	No	No	Yes	Yes	Yes	No	No
Ability to change the frequency	Yes	Yes	Yes	Yes	Yes	No	No

2) Active Components:

The peak voltages across the semiconductors, which determine their blocking rating can be derived from (12).

$$\begin{cases} V_{\substack{S1,S2-(peak)\\ D3,D4-(peak)}} = \sqrt{2}\dfrac{V_{out-(rms)}}{D} \\ V_{S3\sim S6-(peak)} = \sqrt{2}V_{out-(rms)} \\ V_{D1,D2-(peak)} = \sqrt{2}\dfrac{(1-D)}{D}V_{out-(rms)}. \end{cases} \tag{12}$$

The currents through the semiconductors are also required for device selection. Readily, one can calculate,

$$\begin{cases} I_{\substack{S1,S2-(peak)\\ D3,D4-(peak)}} = \sqrt{2}\dfrac{I_{out-(rms)}}{1-D} \\ I_{S3\sim S6-(peak)} = \sqrt{2}\,I_{out-(rms)} \\ I_{D1,D2-(peak)} = \sqrt{2}\dfrac{D}{1-D}I_{out-(rms)}. \end{cases} \tag{13}$$

III. COMPARATIVE ANALYSIS

In the following subsections, a comprehensive comparison among the proposed converter, the MC competitors of [19]–[22] and AC regulators of [29] and [30] is performed, which the results are summarized in Table I.

A. Semiconductors

According to Table I, the total number of semiconductors of the proposed converter is lower than the successful recently proposed MC in [22]. In addition, the total number of semiconductors conducting the current in each mode and also the number of high frequency semiconductors in each switching cycle are minimum compared to the others. Therefore, it can be predicted that the semiconductors losses of the proposed converter are the lowest.

The total semiconductors current stresses are also reported, from which one can calculate the overall peak current stress of the proposed converter, which is considerably lower than that of the other competitors allowing the semiconductors with less current ratings for the proposed converter.

B. Total Switching Device Power Comparison

In order to quantify the voltage and current rating requirements of the semiconductors, the total peak and average switching device powers (SDP_{pk} and SDP_{avg}) already introduced in [31] are calculated for the proposed converter, as reported in (14). According to [31], the SDP_{pk} is considered as

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2019.2914644, IEEE Transactions on Industrial Electronics

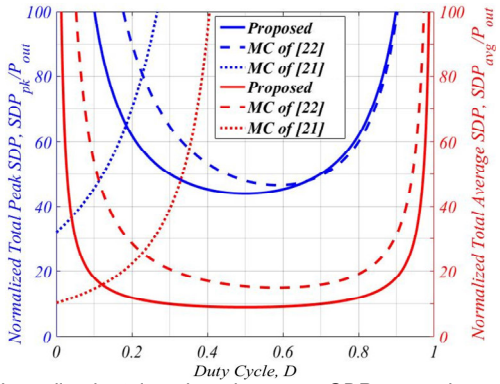

Fig. 5. Normalized total peak and average *SDP* comparison.

a cost indicator of the converters while the SDP_{avg} is used for evaluation of the thermal requirement of the semiconductors and the conversion efficiency.

$$\begin{cases} SDP_{pk} = \sum_{n=1}^{N} V_{peak} I_{peak} = \dfrac{8+12D-12D^2}{D(1-D)} P_{out} \\ SDP_{avg} = \sum_{n=1}^{N} V_{peak} I_{avg} = \dfrac{4+12D-12D^2}{\pi D(1-D)} P_{out} \end{cases} \quad (14)$$

In equation (14), N is the number of semiconductors and V_{peak} and I_{peak} are their peak voltage and current stresses, respectively.

Both SDP_{pk} and SDP_{avg} are also calculated for the MCs of [22] and [21]. Then, with assuming the same output power, all *SDP*s are plotted along with that of the proposed converter in Fig. 5 versus the duty cycle. As seen from this figure, the SDP_{pk} of the proposed converter is considerably lower than that of others for $0.2 < D < 0.6$. Thus, the proposed converter requires the semiconductors with lower peak voltage and current ratings. Also, the SDP_{avg} calculated for the proposed converter is lower than that of others in a wide range of duty cycles. Hence, one can conclude that the proposed converter lets inexpensive semiconductors utilization and also offers lower semiconductor losses, which simultaneously leads to a higher power density and thus a smaller converter size.

C. Reactive Elements

The number of the inductors of the proposed converter is also lower compared to the MC of [21]. In addition, two inductors employed in the proposed converter can be wound on a common core that reduces the magnetic element size and its power loss. Also, unlike the MC of [22], the input current waveform of the proposed converter is quasi-continuous, which lets a smaller input filter inductor. Similar to the MC of [21], the proposed converter employs two capacitors, which provide a safe commutation inductors currents path and improve the input current quality and feed the output load to reduce the required output filter capacitor. These are all achieved without the need for a high capacitance value while the MC of [21] inevitably requires large capacitors to smooth its voltage profile and to improve its waveforms quality.

IV. Performance Evaluation

To confirm the analytical results and verify the performance of the proposed converter, a 200-W test rig is implemented in the laboratory, shown in Fig. 6. As already mentioned in

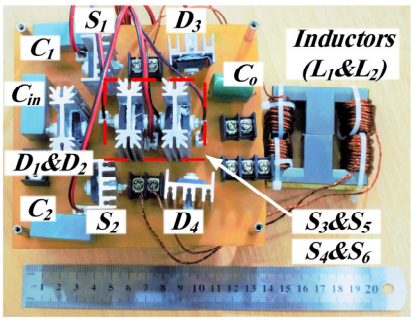

Fig. 6. Prototype of 200-W laboratory test rig.

previous sections, both inductors L_1 and L_2 share an EE ferrite core. The inductors are wound on the gapped side-limbs and the middle-limb is ungapped. The converter parameters are $L_1 = L_2 = 450$ µH, $C_{in} = C_o = 1$ µF, $C_1 = C_2 = 2.2$ µF and the switching frequency is 30 kHz. Also, the switches S_1-S_6 and the diodes D_1-D_4 are IXGH40N60C2/D1 and STTH60L06C, respectively. The experimental tests are performed in both buck and boost modes with the input voltages of 95 Vrms and 45 Vrms (f_{in} = 60Hz), respectively. The output voltage of 70 Vrms is desired for both modes of operation with the output load as $R_L = 24$ Ω. Both buck and boost operations are evaluated for three different output frequencies, such as 30Hz (step-down frequency), 60Hz (same frequency) and 120Hz (step-up frequency). Buck and boost waveforms are presented in Figs. 7 and 8, respectively. The excellent steady-state performance with highly sinusoidal input current and fully symmetrical output voltage waveforms are obvious. As an important evaluation, the quality of the input current waveforms is measured with the power factor (*PF*) and the total harmonic distortion (*THD*) using the FLUKE-435 power analyzer. The quality factors are summarized in Table II for different output frequencies and operation modes. According to this table, the power factor of the input current is close to one for all operating conditions. Also, its *THD*s are significantly lower than the standard limit of 5%. The harmonics content of the input current is also presented in Table III, which is far below the standard limits, e.g. the grid requirements by IEEE Std 519 [32]. In addition, the output voltage harmonics in Table III are found to be similar to that of the MC of [22].

With the proposed converter operating in the buck mode, the input voltage of 95 Vrms is decreased to 70 Vrms at the output side with $D = 0.43$, already calculated from (7). The input voltage (V_{in}), the output voltage (V_{out}), the input current (I_{in}), the output current (I_{out}), the voltage stresses across the semiconductors and the capacitors, and the inductors currents during buck operation mode with the output frequencies of 30Hz, 60Hz and 120Hz are depicted in Fig. 7(a), (b) and (c), respectively.

In addition, the input voltage 45 Vrms is properly increased to 70 Vrms at the output side when the proposed converter operates in the boost mode. This is achieved by setting $D = 0.61$, which is already calculated from (7). The waveforms for the boost mode are presented when the output frequency is 30Hz, 60Hz and 120Hz in Fig. 8(a), (b) and (c), respectively.

Clearly, for both modes of operation, the proposed converter can maintain its superior performance at different output frequencies. As already expected, the aforementioned results

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2019.2914644, IEEE Transactions on Industrial Electronics

TABLE II
INPUT CURRENT QUALITY FACTORS COMPARISON AMONG VARIOUS OUTPUT FREQUENCIES

Quality Factor	**Power Factor, *PF***						**Total Harmonic Distortion, *THD%***					
Output Frequency	**30Hz**		**60Hz**		**120Hz**		**30Hz**		**60Hz**		**120Hz**	
Operation Mode	Boost	Buck	Boost	Buck	Boost	Buck	Boost	Buck	Boost	Buck	Boost	Buck
Input Current, I_{in}	0.98	0.977	0.972	0.976	0.96	0.98	2.21%	2.5%	2%	2.1%	3.8%	4.5%

TABLE III
*THD*S AND LOW-ORDER HARMONICS CONTENT OF INPUT CURRENT AND OUTPUT VOLTAGE

Output Frequency	**30Hz**		**60Hz**		**120Hz**		**30Hz**		**60Hz**		**120Hz**	
Operation Mode	Boost	Buck	Boost	Buck	Boost	Buck	Boost	Buck	Boost	Buck	Boost	Buck
Harmonic Order	**Input Current Harmonics Amplitude (A)**						**Output Voltage Harmonics Amplitude (V)**					
1st	6.64	3.12	6.48	3.13	6.53	3.12	85	84.47	99.1	100	83.97	84.36
3rd	0.04	0.02	0.03	0.03	0.07	0.05	51.27	50.57	0.21	0.74	21.71	21.74
5th	0.04	0.02	0.03	0.03	0.06	0.06	12.44	11.99	0.23	1	13	12.83
7th	0.04	0.02	0.04	0.03	0.07	0.07	5.68	5.53	0.28	1.24	9.37	9.11
9th	0.04	0.02	0.04	0.03	0.06	0.06	3.57	3.18	0.34	1.3	7.26	7.06
THD%	2.21%	2.5%	2%	2.1%	3.8%	4.5%	62.74%	62.28%	2.67%	3.85%	62.76%	62.5%

evidently approve the theoretically developed operation principles of the switching devices. Obviously, the operation of the high-frequency switching-cells with respect to the input voltage half cycle is also confirmed. In addition, as seen from the zoomed view of the voltage stress waveforms in Figs. 7 and 8, the semiconductors turn ON and OFF without any noticeable voltage spikes, which was already expected. All experimental voltages and currents values are in good agreement with the calculated values from (8)-(15).

It should be noted that the quality of the output waveforms might not be adequate for those applications requiring high quality sinusoids, such as driving an induction motor. However, very high quality output waveforms can be easily achieved by modifying the switching strategy of Fig. 3. For instance, by using a simple sinusoidal PWM (SPWM) for the H-bridge circuit of the proposed converter (refer to Fig. 2), the generated output current can be a highly sinusoidal waveform at the price of added complexity and switching losses.

The efficiency of the proposed converter is shown in Fig. 9(a) along with that of the MC of [22], for different input voltages ranging from 45 Vrms to 95 Vrms. Also, the efficiency comparison at different output powers is plotted in Fig. 9(b). It should be noted that the successful MC of [22] is chosen for the efficiency comparison due to its highest efficient operation compared to other former MCs. Both the efficiency curves of Fig. 9(a) are plotted for the same output power of 200-W while it varies from 75-W to 250-W for the efficiency cureves of Fig. 9(b) when the proposed converter operates under both buck and boost modes (45 Vrms and 95 Vrms input voltage supply, respectively). The output voltage of 70 Vrms is kept constant for all efficiency curves of Fig. 9(a) and (b). It is seen that the efficiency of the proposed converter is considerably higher than that of the MC of [22] for a wide range of input voltage and output power. The lower number of conducting semiconductors at any time, the lower number of high-frequency switches, eliminating voltage spikes across the switches, inherent commutation capability without any dead/overlap time for switchings are the main reasons of lower power loss of the proposed converter. It should be noted that the peak efficiency of the proposed converter is 92.8% when V_{in} = 95 Vrms, where it operates in the buck mode. The efficiency comparison results were already expected from the comparative analysis presented in section III based on peak and average *SDP* comparison of Fig. 5.

The distribution of power loss in operation modes of buck and boost is calculated for the proposed converter using the same procedure as [33]–[35] and the results are plotted in Fig. 9(c). The total power losses are almost 15.5 W and 30.7 W for the buck and the boost modes, respectively. In the buck mode, the highest power loss is the losses in the low-frequency switches S_3 to S_6 (4.73 W). In the boost mode, the highest power loss occurs in the low-frequency diodes D_1 and D_2. Each of these diodes carries one half cycle of the input current. As obvious from Fig. 9(c), the total power losses of the low frequency switches S_3 to S_6 in both buck and boost modes are the same. Assuming a same output voltage and power, the load currents of the proposed converter are the same in both buck and boost modes. Thus, a same current flows through the low frequency switches S_3 to S_6 in both these modes and then a same total power loss is expected for the low frequency switches S_3 to S_6 in both buck and boost modes. This is confirmed through the results of Fig. 9(c).

V. CONCLUSION

This paper proposes a novel single-phase buck-boost variable-frequency AC-AC converter offering a higher efficiency compared to its competitors. Also, this converter employs a lower number of diodes and high-frequency switches in addition to lower total ratings for all semiconductors defined by the known parameter of *SDP*. Moreover, effective employment of two parallel capacitors allows a smooth and quasi-continuous input current waveform that eliminates the

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2019.2914644, IEEE Transactions on Industrial Electronics

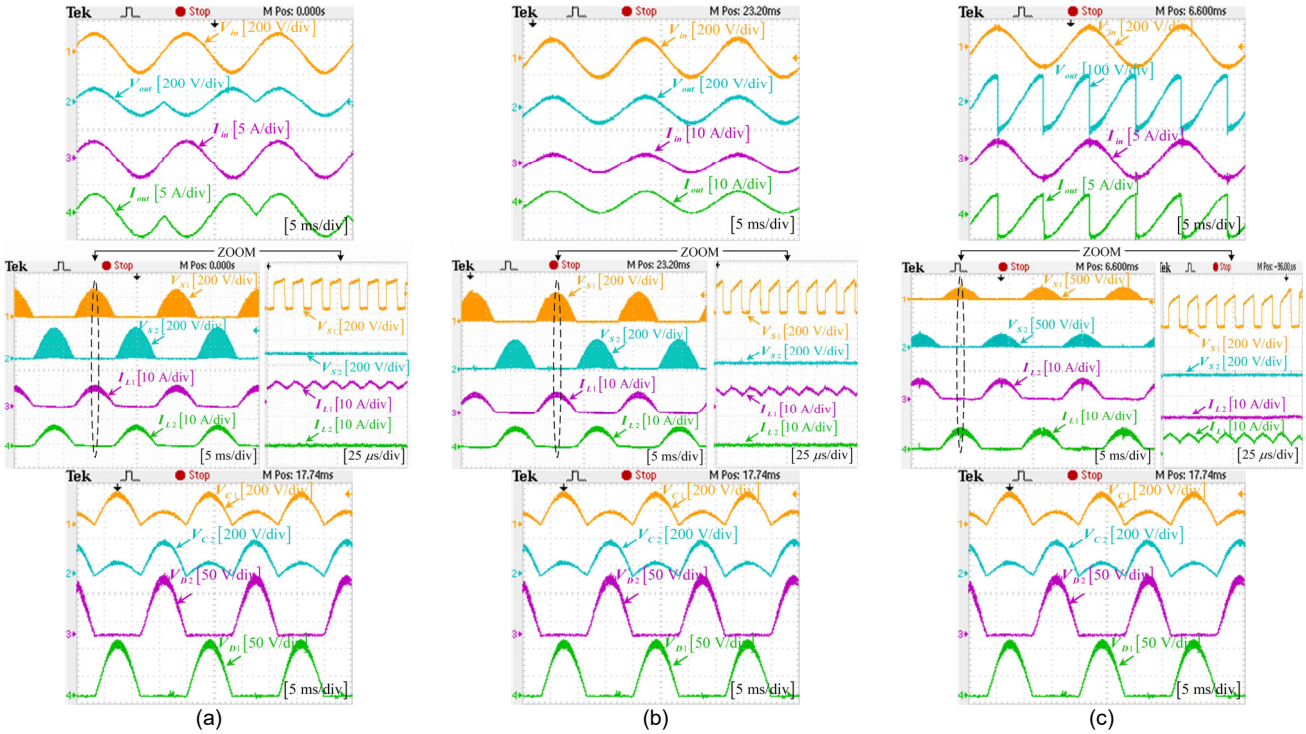

Fig. 7. Buck operation mode waveforms: input and output waveforms, blocked voltages by S_1 and S_2, inductors currents, voltages across capacitors and inversed voltages across diodes D_1 and D_2 with output frequency of (a) 30Hz, (b) 60Hz, and (c) 120Hz.

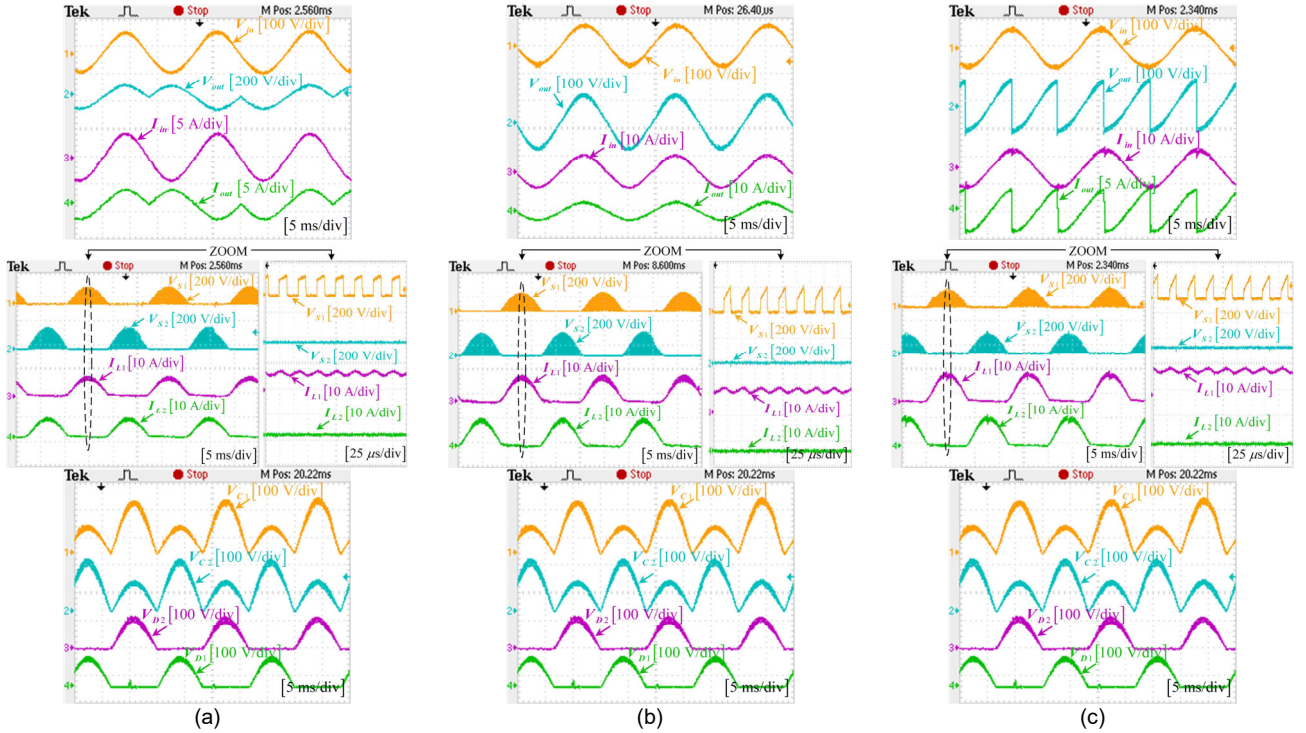

Fig. 8. Boost operation mode waveforms: input and output waveforms, blocked voltages by S_1 and S_2, inductors currents, voltages across capacitors and inversed voltages across diodes D_1 and D_2 with output frequency of (a) 30Hz, (b) 60Hz, and (c) 120Hz.

need for a bulky input filter inductor. Also, these capacitors provide a safe commutation path for the inductors currents, which removes the need for turn-OFF delay for the switches or any soft commutation strategy. The theoretical achievements are confirmed through extensive tests on a 200-W converter and for three different output frequencies including 30Hz, 60Hz and 120Hz.

REFERENCES

[1] A. A. Khan, H. Cha, J. W. Baek, J. Kim, and J. Cho, "Cascaded Dual-Buck AC-AC Converter with Reduced Number of Inductors," *IEEE*

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2019.2914644, IEEE Transactions on Industrial Electronics

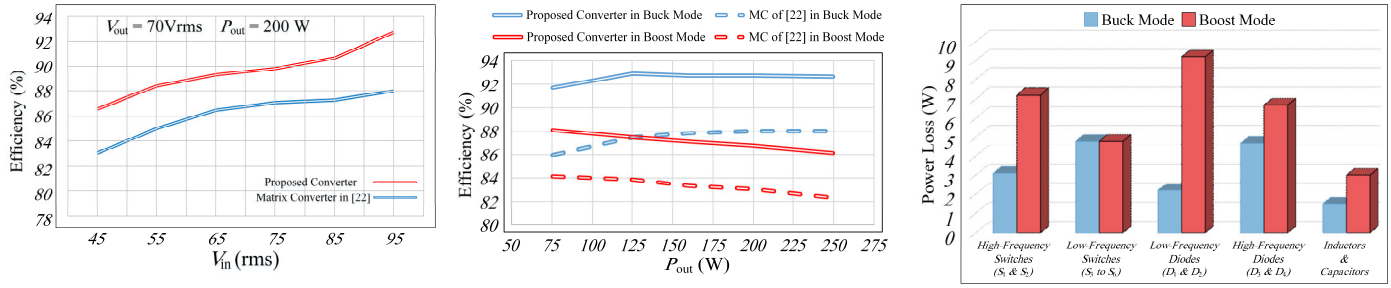

Fig. 9. Efficiency comparison of proposed converter (a) for various input voltage, (b) for various output power and (c) power loss distribution among components.

Trans. Power Electron., vol. 32, no. 10, pp. 7509–7520, 2017.

[2] A. A. Khan, H. Cha, and H. F. Ahmed, "High-efficiency single-phase AC-AC converters without commutation problem," *IEEE Trans. Power Electron.*, vol. 31, no. 8, pp. 5655–5665, 2016.

[3] A. A. Khan, H. Cha, H. F. Ahmed, J. Kim, and J. Cho, "A Highly Reliable and High-Efficiency Quasi Single-Stage Buck–Boost Inverter," *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4185–4198, Jun. 2017.

[4] S. Kim, H. G. Kim, and H. Cha, "Dynamic Voltage Restorer Using Switching Cell Structured Multilevel AC-AC Converter," *IEEE Trans. Power Electron.*, vol. 32, no. 11, pp. 8406–8418, 2017.

[5] X. P. Fang, Z. M. Qian, and F. Z. Peng, "Single-Phase Z-Source PWM AC-AC Converters," *IEEE Power Electron. Lett.*, vol. 3, no. 4, pp. 121–124, 2005.

[6] S. Sharifi, F. Jahani, and M. Monfared, "Direct Single Phase AC-AC Converters Based on Series Impedance Networks," *IEEE Trans. Power Electron.*, vol. 33, no. 12, pp. 10380–10389, 2018.

[7] O. Cipriano da Silva Filho, B. R. de Almeida, D. de S. Oliveira, and T. R. Fernandes Neto, "High-Frequency Isolated AC-DC-AC Interleaved Converter for Power Quality Applications," *IEEE Trans. Ind. Appl.*, vol. 9994, no. c, 2018.

[8] M. A. M. Albreem, H. T. A. Naser, and M. E. A. Abofares, "Design of indirect AC-AC converter based on linear controller for power systems," in *2016 International Conference on Advances in Electrical, Electronic and Systems Engineering (ICAEES)*, 2016, pp. 500–505.

[9] D. Lee and Y. Kim, "Control of Single-Phase-to-Three-Phase AC / DC / AC PWM Converters for Induction Motor Drives," vol. 54, no. 2, pp. 797–804, 2007.

[10] P. Alemi, Y. C. Jeung, and D. C. Lee, "DC-Link capacitance minimization in t-type three-level AC/DC/AC PWM converters," *IEEE Trans. Ind. Electron.*, vol. 62, no. 3, pp. 1382–1391, 2015.

[11] T. Friedli, J. W. Kolar, J. Rodriguez, and P. W. Wheeler, "Comparative evaluation of three-phase AC-AC matrix converter and voltage DC-link back-to-back converter systems," *IEEE Trans. Ind. Electron.*, vol. 59, no. 12, pp. 4487–4510, 2012.

[12] O. Ellabban, H. Abu-Rub, and S. Bayhan, "Z-Source Matrix Converter: An Overview," *IEEE Trans. Power Electron.*, vol. 31, no. 11, pp. 7436–7450, 2016.

[13] Y. Sun, X. Li, M. Su, H. Wang, H. Dan, and W. Xiong, "Indirect matrix converter-based topology and modulation schemes for enhancing input reactive power capability," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 4669–4681, 2015.

[14] C. P. W. M. Method, T. D. Nguyen, H. Lee, and S. Member, "Dual Three-Phase Indirect Matrix Converter With," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 569–581, 2014.

[15] S. Sünter and Ö. Aydoğmuş, "Implementation of a single-phase matrix converter induction motor drive," *Electr. Eng.*, vol. 90, no. 6, pp. 425–433, Jun. 2008.

[16] N. Nguyen-Quang, D. A. Stone, C. M. Bingham, and M. P. Foster, "Single phase matrix converter for radio frequency induction heating," *Int. Symp. Power Electron. Electr. Drives, Autom. Motion, 2006. SPEEDAM 2006.*, vol. 2006, pp. 614–618, 2006.

[17] R. Cardenas, R. Pena, P. Wheeler, J. Clare, and G. Asher, "Control of the Reactive Power Supplied by a WECS Based on an Induction Generator Fed by a Matrix Converter," *IEEE Trans. Ind. Electron.*, vol. 56, no. 2, pp. 429–438, Feb. 2009.

[18] A. Zuckerberger, D. Weinstock, and A. Alexandrovitz, "Single-phase matrix converter," *IEE Proc. - Electr. Power Appl.*, vol. 144, no. 4, p. 235, 1997.

[19] Z. Idris, M. K. Hamzah, and M. F. Saidon, "Implementation of Single-Phase Matrix Converter as a Direct AC-AC Converter with Commutation Strategies," in *37th IEEE Power Electronics Specialists Conference*, 2006, pp. 1–7.

[20] C.-M. Young, H.-L. Chen, and M.-H. Chen, "A Cockcroft–Walton Voltage Multiplier Fed by a Three-Phase-to-Single-Phase Matrix Converter With PFC," *IEEE Trans. Ind. Appl.*, vol. 50, no. 3, pp. 1994–2004, May 2014.

[21] M. K. Nguyen, Y. G. Jung, Y. C. Lim, and Y. M. Kim, "A single-phase Z-source buckboost matrix converter," *IEEE Trans. Power Electron.*, vol. 25, no. 2, pp. 453–462, 2010.

[22] H. F. Ahmed, H. Cha, A. A. Khan, J. Kim, and J. Cho, "A single-phase buck-boost matrix converter with only six switches and without commutation problem," *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 1232–1244, 2017.

[23] D. A. Stone, C. M. Bingham, M. P. Foster, M. Street, and S. Sheffield, "Comparison of single-phase matrix converter and H-bridge converter for radio frequency induction heating," *Power Electron. Appl. 2007 Eur. Conf.*, pp. 1–9, 2007.

[24] C.-M. Young, M.-H. Chen, S.-H. Yeh, and K.-H. Yuo, "A Single-Phase Single-Stage High Step-Up AC–DC Matrix Converter Based on Cockcroft–Walton Voltage Multiplier With PFC," *IEEE Trans. Power Electron.*, vol. 27, no. 12, pp. 4894–4905, Dec. 2012.

[25] P. Drabek, Z. Peroutka, M. Pittermann, and M. Cedl, "New Configuration of Traction Converter With Medium-Frequency Transformer Using Matrix Converters," *IEEE Trans. Ind. Electron.*, vol. 58, no. 11, pp. 5041–5048, Nov. 2011.

[26] R. Barrera-Cardenas and M. Molinas, "Comparative Study of Wind Turbine Power Converters Based on Medium-Frequency AC-Link for Offshore DC-Grids," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 3, no. 2, pp. 525–541, Jun. 2015.

[27] J. Perez, V. Cardenas, L. Moran, and C. Nunez, "Single-Phase AC-AC Converter Operating as a Dynamic Voltage Restorer (DVR)," in *IECON 2006 - 32nd Annual Conference on IEEE Industrial Electronics*, 2006, pp. 1938–1943.

[28] D. Barater, C. Concari, G. Franceschini, and G. Buticchi, "Single-Phase Series Active Power Filter with Transformer-Coupled Matrix Converter," *IET Power Electron.*, vol. 9, no. 6, pp. 1279–1289, May 2016.

[29] A. A. Khan, H. Cha, and H. F. Ahmed, "An Improved Single-Phase Direct PWM Inverting Buck-Boost AC-AC Converter," *IEEE Trans. Ind. Electron.*, vol. 63, no. 9, pp. 5384–5393, 2016.

[30] H.-H. Shin, H. Cha, H.-G. Kim, and D.-W. Yoo, "Novel Single-Phase PWM AC–AC Converters Solving Commutation Problem Using Switching Cell Structure and Coupled Inductor," *IEEE Trans. Power Electron.*, vol. 30, no. 4, pp. 2137–2147, Apr. 2015.

[31] M. Shen, A. Joseph, J. Wang, F. Z. Peng, and D. J. Adams, "Comparison of traditional inverters and Z-source inverter for fuel cell vehicles," in *Power Electronics in Transportation (IEEE Cat. No.04TH8756)*, 2004, pp. 125–132.

[32] IEEE Power and Energy Society, "IEEE Recommended Practice and Requirements for Harmonic Control in Electric Power Systems," *IEEE Std. 519-2014*. Mar. 27, 2014.

[33] D. Graovac and M. Pürschel, "IGBT Power Losses Calculation U sing the Data-Sheet Parameters." Infineon, App. Note, Jan. 2009.

[34] R. W. Erickson and D. Maksimovic, *Fundamentals of Power*

Electronics. Boston, MA, USA: Springer, 2001.

[35] C. W. Mclyman, *Transformer and Inductor Design Handbook*. Boca Raton, FL, USA: CRC Press, 2011.

Saeed Sharifi received both B.Sc. and M.Sc. degrees (with honors) in electrical engineering from Ferdowsi University of Mashhad, Iran, in 2015 and 2018, respectively in power electronics.

His research interests include power electronic converters, especially impedance networks, high order passive filters, grid connected converters, and AC-AC converters.

Mohammad Monfared (S'07–M'10-SM'15) received the B.Sc. degree in electrical engineering from Ferdowsi University of Mashhad, Iran, in 2004, and the M.Sc. and Ph.D. degrees (both with honors) in electrical engineering from Amirkabir University of Technology, Tehran, Iran, in 2006 and 2010, respectively.

He is currently an Associate Professor at Ferdowsi University of Mashhad, Iran, where he has received the Best Researcher Award in 2015. His research interests include power electronics, renewable energy systems, and power quality.

Mohammad Babaei received both B.Sc. and M.Sc. degrees in electrical engineering from Ferdowsi University of Mashhad, Iran, in 2016 and 2019, respectively in power electronics.

His research interests include power electronic converters, especially rectifiers, impedance networks, AC-AC converters, and renewable energy systems.

Alireza Pourfaraj was born in 1994. He received the B.Sc. and the M.Sc. degrees in electrical engineering from Ferdowsi University of Mashhad, Iran, in 2016 and 2018, respectively.

His research interests include power electronic converters, especially grid connected inverters, impedance networks, and AC-AC converters.