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# A Theory to Synthesize Non-isolated DC-DC Converters using Flux Balance Principle

Soumya Shubhra. Nag, *Member, IEEE*, Ramanuja Panigrahi, *Student Member, IEEE*, Santanu K. Mishra, *Senior Member, IEEE*, Avinash Joshi, Khai D. T. Ngo, *Fellow, IEEE*, Suman Mandal

***Abstract*- The paper describes a theory to synthesize non-isolated DC-DC converters. It uses the fundamental flux balance equation across the inductors of a converter as a starting point in this synthesis process. The flux balance equations are the linear equations of the input voltage, capacitor voltages and duty cycle (D). The coefficients of these linear equations can be selected from a finite set of choices. These choices define the converter topologies which are subsequently used to synthesize a converter. The synthesis procedure applies to a converter of multiple order. All the possible converters are identified for a first order topology. In the case of second-order converters, all the choices of the flux balance equation are defined. Based on these choices three new quadratic topologies are derived and verified to demonstrate the effectiveness of the theory. The procedure to synthesize a converter from a given voltage conversion ratio is also outlined.**

***Index Terms*— DC-DC converters, Synthesis of converter, Flux Balance equation**

## I. INTRODUCTION

Non-isolated DC-DC converters are the basic building blocks for power processing in renewable applications, data centers, and various consumer electronics devices, etc. Buck, Boost, and Buck-boost topologies are the three major topologies which are manipulated to obtain other non-isolated topologies [1-17]. With increasing novel areas of application, there is a need to look for DC-DC converters with a given voltage conversion characteristic. For example, quadratic buck (Q buck) converter provides a very low output to input conversion ratio at a relatively higher duty-cycle [12-13], which makes it suitable for bias voltage derivation when input DC is very high. Mostly, converter topologies are invented intuitively or by combining the existing basic topologies of buck, boost, and buck-boost converter. However, a systematic procedure to synthesize a converter topology from the required voltage conversion ratio is scarce. This paper presents a thorough review of the prior attempts to generalize DC-DC converter synthesis process and subsequently proposes a method to synthesize the exhaustive set of DC-DC converters of a given order.

While many DC-DC converters have been invented over the past few decades, there has been a constant drive among the researchers to find a unifying link among the different DC-DC converter topologies and find a generalized converter synthesis theory. Many such approaches such as graph-theoretic approach with duality principle [1], [2], converter switching cell theory [3], [4], [5], [6], analytical synthesis theory [7], [8], and converter synthesis with layer and graft schemes [9-11], etc., are presented in the literature. The graph-theoretic approach was used in [1] to establish a relation between basic Pulse Width Modulated (PWM) converters [1-7, 18-22]. With the help of the duality principle, new current source and voltage source PWM converter topologies were developed. Transformer isolated Cuk and SEPIC topologies were also discussed in [2]. Converter switching cell-based converter synthesis theory was proposed in [3], [4]. A converter switching cell was viewed as a three port network consisting of switches, inductors, and a capacitor which had a DC source at the input port and the load bypassed by a capacitor at the output port. The input and the load is assumed to share a common reference point or ground.

Several new converter topologies were presented in [4] using different converter cells with two inductors and one capacitor. Although new converter structures were unveiled, it did not present any comprehensive converter synthesis procedure. Synthesis of PWM converter based on the inductor flux balance and capacitor charge balance equations is presented in [7]. An extension of the method in [7] is presented in [8], where the matrix representation of converters was used to synthesize different converters. However, several converter topologies were degenerated in [7], [8] which can be used to simplify converter operation and to construct new topologies.

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Soumya S. Nag is with the Department of Electrical Engineering at Indian Institute of Technology Delhi, New Delhi, India. (e-mail: ssnag@ee.iitd.ac.in).

Ramanuja Panigrahi, Santanu K. Mishra, and Avinash Joshi are with the Department of Electrical Engineering, Indian Institute of Technology Kanpur, Kanpur, 208016, India (e-mail: ramanuja@iitk.ac.in; santanum@iitk.ac.in; ajoshi@iitk.ac.in).

Khai D. T. Ngo is with the Center for Power Electronics Systems, Virginia Polytechnic Institute and State University, Blacksburg, VA 24061, USA (e-mail: kdtn@vt.edu).

Suman Mandal is with the Department of Electrical Engineering at Indian Institute of Technology Bombay, Mumbai, India. (e-mail: sumaniitb29@gmail.com).

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The graft theory proposed in [9-11] deals with the formation of single stage converters from two cascaded single stage converters. The power stages are cascaded to achieve multiple functionalities. Then the switches and energy storage elements are merged to reduce the component count. Afterwards, the number of switches is further reduced based on the applications.

The analytical converter synthesis method, presented in [7], studied different converter structures by exploring the circuit equations evolving from different repetitively-switched linear networks. In [7], the converter voltage loop equations (KVL) and current branch equations (KCL) are written for the two repeating switching states which are used to form flux balance equation and charge balance equation. The flux balance and charge balance equations are characterized by a number of parameters ($F_{cl}$, $F_{cr}$, $F_{gl}$, $F_{gr}$), each of which can be +1, 0 or -1. These parameters determine the interconnection among the passive elements with the input source and load at the output in each switching state. The load is assumed to be always bypassed by a capacitor. Thus, a range of converter topologies can be found by exploring the possible combinations of the parameters $F_{cl}$, $F_{cr}$, $F_{gl}$, $F_{gr}$. This converter synthesis procedure involves complex procedure including the formation of network graphs, cut-sets, etc., in order to form a set of realizable converters. This method involves a large number of computations (matrix operations). Hence, the extension of this method to a second or higher order converter is not very straightforward. Different methods [23-27] are reported in the literature to analyze and model DC-DC converters.

In this paper, a synthesis method is proposed which directly uses the principle of inductor volt-sec balance [28]. The inductor volt-sec balance is described by a linear algebraic equation in voltage across each inductor ($V_{Li}$) during the operating intervals of a switching cycle. The coefficients of the equation, integers from the set {-1, 0, 1}, are selected to obtain the required voltage conversion ratio. The procedure to synthesize a topology from a specific voltage conversion ratio is also outlined.

The paper starts with the assumptions and generalized synthesis steps, stated in section II. Section III presents the general flux balance equations of an inductor in a converter. Section IV presents the application of the theory given in Section III to synthesize first order converters. Various constraints in the process of synthesis are outlined, and examples are discussed to illustrate the concepts. Section V explains the steps to synthesize second order converters. In this section, the synthesis steps are outlined on how to obtain new converter topologies from a given voltage conversion equation. This procedure is used to discover three new quadratic buck (Q buck), boost (Q boost), and buck-boost (Q buck-boost) topologies. The synthesis procedure can be extended to obtain other topologies from any given voltage conversion equation.

## II. Fundamental Assumptions

The proposed converter synthesis method is based on the following assumptions:

1) The circuit elements of the converter are considered to be ideal.
2) The capacitor voltages are assumed to be constant under steady-state.
3) The inductor currents are continuous and are positive in a switching cycle, i.e., continuous conduction mode (CCM) is assumed.
4) There is a single input DC source.
5) The converter output voltage is a function of variables duty-cycle ($D$) and the input voltage ($V_{in}$). The output voltage is load independent. It is important to note that, this condition is true when the converter topology has an equal number of inductors and capacitors [2]. In other words, when the number of inductors and the number of capacitors in a converter is not equal, the output voltage becomes load dependent.

## III. Inductor Voltage Equation

The desired converter configuration has a certain number of inductor-capacitor pairs, which in turn defines the order of the converter. The steady state voltage across an inductor over a switching cycle is zero. Under CCM operation, the switching cycle is divided into two intervals, $D.T_s$ and $D'.T_s$, where $D'= (1-D)$. $D$ is commonly known as the duty cycle of a converter. Furthermore, assuming switching frequency is much higher compared to the $LC$ resonant frequency, the voltages across the capacitors are a constant during the switching period. Assuming the inductor to be ideal, the voltage across the inductor is a linear function of the input voltage ($V_{in}$) and capacitor voltages ($V_{C1}$, $V_{C2}$, …., etc.). Thus, the volt-sec balance equation for the $i^{th}$ inductor of an $n^{th}$ order converter is given by (1).

In (1), each coefficient $\alpha_{ij}$ and $\beta_{ij}$ can only have integer values from the set {0, 1, -1}. This corresponds to the absence or presence of $V_{in}$ and a given capacitor voltage, with a particular polarity, across the inductor. $\alpha$ represents the connections of the inductor in $D$ interval, and $\beta$ represents the connections in $D'$ interval. The subscripts '$i$' represents the inductor number and '$j$' represents connections with respect to voltages, i.e., $j$ = o means relation with $V_{in}$ and $j$ = 1 means relation with $V_{C1}$, and so on. The value of $\alpha$ and $\beta$ are limited to {0, ±1}. 0 means no connection. ±1 signifies the voltage is connected across the inductor in the same/ opposite polarity as the reference. (1) can be written in the matrix form as shown in (2).

As each of the coefficient $\alpha_{ij}$ and $\beta_{ij}$ can take one of the values from the set {0, 1, -1}, it can be seen that there are a large number of possible matrices and hence the corresponding converters. (2) can be rewritten as

$$[C]_{n\times n}.[V_C]_{n\times 1} = -[C_{i0}]_{n\times 1}.V_{in}$$

Therefore, by matrix inversion

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$$\langle v_{L_i} \rangle_{T_s} = \left(\alpha_{i0}.V_{in} + \alpha_{i1}.V_{C1} \ldots \alpha_{ij}.V_{cj} + \cdots + \alpha_{in}.V_{Cn}\right).D + \left(\beta_{i0}.V_{in} + \beta_{i1}.V_{C1} \ldots + \beta_{ij}.V_{Cj} \ldots + \beta_{in}.V_{Cn}\right).D' = 0 \quad (1)$$

Where,

$$i = 1,2,3 \ldots . n \ \& \ j = 0,1,2,3 \ldots . n$$

$$\begin{bmatrix} {C_{11}}^T.D_t & {C_{12}}^T.D_t & \ldots & {C_{1j}}^T.D_t & \ldots & {C_{1n}}^T.D_t \\ {C_{21}}^T.D_t & {C_{22}}^T.D_t & \ldots & {C_{2j}}^T.D_t & \ldots & {C_{2n}}^T.D_t \\ \vdots & \vdots & & \vdots & & \vdots \\ {C_{i1}}^T.D_t & {C_{i2}}^T.D_t & \ldots & {C_{ij}}^T.D_t & \ldots & {C_{in}}^T.D_t \\ \vdots & \vdots & & \vdots & & \vdots \\ {C_{n1}}^T.D_t & {C_{n2}}^T.D_t & \ldots & {C_{nj}}^T.D_t & \ldots & {C_{nn}}^T.D_t \end{bmatrix} \cdot \begin{bmatrix} V_{C1} \\ V_{C2} \\ \vdots \\ V_{Ci} \\ \vdots \\ V_{Cn} \end{bmatrix} = - \begin{bmatrix} {C_{10}}^T.D_t \\ {C_{20}}^T.D_t \\ \vdots \\ {C_{i0}}^T.D_t \\ \vdots \\ {C_{n0}}^T.D_t \end{bmatrix} . V_{in} \quad (2)$$

Where,

$$C_{ij} = \begin{bmatrix} \alpha_{ij} \\ \beta_{ij} \end{bmatrix} D_t = \begin{bmatrix} D \\ D' \end{bmatrix} \ i = 1,2,3 \ldots . n \ \& \ j = 0,1,2,3 \ldots . n$$

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$$[V_C]_{n\times 1} = {[C]^{-1}}_{n\times n}\{-[C_{i0}]_{n\times 1}\} \times V_{in}$$

$$\Longrightarrow [V_C]_{n\times 1} = \frac{1}{\Delta} \begin{bmatrix} P_{11} & P_{12} & \ldots & P_{1j} & \ldots & P_{1n} \\ P_{21} & P_{22} & \ldots & P_{2j} & \ldots & P_{2n} \\ \vdots & \vdots & & \vdots & & \vdots \\ P_{i1} & P_{i2} & \ldots & P_{ij} & \ldots & P_{in} \\ \vdots & \vdots & & \vdots & & \vdots \\ P_{n1} & P_{n2} & \ldots & P_{nj} & \ldots & P_{nn} \end{bmatrix} \cdot \begin{bmatrix} {C_{10}}^T.D_t \\ {C_{20}}^T.D_t \\ \vdots \\ {C_{i0}}^T.D_t \\ \vdots \\ {C_{n0}}^T.D_t \end{bmatrix} . V_{in}$$

Where, $P_{ij}$ is a polynomial of order n-1, and the determinant ($\Delta$) is an n[th] order polynomial in $D$.

From this equation $[V_{Ci}]$ is given by

$$[V_{Ci}] = \frac{V_{in}}{\Delta} \times \sum_{j=1}^{n} P_{ij} \left({C_{j0}}^T.D_t\right)$$

$$\Longrightarrow [V_{Cn}] = \frac{V_{in}}{\Delta} \times \sum_{j=1}^{n} P_{nj} \left({C_{j0}}^T.D_t\right)$$

Hence, the voltage gain $G_n(D)$ can be represented as

$$G_n(D) = \frac{V_{Cn}}{V_{in}} = \frac{\sum_{j=1}^{n} P_{nj} \left({C_{j0}}^T.D_t\right)}{\Delta} = \frac{\sum_{i=0}^{n} A_i D^i}{\sum_{i=0}^{n} B_i D^i}$$

## IV. First-Order Converters

### A. Gain Derivation

The first order converters have been defined as converters having only one $LC$ pair and one input voltage ($V_{in}$). Hence, the output is taken across the only voltage stiff element, apart from the input, present in the circuit, i.e., $V_{C1}$. The converter gain ($G = V_{C1}/V_{in}$) is a ratio of two first-order polynomials in $D$. Using (2), the general form of the volt-sec equation in matrix form is given by

$$\left({C_{11}}^T.D_t\right).V_{C1} = -\left({C_{10}}^T.D_t\right).V_{in}$$

Where,

$$C_{11}^T = [\alpha_{11}\ \beta_{11}], and\ C_{10}^T = [\alpha_{10}\ \beta_{10}] \quad (3)$$

Therefore, (3) can be expanded as

$$(\alpha_{11}D + \beta_{11}D')V_{C1} + (\alpha_{10}D + \beta_{10}D')V_{in} = 0 \quad (4\text{ a})$$

The voltage across the inductor in each interval is as follows

$$v_L = \begin{cases} \alpha_{11}V_{C1} + \alpha_{10}V_{in}, & in\ D\ interval \\ \beta_{11}V_{C1} + \beta_{10}V_{in}, & in\ D'\ interval \end{cases} \quad (4\text{ b})$$

The converter gain $G$ is given by

$$G = \frac{V_{C1}}{V_{in}} = -\frac{{C_{10}}^T.D_t}{{C_{11}}^T.D_t} = -\frac{\alpha_{10}.D + \beta_{10}.D'}{\alpha_{11}.D + \beta_{11}.D'}, \quad (5)$$

Where $D'$=*1-D*.

For example, in the conventional boost converter, shown in Fig. 1(a), $\begin{bmatrix} \alpha_{10} \\ \alpha_{11} \end{bmatrix} = \begin{bmatrix} 1 \\ 0 \end{bmatrix}, \begin{bmatrix} \beta_{10} \\ \beta_{11} \end{bmatrix} = \begin{bmatrix} 1 \\ -1 \end{bmatrix}$, and gain$(G) = \frac{V_{C1}}{V_{in}} = \frac{1}{1-D}$.

The following observations can be made using (5)

i. If the coefficients *($\alpha_{10}$, $\beta_{10}$)* and/ or *($\alpha_{11}$, $\beta_{11}$)* are zero, the gain ($G$) reduces to an invalid form. Therefore, this choice of coefficients is not used.
ii. If $\beta_{10} = \alpha_{10}$ and $\beta_{11} = \alpha_{11}$, $G = (-\alpha_{10}/\alpha_{11})$, which makes it independent of duty cycle $D$. As the control variable is lost, this is not a valid choice for a power converter.
iii. If $\beta_{10} = -\alpha_{10}$ and $\beta_{11} = -\alpha_{11}$, $G = (-\alpha_{10}/\alpha_{11})$, which makes it independent of duty cycle $D$. As the control variable is lost, this is not a valid choice for a power converter.
iv. If all the four coefficients are negated, simultaneously, $G$ remains unchanged.

Therefore, the following restriction can be imposed on the choice of coefficients in (4a) for the volt-sec equation of a first order converter.

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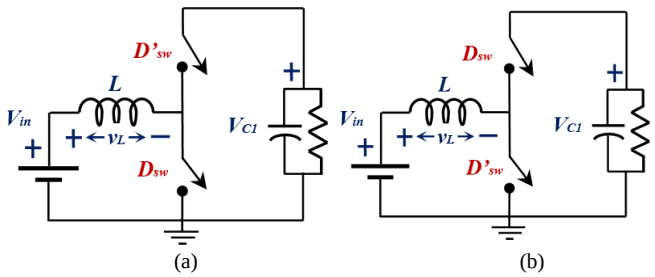


Fig. 1. Example of Complementary Topologies: (a) Conventional Boost converter, and (b) Complementary Boost converter (C-Boost).

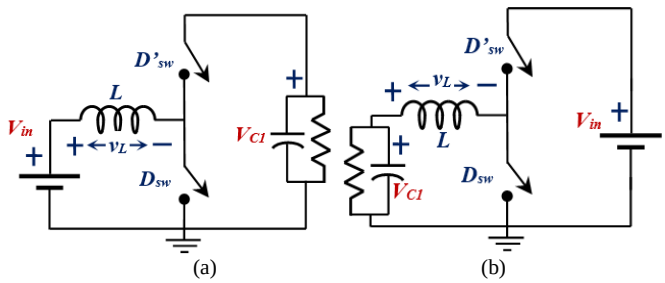


Fig. 2. Example of Inverse Topologies: (a) Conventional boost converter (b) Inverse boost converter (I- Boost).

$$\begin{bmatrix}\alpha_{10}\\ \alpha_{11}\end{bmatrix} \neq \pm\begin{bmatrix}\beta_{10}\\ \beta_{11}\end{bmatrix} \tag{6}$$

### B. *Complementary Converters*

Complementary topology *(C-topology)* is obtained by exchanging entire vectors $\alpha$ and $\beta$. This effectively leads to the same converter topology with $D$ and $D'$ (= *1-D*) control signals interchanged. The general form of voltage conversion equation is given by

$$G = \frac{V_{C1}}{V_{in}} = -\left[\frac{\beta_{10}.D + \alpha_{10}.D'}{\beta_{11}.D + \alpha_{11}.D'}\right]$$

As it can be noted, for the first-order converters exchanging $D$ and $D'$ amounts to exchanging values of $\alpha_{10}$ with $\beta_{10}$ and $\alpha_{11}$ with $\beta_{11}$.

For example, a conventional boost converter has a voltage conversion ratio equal to $V_o = \frac{V_{in}}{1-D}$. A complementary boost converter (*C-Boost*) has a conversion ratio $V_o = \frac{V_{in}}{D}$. Both the topologies are shown in Fig. 1.

### C. *Inversion of Gain*

If the values of $C_{10}^T = [\alpha_{10}, \beta_{10}]$ and $C_{11}^T = [\alpha_{11}, \beta_{11}]$ are interchanged, the expression of the voltage gain ($G$) is inverted and leads to inverted topology (*I-topology*). This leads to exchange the values of $\alpha_{10}$ with $\alpha_{11}$ and the values of $\beta_{10}$ with $\beta_{11}$. From an implementation perspective, this operation means that the input and output of the converter are interchanged without any change in the topology or control inputs.

For example, for a boost converter, the corresponding coefficient in (5) are $C_{10}^T = [1, 0]$, and $C_{11}^T = [1, -1]$. On the contrary, for the Inverted boost converter (*I-boost*) the corresponding coefficient in (5) are $C_{10}^T = [1, -1]$, and $C_{11}^T = [1, 0]$. This is equivalent to exchanging the input and output of the converter without any change to the control as shown in Fig. 2.

### D. *Achieving Negative Gain*

Keeping the definition of gain as before, $G = \frac{V_{C1}}{V_{in}}$, If the input voltage is inverted to $-V_{in}$, the output becomes negative. This can be viewed as a negative gain. This is the easiest way to achieve negative gain without changing the converter structure. Thus, changing the polarity of the input voltage is the most straight forward way to achieve negative gain.

### E. *Total Number of 1st order converters*

Based on (5), the coefficients ($\alpha_{10}$ and $\alpha_{11}$) and ($\beta_{10}$ and $\beta_{11}$) are chosen from a set {0, -1, 1}. However, the choice of [0, 0] is prohibited. Therefore, $3^2$-1=8 choices exist for each vector $C_{10}$ and $C_{11}$. Therefore, $8^2$=64 different gain expressions are possible. However, the constraints $\alpha_{10} \neq \pm\beta_{10}$ *and* $\alpha_{11} = \pm\beta_{11}$ restrict the total number of gain expression to 8×(8-2) =48.

Table I summarizes the converter configurations and their gains for all possible choices of ($\alpha_{10}$, $\alpha_{11}$) and ($\beta_{10}$, $\beta_{11}$). The values of variables ($\alpha_{10}$, $\alpha_{11}$) and ($\beta_{10}$, $\beta_{11}$) are listed in the top row and left column, respectively. For a particular combination of ($\alpha_{10}$, $\alpha_{11}$) and ($\beta_{10}$, $\beta_{11}$) values, the voltage across the inductor (from (4b)), and the converter gain ($G$) (from (5)) are tabulated. 4(b) gives the voltage across the inductor in $D$ and $D'$ intervals. For each value of ($\alpha_{10}$, $\alpha_{11}$) the voltage across the inductor in D interval is shown at the top of the table. Similarly, the voltages in the $D'$ interval are shown at the left side of the table for each of the values of ($\beta_{10}$, $\beta_{11}$). A combination of ($\alpha_{10}$, $\alpha_{11}$) and ($\beta_{10}$, $\beta_{11}$) values gives the converter gain as per (5). These are shown in the corresponding cells of the table. The prohibited choices are shown as hatched squares. As several first-order converter configurations are well known, the names of the converters and their variants are also indicated. The complementary, negative, and inverse gains are indicated by prefixes *C*, *N*, and *I*, respectively.

### F. *Synthesizing a Converter from its Voltage Conversion Equation*

The procedure to go from a flux balance equation to a converter topology is illustrated here with an example. Let's say, the required conversion ratio is

$$\frac{V_{C1}}{V_{in}} = \frac{(1-2D)}{(1-D)} \tag{7}$$

It leads to a flux balance equation of a topology

$$V_{in}.D + (-V_{in} + V_{C1}).D' = 0 \tag{8}$$

Fig. 3 (a) plots this converter ratio as a function of the duty cycle. The procedure to implement the schematic starts with the identification of voltage across the inductor during $D$ and $D'$

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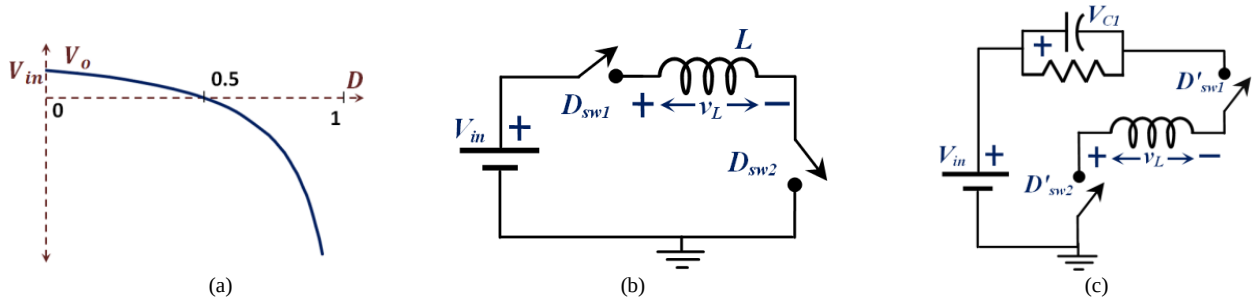
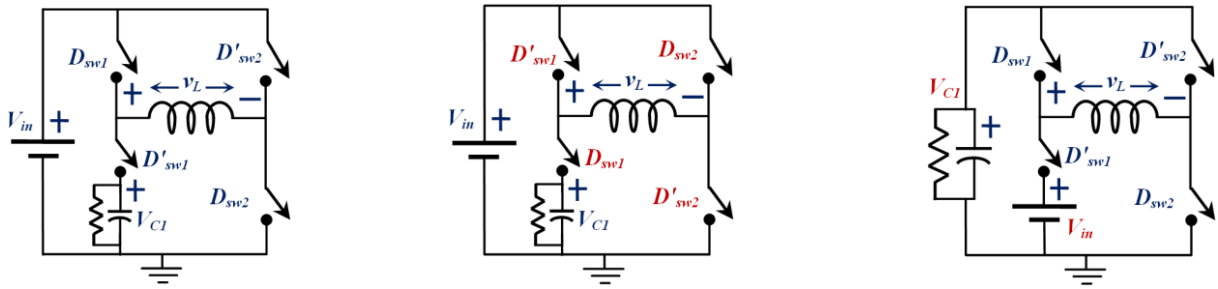


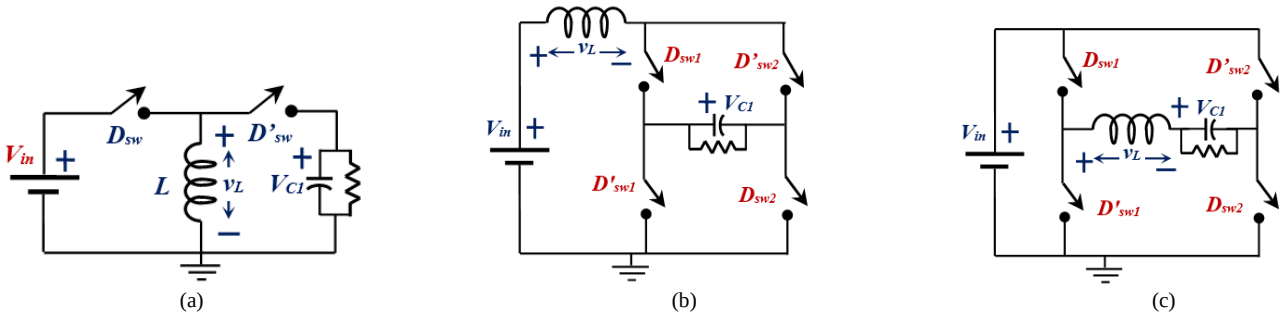

(a) (b) (c)

Fig. 3. (a) Conversion ratio as a function of the Duty cycle (D), (b) Circuit in D-interval, and (c) Circuit in D'-interval.




(a) (b) (c)

Fig. 4. (a) Complementary Watkins-Johnson topology, (b) Complementary-Complementary Watkins-Johnson topology = Watkins-Johnson topology, and (c) Inverse Watkins-Johnson topology




(a) (b) (c)

Fig. 5. (a) Buck-boost topology, (b) Current fed topology, and (c) Bridge topology.

interval. In *D* interval, the voltage across the inductor is $V_{in}$, and in *D*' interval, it is ($-V_{in}+V_{C1}$) as shown in Fig. 3 (b) and (c), respectively.

The overall topology is shown in Fig. 4 (a), and it is named complementary Watkins-Johnson topology (C-WJ). Its complementary topology is the well-known Watkins-Johnson topology, illustrated in Fig. 4(b). The inverse of Watkins Johnson topology is obtained simply by exchanging the sources and load of a Watkins-Johnson topology as shown in Fig. 4 (c). For *D* greater than 0.5, the output can be higher or lower than the input with negative polarity. Below *D* = 0.5, the topology exhibits a buck function.

### G. *Symmetries in Table 1*

The governing equation of a first order converter is given in (4a). All the combinations are tabulated in Table I. Based on this equation, the following symmetries can be observed.

*1)* If the values of $\alpha$ and $\beta$ are changed to $-\alpha$ and $-\beta$, the volt-sec equation remains unchanged. For example, the converter corresponding to $\alpha^T$ = [1 0], $\beta^T$ = [0 1] present at left corner of Table I, is identical with the converter corresponding to $\alpha^T$ = [-1 0], $\beta^T$ = [0 -1]. Thus, the table can be divided into four quadrants, each corresponding to 12 admissible combinations of $\alpha$ and $\beta$ values. The entries in 3rd and 1st quadrant lead to same converters. Same is true for the 2nd and 4th quadrants. Thus, only the left half of the table needs to be examined.

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TABLE I
FIRST ORDER CONVERTER CHART

| $[\alpha_{10}, \alpha_{11}]$ | [1, 0] | [0, 1] | [1, -1] | [1, 1] | [-1, 0] | [0, -1] | - [1, -1] | - [1, 1] |
|---|---|---|---|---|---|---|---|---|
| $[\beta_{10}, \beta_{11}]$ | *(Voltage Across the Inductor in D-interval corresponding to $[\alpha_{10}, \alpha_{11}]$ values)* | | | | | | | |
| | $V_{in}$ | $V_C$ | $(V_{in}-V_C)$ | $(V_{in}+V_C)$ | $(-V_{in})$ | $(-V_C)$ | $(-V_{in}+V_C)$ | $(-V_{in}-V_C)$ |
| [1, 0] | $V_{in}$ | $-\frac{(1-D)}{D}$<br>**I-/ C- Buck-Boost** | $\frac{1}{D}$<br>**I- Buck** | $-\frac{1}{D}$<br>**N-I-Buck** | | $\frac{(1-D)}{D}$<br>**I-/ C- Non-Inverting Buck-Boost** | $\frac{(2D-1)}{D}$<br>**WJ** | $\frac{(1-2D)}{D}$<br>**N-WJ** |
| [0, 1] | $V_C$ | $-\frac{D}{(1-D)}$<br>**Buck-Boost** | $\frac{D}{(2D-1)}$<br>**I- Watkins-Johnson (IWJ)** | $-D$<br>**N-Buck** | $\frac{D}{(1-D)}$<br>**N-Buck-Boost** | | D<br>**Buck** | $\frac{D}{(1-2D)}$<br>***I- N-WJ*** |
| [1, -1] | $V_{in}-V_C$ | $\frac{1}{(1-D)}$<br>**Boost** | $\frac{(1-D)}{(1-2D)}$<br>**I-C-WJ** | $\frac{1}{(1-2D)}$<br>**C-Current Fed** | $\frac{(1-2D)}{(1-D)}$<br>**C-WJ** | $(1-D)$<br>**I-Boost/ C-Buck** | | $(1-2D)$<br>**C-Bridge** |
| [1, 1] | $(V_{in}+V_C)$ | $-\frac{1}{(1-D)}$<br>**N-Boost** | $-(1-D)$<br>**N-I-Boost** | $\frac{1}{(2D-1)}$<br>**I-Bridge/ Current-fed** | $\frac{(2D-1)}{(1-D)}$<br>***N-C-WJ*** | $\frac{(1-D)}{(2D-1)}$<br>***I-C-WJ*** | $(2D-1)$<br>**Bridge/ I- Current-fed** | |
| [-1, 0] | $-V_{in}$ | $\frac{(1-D)}{D}$<br>**Non Inverting Buck-Boost** | $\frac{(2D-1)}{D}$<br>**WJ/ I-IWJ** | $\frac{(1-2D)}{D}$<br>**N-WJ** | | $-\frac{(1-D)}{D}$<br>**I-Buck-Boost** | $\frac{1}{D}$<br>**C-Boost/ I-Buck** | $-\frac{1}{D}$<br>**N-C-Boost** |
| [0, -1] | $-V_C$ | $\frac{D}{(1-D)}$<br>**Non Inv. Buck-Boost** | $D$<br>**Buck** | $\frac{D}{(1-2D)}$<br>**I- N-WJ** | $-\frac{D}{(1-D)}$<br>**Buck-Boost** | | $\frac{D}{(2D-1)}$<br>**I-WJ** | $-D$<br>**N-Buck** |
| [-1, 1] | $-(V_{in}+V_C)$ | $\frac{(1-2D)}{(1-D)}$<br>**C-WJ** | $(1-D)$<br>**I-Boost** | $(1-2D)$<br>**C-Bridge** | $\frac{1}{(1-D)}$<br>**Boost** | $\frac{(1-D)}{(1-2D)}$<br>**C-IWJ** | | $\frac{1}{(1-2D)}$<br>**C-Current-fed** |
| [-1, -1] | $-(V_{in}+V_C)$ | $\frac{(2D-1)}{(1-D)}$<br>**N-C-WJ** | $\frac{(1-D)}{(2D-1)}$<br>**I-C-WJ** | $(2D-1)$<br>**Bridge/ I- Current-fed** | $-\frac{1}{(1-D)}$<br>**N-Boost** | $-(1-D)$<br>**N-I-Boost** | $\frac{1}{(2D-1)}$<br>**I-Bridge** | |

*(Voltage Across the Inductor in D-interval corresponding to $[\beta_{10}, \beta_{11}]$ values)*

| | |
|---|---|
| | Invalid Combination of $[\alpha_{10}, \alpha_{11}]$, and $[\beta_{10}, \beta_{11}]$. |
| *Gain* | Converter gain ($G$) corresponding to $[\alpha_{10}, \alpha_{11}]$, and $[\beta_{10}, \beta_{11}]$ values. |
| **Name** | Name of the converter corresponding to $[\alpha_{10}, \alpha_{11}]$, and $[\beta_{10}, \beta_{11}]$ values where complementary, negative, and inverse gains are indicated by prefixes *C*, *N*, and *I*, respectively. |

*2)* An exchange of values of $\alpha$ and $\beta$ leads to the complementary converter. The operations at $D$ and $D'$ are equivalent. Thus, it is sufficient to consider only lower triangular half of any given quadrant.

*3)* Exchanging values of ($\alpha_{10}$ and $\alpha_{11}$) and ($\beta_{10}$ and $\beta_{11}$) leads to a change in gain from $G$ to $1/G$. This corresponds to exchanging input and output terminals of a configuration. This was discussed in subsection C of this section.

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Based on this table, as far as topology is concerned, four basic converters are identified: Boost, Buck-Boost, Watkins-Johnson, and Current Fed topologies. Boost and Watkins-Johnson (WJ) topologies are shown in Fig 1(a) and 4(b), respectively. The Buck-Boost and Current fed topologies are shown in Fig. 5(a) and (b), respectively. It can also be noted that the Bridge topology, shown in Fig 5(c), is the Inverse Current fed bridge (I-Current fed). The remaining configurations are either inverse, complementary, negative, or a combination of the aforementioned basic topologies. An interesting observation is that the buck converter doesn't appear to be a basic topology. The reason being, topologically, it is same as a boost converter. In fact, it can be termed as a Complementary-Inverted Boost topology.

## V. SECOND-ORDER CONVERTERS

Similarly, in second-order converters [29-37] there are two *LC* pairs and one input voltage ($V_{in}$). The voltage ($V_{C2}$), across the capacitor $C_2$, is considered as the output. Whereas, voltage ($V_{C1}$), across the capacitor $C_1$ is an intermediate DC link. Using (2), the general form of the volt-sec equation in matrix form is given by

$$\begin{bmatrix} C_{11}^T D_t & C_{12}^T D_t \\ C_{21}^T D_t & C_{22}^T D_t \end{bmatrix} . \begin{bmatrix} V_{C1} \\ V_{C2} \end{bmatrix} = - \begin{bmatrix} {C_{10}}^T . D_t \\ {C_{20}}^T . D_t \end{bmatrix} . V_{in}$$

This simplifies to,

$$\begin{aligned} (f_{11}).D + (f_{12}).D' &= 0 \\ (f_{21}).D + (f_{22}).D' &= 0 \end{aligned} \quad (9a)$$

Where,

$$\begin{aligned} f_{11} &= \alpha_{10}.V_{in} + \alpha_{11}.V_{C1} + \alpha_{12}.V_{C2}, \\ f_{12} &= \beta_{10}.V_{in} + \beta_{11}.V_{C1} + \beta_{12}.V_{C2}, \\ f_{21} &= \alpha_{20}.V_{in} + \alpha_{21}.V_{C1} + \alpha_{22}.V_{C2}, \\ and\ f_{22} &= \beta_{20}.V_{in} + \beta_{21}.V_{C1} + \beta_{22}.V_{C2} \end{aligned}$$

In the above equation, the coefficients $\alpha_{ij}$ and $\beta_{ij}$, $i$ = 1, 2 and $j$ = 0, 1, 2 are chosen from the set {0, +1, -1}. Using (9a), the number of valid combinations of individual functions $f_{11}$, $f_{12}$ and $f_{21}$, $f_{22}$ are given by

$$\begin{aligned} m_2 = \sum_{i=1}^{3} \left( {}^3C_i \times 2^i \right) &= \left( {}^3C_1 \times 2^1 \right) + \left( {}^3C_2 \times 2^2 \right) \\ &\quad + \left( {}^3C_3 \times 2^3 \right) \\ &= 6 + 12 + 8 = 26 \end{aligned}$$

This conclusion can also be obtained using ($3^{2+1}$-1). These 26 valid expressions for functions $f_{11}$, $f_{12}$, $f_{21}$, and $f_{22}$ are given by

$$\left.\begin{matrix} \pm V_{in}, \pm V_{C1}, \pm V_{C2} \end{matrix}\right\} \text{6 terms with one variable}$$

$$\left.\begin{matrix} \pm(V_{in} + V_{C1}), \pm(V_{in} + V_{C2}) \\ \pm(V_{C1} + V_{C1}), \pm(V_{in} - V_{C1}) \\ \pm(V_{in} - V_{C2}), \pm(V_{C1} - V_{C1}) \end{matrix}\right\} \text{12 terms with two variables}$$

$$\left.\begin{matrix} \pm(V_{in} + V_{C1} + V_{C2}), \pm(V_{in} - V_{C1} + V_{C2}) \\ \pm(V_{in} + V_{C1} - V_{C2}), \pm(V_{in} - V_{C1} - V_{C2}) \end{matrix}\right\} \text{8 terms with three variables}$$

A particular choice of functions $f_{11}$, $f_{12}$, $f_{21}$, and $f_{22}$ corresponds to certain values for parameters $\alpha_{ij}$ and $\beta_{ij}$, for $i$ = 1, 2, $j$ = 0, 1, 2, from the set {0,1,-1}.

The gain of the converter G=$V_{C2}/V_{in}$ is given by,

$$\begin{aligned} G &= \frac{V_{C2}}{V_{in}} \\ &= \frac{D^2 \begin{vmatrix} \alpha_{21} & \alpha_{11} \\ \alpha_{20} & \alpha_{10} \end{vmatrix} + DD' \left( \begin{vmatrix} \alpha_{21} & \beta_{11} \\ \alpha_{20} & \beta_{10} \end{vmatrix} + \begin{vmatrix} \beta_{21} & \alpha_{11} \\ \beta_{20} & \alpha_{10} \end{vmatrix} \right) + D'^2 \begin{vmatrix} \beta_{21} & \beta_{11} \\ \beta_{20} & \beta_{10} \end{vmatrix}}{D^2 \begin{vmatrix} \alpha_{22} & \alpha_{12} \\ \alpha_{21} & \alpha_{11} \end{vmatrix} + DD' \left( \begin{vmatrix} \alpha_{22} & \beta_{12} \\ \alpha_{21} & \beta_{11} \end{vmatrix} + \begin{vmatrix} \beta_{22} & \alpha_{12} \\ \beta_{21} & \alpha_{11} \end{vmatrix} \right) + D'^2 \begin{vmatrix} \beta_{22} & \beta_{12} \\ \beta_{21} & \beta_{11} \end{vmatrix}} \end{aligned} \quad (9b)$$

This expression leads to following observations.

### A. Gain Expression

The gain ($G=V_{C2}/V_{in}$) is the ratio of two second-order polynomials as given in (9b). This decides the general form of the gain expression that can be realized.

### B. Cascading Two First Order Converters to Realize A Second-Order Converter

Cascading two converters simply means the output of the first converter acts as an input to the second converter. The output of the second converter is the overall output of the second-order converter. This is equivalent to making coefficients $\alpha_{12}, \beta_{12}, \alpha_{20}$, and $\beta_{20}$ equal to zero. The coefficients $f_{11}$, $f_{12}$, $f_{21}$, and $f_{22}$ in (9a) reduces to

$$\begin{aligned} f_{11} &= \alpha_{10}.V_{in} + \alpha_{11}.V_{C1}, \\ f_{12} &= \beta_{10}.V_{in} + \beta_{11}.V_{C1}, \\ f_{21} &= \alpha_{21}.V_{C1} + \alpha_{22}.V_{C2}, \\ \text{and } f_{22} &= \beta_{21}.V_{C1} + \beta_{22}.V_{C2} \end{aligned} \quad (11)$$

In this case, the gain expression in (9b) reduces to

$$G = \frac{V_{C2}}{V_{in}} = \left( -\frac{\alpha_{10}D + \beta_{10}D'}{\alpha_{11}D + \beta_{11}D'} \right) \times \left( -\frac{\alpha_{21}D + \beta_{21}D'}{\alpha_{22}D + \beta_{22}D'} \right)$$

Each factor of the aforementioned equation corresponds to a gain expression of the type given by (5) for first-order converters. In other words, a second order converter can be decomposed into two cascaded first order converters, as shown in Fig 6. If both the volt-sec equations are the same, they lead to quadratic structures such as boost[2], buck-boost[2], etc.

For example, as shown in Table II, converters with DC conversion ratios $\frac{D(1-D)}{(1-2D)^2}, \frac{(1-D)^2}{(1-2D)^2}, \frac{(1-2D)^2}{(1-D)}$ and $\frac{D^2}{(1-D)^2}$ can be realized with a minimum of two inductors, two capacitor

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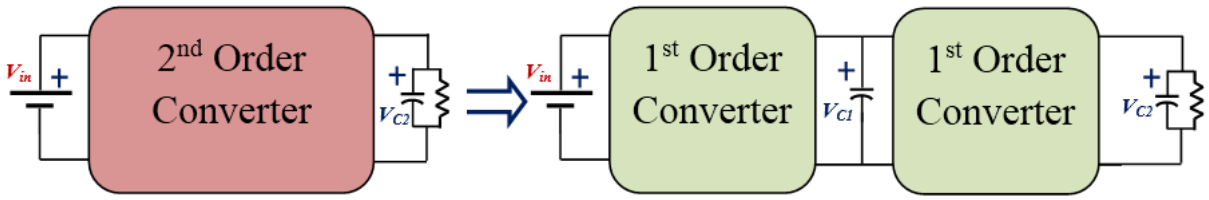


Fig. 6. Cascade decomposition of second order converters.

TABLE II
CASCADE DECOMPOSITION OF SECOND ORDER CONVERTERS.

| DC conversion ratio of the 2nd order converter | DC conversion ratio of cascaded 1st order converters |
|---|---|
| $\frac{D(1-D)}{(1-2D)^2}$ | $\frac{D}{(1-2D)}$ and $\frac{(1-D)}{(1-2D)}$ |
| $\frac{(1-D)^2}{(1-2D)^2}$ | $\frac{(1-D)}{(1-2D)}$ and $\frac{(1-D)}{(1-2D)}$ |
| $\frac{(1-2D)^2}{(1-D)}$ | $\frac{(1-2D)^2}{(1-D)}$ and $(1-2D)$ |
| $\frac{D^2}{(1-D)^2}$ | $\frac{D}{(1-D)}$ and $\frac{D}{(1-D)}$ |

TABLE III
POSSIBLE TERMS FOR CONVERSION RATIO $D^2/(1\text{-}D)^2$

| Converters | $f_{11}$ | $f_{12}$ | $f_{21}$ | $f_{22}$ |
|---|---|---|---|---|
| 1 [New] | $V_{in}$ | $V_{in}+V_{C1}$ | $V_{in}+V_{C1}$ | $V_{C2}$ |
| 2 [New] | $V_{in}$ | $V_{C2}-V_{C1}$ | $V_{C2}-V_{C1}$ | $V_{C2}$ |
| 3 [38] | $V_{in}$ | $-V_{C1}$ | $-V_{C1}$ | $V_{C2}$ |
| 4 [39] | $V_{in}$ | $-V_{C1}$ | $V_{in}+V_{C1}$ | $-(V_{C1}+V_{C2})$ |

converter structures. Some of these converters possess wider voltage gain characteristics compared to converters presented in [12], [13] but have not been considered before in literature. A simple way of realizing these converters would be to connect two first order converters, as listed in Table II, in cascade. The number of active switches can be optimized for an intended application by applying the merging theory proposed in [10].

### C. Other Symmetries in Second Order Converters

Complementary, inverse, and inverse-complementary topologies can be easily synthesized from the gain expression of a converter topology. As there are two sets of volt-sec equations, two more exceptions are applicable in this case.

1) If $C_{10} = \pm C_{20}$, $C_{11} = \pm C_{21}$, and $C_{12} = \pm C_{22}$, it leads to two cases where both the inductors have the same volt-sec equation. Each case is equivalent to two identical first-order converters in parallel with a common output.
2) If $C_{11} = \pm C_{21}$ or $C_{11} = 0, \text{or } C_{21} = 0$, the converter gain degenerates to a first order gain.

TABLE IV
INDUCTOR VOLT-SEC EQUATIONS CORRESPONDING TO DIFFERENT $\alpha$ AND $\beta$ VALUES.

| $i$=1 for $L_1$ and $i$=2 for $L_2$ | | | | | |
|---|---|---|---|---|---|
| $[\alpha_{i0}, \alpha_{i1}, \alpha_{i2}]$ / $[\beta_{i0}, \beta_{i1}, \beta_{i2}]$ | [1,0,0] | [0,1,0] | [0,0,1] | [1,1,0] | … |
| [1,0,0] | | $DV_{C1}=-D'V_{in}$ | $DV_{C2}=-D'V_{in}$ | $DV_{C1}=-V_{in}$ | … |
| [0,1,0] | $DV_{in}=-D'V_{C1}$ | | $DV_{C2}=-D'V_{C1}$ | $V_{C1}=-DV_{in}$ | … |
| [0,0,1] | $DV_{in}=-D'V_{C2}$ | $DV_{C1}=-D'V_{C2}$ | | $D(V_{in}+V_{C1})=-D'V_{in}$ | … |
| [1,1,0] | $V_{in}=-D'V_{C1}$ | $V_{C1}=-D'V_{in}$ | $DV_{C2}=D'(V_{in}+V_{C1})$ | | … |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | |

*(26×26)*

### D. Different Flux Balance Equations Leading to The Same Converter Gain (G)

(9b) has twelve parameters of the type $\alpha_{ij}$, $\beta_{ij}$. The gain expression has only six coefficients depending on these parameters. Therefore, for the desired gain expression, six parameters can be chosen arbitrarily while remaining six can be calculated to set the desired gain. Hence, different choices of parameters may lead to same gain expression, i.e., converters can have different electrical equivalent circuits in different switching intervals, yet they share a common voltage conversion ratio. Table III provides four different ways to realize a quadratic buck-boost converter. From these, the last two topologies are reported in [35, 36]. However, the converters 1 and 2 are new topologies that are identified by the proposed theory. These topologies are discussed further in section VI.

### E. Total number of second order converters

The values of coefficients ($\alpha_{i0}$, $\alpha_{i1}$, $\alpha_{i2}$) and ($\beta_{i0}$, $\beta_{i1}$, $\beta_{i2}$) are chosen from a set {0, -1, 1}, for $i$ = 1, 2. However, the choice [0, 0, 0] is prohibited. Therefore, $3^3$-1=26 choices exist for each vector. Hence, as tabulated in Table IV, 26×26 different volt-sec expressions are possible. However, the constraints $\alpha_{i0} \neq \pm\beta_{i0}$, $\alpha_{i1} \neq \pm\beta_{i1}$, *and* $\alpha_{i2} \neq \pm\beta_{i2}$ restrict the total number of volt-sec expressions to 26×(26-2). As a result,

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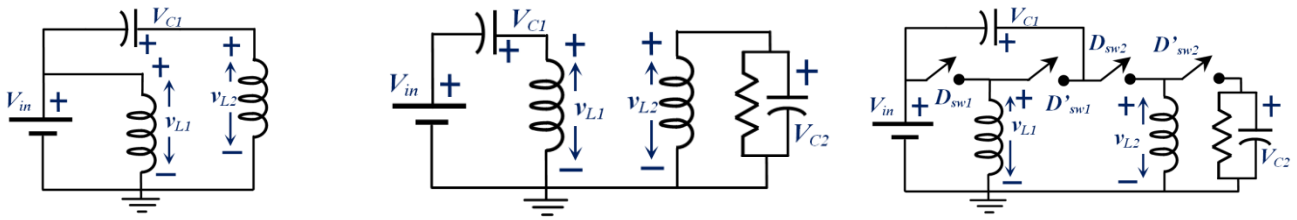


Fig. 7. (a) D Interval of Q buck-boost Topology, (b) D' Interval of Q buck-boost Topology, and (c) Q buck-boost Topology.

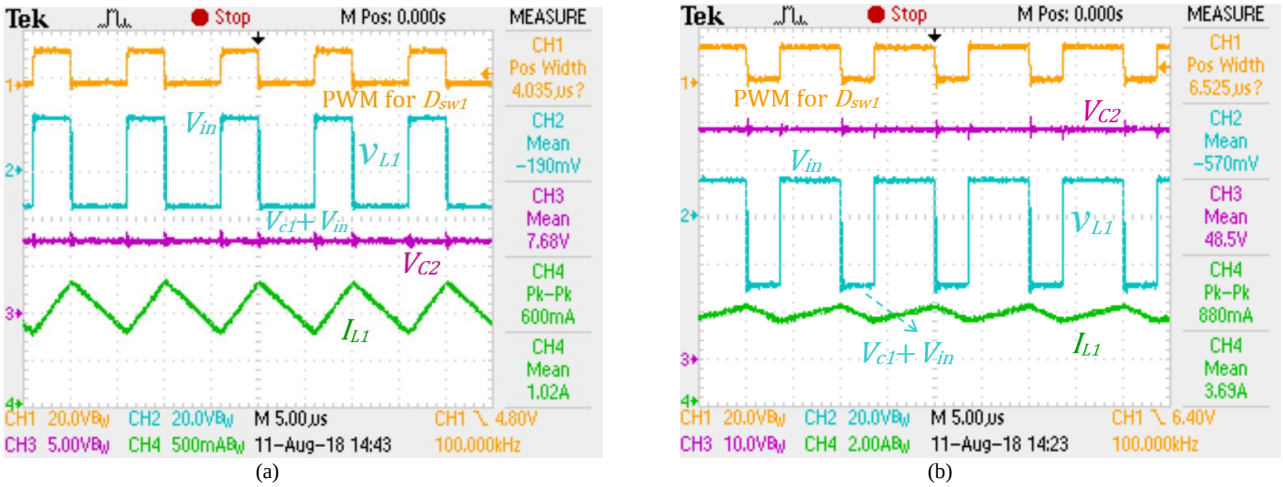


Fig. 8. Experimental verification of the proposed Q buck-boost with (a) $V_{in}$= 22 V, $D$=0.4, and $R_o$= 9Ω at $F_s$=100 kHz (buck mode), and (b) $V_{in}$= 16 V, and $D$=0.6, and $R_o$= 74 Ω at $F_s$=100 kHz (boost mode). Experimental parameters: $L_1$, $L_2$: 160 µH; and $C1$, $C2$: 300 µF. Component Specifications: $D_{sw1}$, $D_{sw2}$: Rohm-SCT3120AL MOSFETs; $D'_{sw1}$, $D'_{sw2}$: C3D10060A diodes.

*1)* For same values of vectors $\alpha_i$ and $\beta_i$, for $i$ = 1 and $i$ = 2, the resulting converter is equivalent to two first order converters in parallel.

*2)* For different values of vectors $\alpha_i$ and $\beta_i$, for $i$=1 and $i$=2, we obtain different flux balance equations for each inductor. There are very large no. of choices (26×24)×{(26×24)-2} that can be made. However, from this set, a large number of choices may lead to same converter gain expression. Therefore, it is important to synthesize the converter starting from the required voltage conversion gain expression, as discussed in section VI.

## VI. Synthesizing a Converter From its Voltage Conversion Equation

Any converter can be synthesized from its voltage conversion equation. In order to do so, first a voltage conversion equation needs to be selected, and from this, the functions $f_{11}$, $f_{12}$, $f_{21}$, and $f_{22}$ are derived. It will be shown that this is not a unique process as identified in section V. As soon as the flux balance functions are derived, the converter topology can be synthesized to realize this function. Several new quadratic structures are synthesized to demonstrate the versatility of this theory.

### A. Quadratic Buck-Boost Topology (Q Buck-Boost)

The basic quadratic buck-boost voltage conversion equation is given by $V_{C2} = \left(\frac{D}{D'}\right)^2 . V_{in}$. As identified in section V, converter synthesis is not a unique process. Depending on the functions $f_{11}$, $f_{12}$, $f_{21}$, and $f_{22}$, different converter topologies can be synthesized to achieve the gain $\left(\frac{D}{D'}\right)^2$. Table III provides four different ways to realize a quadratic buck-boost converter. From these, the last two topologies are reported in [38], and [39], respectively. However, the topologies 1 and 2 are new topologies that are identified by the proposed theory. The detailed synthesis method for topologies 1 and 2 are discussed here.

#### *1) Topology 1:*

The basic quadratic buck-boost voltage conversion equation is given by

$$V_{C2} = \left(\frac{D}{D'}\right)^2 . V_{in} = \left(-\frac{V_{in}}{D'}\right).\left(-\frac{D^2}{D'}\right) = V_{C1}.\left(-\frac{D^2}{D'}\right) \quad (12)$$

Where

$$V_{C1} = -\frac{V_{in}}{D'} \quad (13)$$

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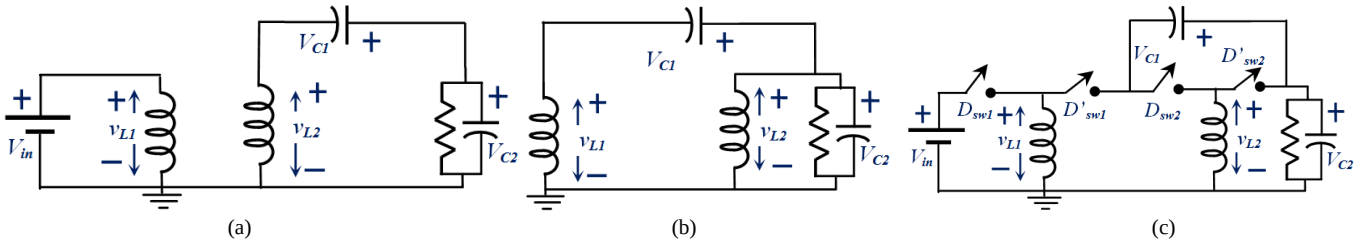


Fig. 9. (a) D Interval of Q buck-boost Topology 2, (b) D' Interval of Q buck-boost Topology 2, and (c) Q buck-boost Topology 2.

Using the above two equations, the volt-sec balance equations across the two inductors can be derived. Depending on the way the volt-sec equations are written, it leads to different $f_{11}$, $f_{12}$, $f_{21}$, and $f_{22}$ functions. Thus, it leads to different topologies. Using (13) with the substitution ($D$+$D'$) =1

$$V_{C1}.D' = -(D.V_{in} + D'.V_{in})$$
$$\Longrightarrow D.V_{in} + D'.(V_{in} + V_{C1}) = 0 \quad (14)$$

For the volt-sec balance equation for the second inductor,

$$V_{C2} = V_{C1}.\left(-\frac{D^2}{D'}\right)$$
$$\Longrightarrow V_{C2}.D' = -D^2.V_{C1}$$
$$\Longrightarrow V_{C2}.D' + D^2.V_{C1} = V_{C2}.D' + D.(1-D').V_{C1} = 0$$
$$\Longrightarrow D.(V_{in} + V_{C1}) + D'.(V_{C2}) = 0 \quad (15)$$

(14) and (15) corresponds to $f_{11} = V_{in}$, $f_{12} = (V_{in}+V_{C1})$, $f_{21} = (V_{in}+V_{C1})$, and $f_{22} = V_{C2}$.Fig. 7 (a) and (b) show the linear circuits formed by (14) and (15). Fig. 7(c) shows the new Q buck-boost topology. Experimental results verifying the circuit operation in buck mode and boost mode are shown in Fig. 8 (a) and (b), respectively. Steady-state waveforms of PWM signal for switch $D_{sw1}$, voltage across $L_1$ ($v_{L1}$), output voltage ($V_{C2}$), and inductor current ($I_{L1}$) are shown. In the experimental prototype, switches $D_{sw1}$ and $D_{sw2}$ are realized using Rohm-SCT3120AL MOSFETs and remaining two switches are realized using C3D10060A diodes. The inductance ($L_1$ and $L_2$) and capacitance ($C_1$ and $C_2$) are chosen to be 160 µH and 300 µF, respectively.

### 2) *Topology 2:*

The basic quadratic buck-boost voltage conversion equation is given by

$$V_{C2} = \left(\frac{D}{D'}\right)^2.V_{in} = D.\frac{D}{(D')^2}.V_{in} = D.V_{C1} \quad (16)$$

Where

$$V_{C1} = \frac{D}{(D')^2}.V_{in} \quad (17)$$

Using the above two equations, the volt-sec balance equations across the two inductors can be derived. Depending on the way the volt-sec equations are written, it leads to different $f_{11}$, $f_{12}$, $f_{21}$, and $f_{22}$ functions. Thus, it leads to different topologies.

Using (17)

$$V_{C1}(D')^2 = D.V_{in}$$
$$\Longrightarrow (1-D)(1-D).V_{C1} = D.V_{in}$$
$$\Longrightarrow (D')(V_{C1} - D.V_{C1}) = D.V_{in}$$
$$\Longrightarrow D.V_{in} + D'.(V_{C2} - V_{C1}) = 0 \quad (18)$$

For the volt-sec balance equation for the second inductor, let's start from (16) with the substitution ($D$+$D'$) =1

$$V_{C2} = D.V_{C1}$$
$$\Longrightarrow (D+D').V_{C2} = D.V_{C1}$$
$$\Longrightarrow D(V_{C2} - V_{C1}) + D'.V_{C2} = 0 \quad (19)$$

(18) and (19) corresponds to $f_{11} = V_{in}$, $f_{12} = (V_{C2}$-$V_{C1})$, $f_{21} = (V_{C2}$-$V_{C1})$, and $f_{22} = V_{C2}$. Fig. 9 (a) and (b) show the linear circuits formed by (18) and (19). Fig. 9 (c) shows the new Q buck boost topology.

It can be noted that though both the topologies are derived from completely different sets of flux balance equations, they are similar in the way that the input and output stages are interchanged.

The proposed Quadratic Buck-Boost Converter topology 1 is compared with the quadratic buck-boost converters presented in [38] and [39]. The voltage stress across the switches are similar to that of the converter proposed in [39]. However, the intermediate $V_{C1}$ is higher in the proposed converter. Similarly, the average current flowing through various switches is equal. Whereas, the ripple in the inductor currents $i_{L1}$ and $i_{L2}$ are different. The voltage stress across the switches and current stress (peak and RMS current flowing through the switches) of the switches are tabulated in Appendix A.

## B. *Quadratic Buck Topology (Q Buck)*

The basic quadratic buck voltage conversion equation is given by $V_{C2} = D^2\,V_{in}$. Depending on the functions $f_{11}$, $f_{12}$, $f_{21}$, and $f_{22}$ different converter topologies can be synthesized to achieve the gain of $D^2$. Table V provides four different ways to realize a quadratic buck converter. From these, the last two topologies are reported in [12], and [40], respectively. However, the topologies 1 and 2 are new topologies that are identified by the proposed theory.

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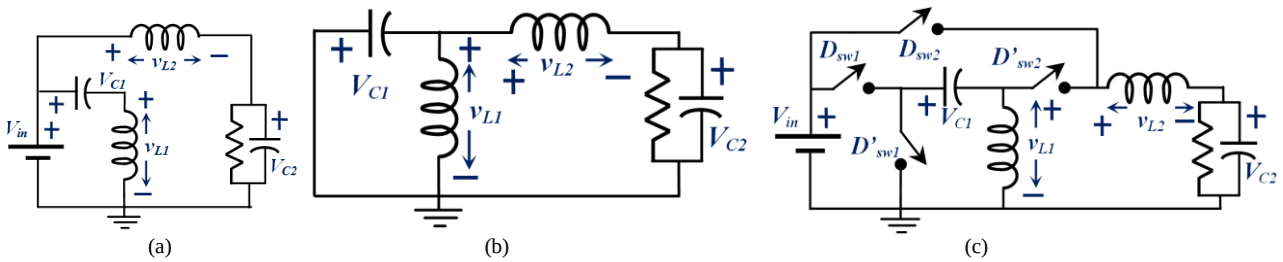
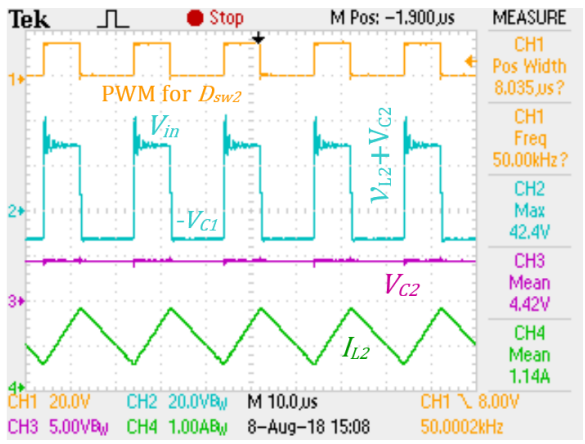
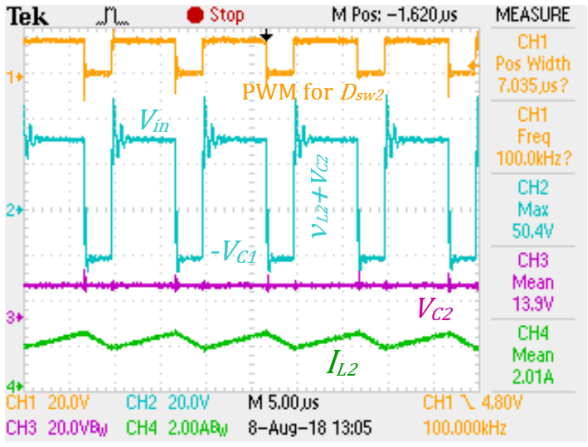



(a) (b) (c)

Fig.10 (a) D Interval of Q Buck Topology 1, (b) D' Interval of Q Buck Topology 1, and (c) Q Buck Topology 1.




(a)




(b)

Fig. 11. Experimental verification of the proposed Q Buck topology with (a) $V_{in}$= 30 V, $D$= 0.4, and $R_o$= 3.8 Ω at $F_s$=50 kHz, and (b) $V_{in}$= 30 V, $D$=0.7, and $R_o$= 7 Ω at $F_s$=100 kHz. Experimental parameters: $L_1$, $L_2$: 160 µH; and $C_1$, $C_2$: 300 µF. Component Specifications: $D'_{sw1}$, $D_{sw2}$: Rohm-SCT3120AL MOSFETs; $D_{sw1}$, $D'_{sw2}$: C3D10060A diodes.

TABLE V
POSSIBLE TERMS FOR CONVERSION RATIO $D^2$

| Converters | $f_{11}$ | $f_{12}$ | $f_{21}$ | $f_{22}$ |
|---|---|---|---|---|
| 1 [new] | $V_{in}$-$V_{C1}$ | -$V_{C1}$ | $V_{in}$-$V_{C2}$ | -$V_{C1}$-$V_{C2}$ |
| 2 [new] | $V_{C1}$ | -$V_{in}$+$V_{C1}$ | $V_{in}$-$V_{C1}$-$V_{C2}$ | -$V_{C2}$ |
| 3 [12] | $V_{in}$-$V_{C1}$ | -$V_{C1}$ | $V_{C1}$-$V_{C2}$ | -$V_{C2}$ |
| 4 [40] | $V_{in}$-$V_{C1}$-$V_{C2}$ | -$V_{C1}$-$V_{C2}$ | $V_{C1}$ | -$V_{C2}$ |

### 1) Topology 1:

Conventional Quadratic buck topology is discussed in [40]. The basic quadratic buck voltage conversion equation is given by

$$V_{C2} = D^2.V_{in} = D.D.V_{in} = D.V_{C1} \qquad (20)$$

Where

$$V_{C1} = D.V_{in} \qquad (21)$$

Using the above two equations, the volt-sec balance equations across the two inductors can be derived. Depending on the way the volt-sec equations are written, it leads to different $f_{11}$, $f_{12}$, $f_{21}$ and $f_{22}$ functions. Thus, it leads to different topologies. Using (21) with the substitution ($D$+$D$') =1

$$V_{C1}(D + D') = D.V_{in}$$

$$\Longrightarrow D.(V_{in} - V_{C1}) + D'.(-V_{C1}) = 0 \qquad (22)$$

For the volt-sec balance equation for the second inductor, let's start from (20) with the substitution ($D$+$D$') =1

$$V_{C2}(D + D') = D.V_{C1}$$

$$\Longrightarrow V_{C2}(D + D') = (1 - D').V_{C1}$$

$$\Longrightarrow V_{C2}(D + D') = V_{C1} - D'.V_{C1}$$

$$\Longrightarrow V_{C2}(D + D') = D.V_{in} - D'.V_{C1}$$

$$\Longrightarrow D.(V_{in} - V_{C2}) + D'.(-V_{C1} - V_{C2}) = 0 \qquad (23)$$

(22) and (23) corresponds to $f_{11}$ = ($V_{in}$-$V_{C1}$), $f_{12}$ = (-$V_{C1}$), $f_{21}$ = ($V_{in}$-$V_{C2}$), and $f_{22}$ = (-$V_{C1}$-$V_{C2}$). Fig. 10 (a) and (b) show the linear circuits formed by (22) and (23), respectively. Fig. 10 (c) shows the new Q buck topology. Experimental results verifying the circuit operation at $D$ = 0.4 and 0.7 are shown in Fig. 11 (a) and (b), respectively. Steady-state waveforms of PWM signal for switch $D_{sw2}$, voltage $V_{C2}$+$v_{L2}$, output voltage ($V_{C2}$), and inductor current ($I_{L2}$) are shown. In the experimental prototype, switches $D'_{sw1}$ and $D_{sw2}$ are realized using Rohm-SCT3120AL MOSFETs and remaining two switches are realized using C3D10060A diodes. The inductance ($L_1$ and $L_2$) and capacitance ($C_1$ and $C_2$) are chosen to be 160 µH and 300 µF, respectively.

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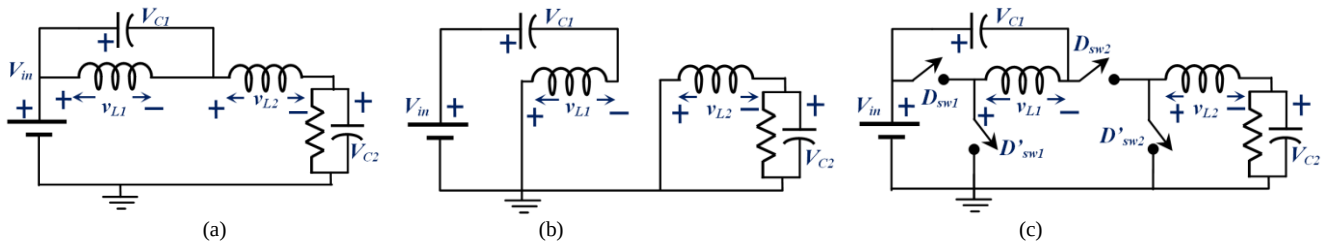


Fig. 12. (a) D Interval of Q Buck Topology 2, (b) D' Interval of Q Buck Topology 2, and (c) Q Buck Topology 2.

### *2) Topology 2:*

The basic quadratic buck voltage conversion equation is given by

$$V_{C2} = D^2.V_{in} = (D^2 + D - D).V_{in} = D.V_{in} - D.D'.V_{in} \quad (24)$$

Where

$$V_{C1} = D'.V_{in} \quad (25)$$

Using the above two equations, the volt-sec balance equations across the two inductors can be derived. Depending on the way the volt-sec equations are written, it leads to different $f_{11}$, $f_{12}$, $f_{21}$, and $f_{22}$ functions. Thus, it leads to different topologies. Using (25) with the substitution ($D$+$D$') = 1

$$V_{C1}(D + D') = D'.V_{in}$$
$$\Longrightarrow D.(V_{C1}) + D'.(-V_{in} + V_{C1}) = 0 \quad (26)$$

For the volt-sec balance equation for the second inductor, let's start from (24) with the substitution ($D$+$D$') =1

$$V_{C2}(D + D') = D.V_{in} - D.V_{C1}$$
$$\Longrightarrow D.(V_{in} - .V_{C1} - V_{C2}) + D'(-V_{C2}) = 0 \quad (27)$$

(26) and (27) corresponds to $f_{11} = V_{C1}$, $f_{12} = (-V_{C1})$, $f_{21} = (V_{in}$-$V_{C1}$-$V_{in})$, and $f_{22} = -V_{C2}$. Fig. 12 (a) and (b) show the linear circuits formed by (26) and (27). Fig. 12 (c) shows the new Q buck topology.

## *C. Quadratic Boost Topology (Q Boost)*

The basic quadratic boost voltage conversion equation is given by $V_{C2} = \frac{1}{D'^2}.V_{in}$. Depending on the functions $f_{11}$, $f_{12}$, $f_{21}$, and $f_{22}$ , different converter topologies can be synthesized to achieve the gain of $\frac{1}{D'^2}$. Table VI provides three different ways to realize a quadratic boost converter. From these, the last two topologies are reported in [41, 42]. Two different topologies are reported in [42]. Both of these topologies are derived from the same flux balance equation. However, the topology 1 is a new topology that came out of this theory. The detailed synthesis method for topologies 1 and 2 are discussed here.

### *1) Topology 1:*

Conventional Quadratic boost topology is discussed in [41]. The basic quadratic boost voltage conversion equation is given by

TABLE VI
POSSIBLE TERMS FOR CONVERSION RATIO $1/(1\text{-}D)^2$

| Converters | $f_{11}$ | $f_{12}$ | $f_{21}$ | $f_{22}$ |
|---|---|---|---|---|
| 1 [new] | $V_{in}$ | $V_{in}$-$V_{C1}$ | $V_{in}$+$V_{C1}$ | $V_{in}$-$V_{C2}$ |
| 3 [41] | $V_{in}$ | -$V_{C1}$ | $V_{in}$+$V_{C1}$ | $V_{in}$+$V_{C1}$-$V_{C2}$ |
| 2 [42] | $V_{in}$ | $V_{in}$ -$V_{C1}$ | $V_{C1}$ | $V_{C1}$-$V_{C2}$ |

$$V_{C2} = \frac{1}{D'^2}.V_{in} = \frac{1}{D'}.\frac{V_{in}}{D'} = \frac{1}{D'}.V_{C1} \quad (28)$$

Where

$$V_{C1} = \frac{1}{D'}.V_{in} \quad (29)$$

Using the above two equations, the volt-sec balance equations across the two inductors can be derived. Depending on the way the volt-sec equations are written, it leads to different $f_{11}$, $f_{12}$, $f_{21}$, and $f_{22}$ functions. Thus, it leads to different topologies. Using (29) with the substitution ($D$+$D$') = 1

$$V_{C1}.D' = D.V_{in} + D'.V_{in}$$
$$\Longrightarrow D.V_{in} + D'.(V_{in} - V_{C1}) = 0 \quad (30)$$

For the volt-sec balance equation for the second inductor, let's start from (28) with the substitution ($D$+$D$') =1

$$V_{C2} = \frac{1}{D'}.V_{C1}$$
$$\Longrightarrow V_{C2} = \frac{(D + D')}{D'}.V_{C1}$$
$$\Longrightarrow V_{C2}.D' = D.V_{C1} + D'.V_{C1} = D.V_{C1} + V_{in}$$
$$\Longrightarrow V_{C2}.D' = D.V_{C1} + D.V_{in} + D'.V_{in}$$
$$\Longrightarrow D.(V_{in} + V_{C1}) + D'.(V_{in} - V_{C2}) = 0 \quad (31)$$

(30) and (31) corresponds to $f_{11} = V_{in}$, $f_{12} = (V_{in}$-$V_{C1})$, $f_{21} = (V_{in}$+$V_{C1})$, and $f_{22} = (V_{in}$-$V_{C2})$. Fig. 13 (a) and (b) show the linear circuits formed by (30) and (31), respectively. Fig. 13 (c) shows the new Q boost topology. Experimental results verifying the circuit operation at $D$ = 0.4 and $D$ = 0.7 are shown in Fig. 14 (a) and (b), respectively. Steady-state waveforms of PWM signal for switch $D_{sw1}$, voltage across $L_1$ ($v_{L1}$), output voltage ($V_{C2}$), and inductor current ($I_{L1}$) are shown. Experimental parameters are identical to that reported for Q-buck boost converter.

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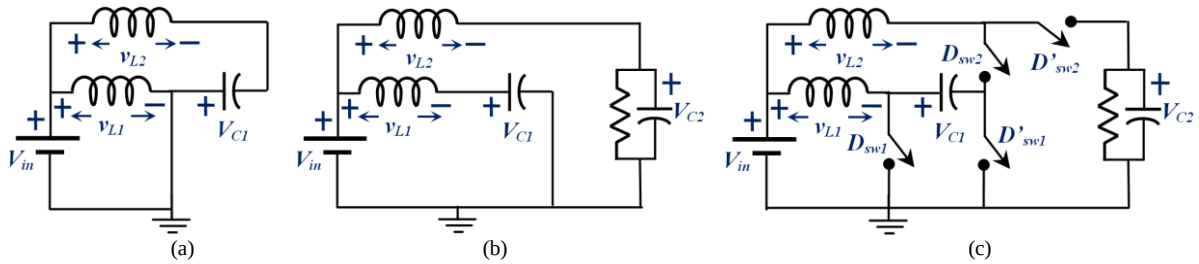


Fig. 13. (a) D Interval of Q Boost Topology 1, (b) D' Interval of Q Boost Topology 1, and (c) Q Boost Topology 1.

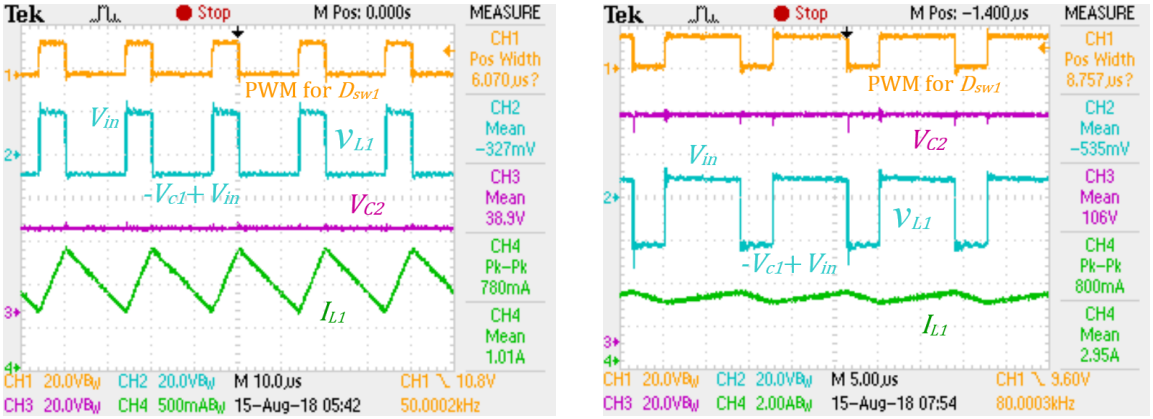


Fig. 14. Experimental verification of proposed Q Boost topology with (a) $V_{in}$= 20 V, $D$=0.3, and $R_o$= 21 Ω at $F_s$=50 kHz, and (b) $V_{in}$= 10 V, $D$=0.7, and $R_o$= 280 Ω at $F_s$=80 kHz. Experimental parameters: $L_1, L_2$: 160 µH; and $C_1$, $C_2$: 300 µF. Component Specifications: $D_{sw1}$, $D_{sw2}$: Rohm-SCT3120AL MOSFETs; $D'_{sw1}$, $D'_{sw2}$: C3D10060A diodes.

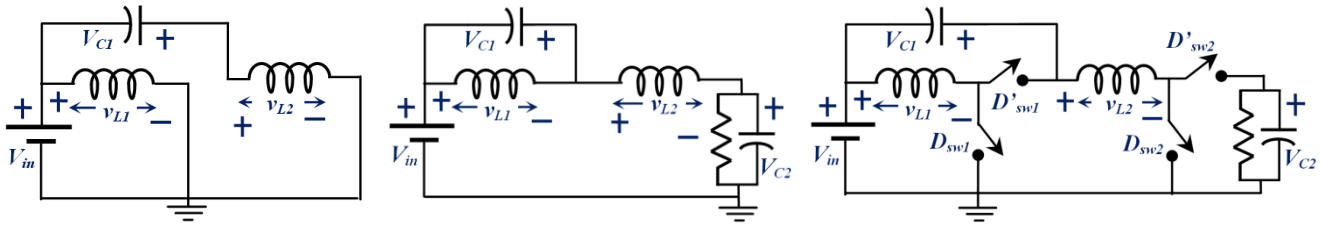


Fig. 15. (a) D Interval of Q Boost Topology 2, (b) D' Interval of Q Boost Topology 2, and (c) Q Boost Topology 2.

### 2) *Topology 2:*

For the second quadratic Boost topology [41], let's start from the basic voltage conversion equation

$$V_{C2} = \frac{1}{D'^2}.V_{in}$$

$$\Longrightarrow D'.V_{C2} = \frac{1}{D'}.V_{in} = \frac{D}{D'}.V_{in} + V_{in} = V_{C1} + V_{in} \qquad (32)$$

Where

$$V_{C1} = \frac{D}{D'}.V_{in} \qquad (33)$$

Using the above two equations, the volt-sec balance equations across the two inductors can be derived. Depending on the way the volt-sec equations are written, it leads to different $f_{11}$, $f_{12}$, $f_{21}$ and $f_{22}$ functions. Thus, it leads to different topologies. Using (33) with the substitution $(D+D')$ =1

$$V_{C1}.D' = D.V_{in}$$

$$\Longrightarrow D.V_{in} - D'.V_{C1} = 0 \qquad (34)$$

For the volt-sec balance equation for the second inductor, let's start from (32) with the substitution $(D+D')$ = 1

$$D'.V_{C2} = V_{C1} + V_{in}$$

$$\Longrightarrow D'.V_{C2} = (D + D')\,V_{C1} + (D + D')\,V_{in}$$

$$\Longrightarrow D.(V_{in}+V_{C1}) + D'.(V_{in}+V_{C1}-V_{C2}) = 0 \qquad (35)$$

(34) and (35) corresponds to $f_{11} = V_{in}$, $f_{12} = (-V_{C1})$, $f_{21} = (V_{in}+V_{C1})$, and $f_{22} = (V_{in}+V_{C1}-V_{C2})$. Fig. 15 (a) and (b) show the

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linear circuits formed by (34) and (35). Fig. 15 (c) shows the Q boost topology reported in [41].

## VII. Conclusion

This paper describes a theory to synthesize non-isolated DC-DC converters from a specified gain. It uses the principle of inductor volt-sec balance to find the range of possible converter configurations. The procedure is first applied to first order converters. The total number of possible first-order converter topologies is 48. Among these topologies, four are identified as basic topologies, and the remaining are either complementary, inverse, negative, or combination of the basic topologies. The principle is also extended to second-order converters. The expression for second-order gain is derived. Various symmetries among second-order converters, cascade decomposition of a second order converter into two first-order converters, and conditions for degeneration to first order gain, etc., are described. It is also seen that different flux balance equations may lead to same converter gain. In second-order converters, there is a very large number of possible configurations. Hence, it is important to synthesize a converter from the required gain expression. The procedure is general enough to synthesize a topology from a given voltage conversion equation. To demonstrate the effectiveness of the procedure, the method is applied to synthesize several new configurations with quadratic gain. The feasibility of these new configurations is verified experimentally.

## Appendix

In this section, the proposed Quadratic Buck-Boost Converter topologies are compared with the quadratic buck-boost converters presented in [35] and [36]. The performances of the proposed converters are compared with those proposed in [35] and [36] in terms of the voltage stress across the switches and current stress (peak and RMS current flowing through the switches), which is reported in Table A.

Table A
Performance Comparison of Quadratic Buck-Boost Converters

| | | Quadratic Buck-Boost Topologies | | | |
|---|---|---|---|---|---|
| | | Proposed Converter 1 | Proposed Converter 2 | Converter Proposed in [38] | Converter Proposed in [39] |
| Device Count | | 2 MOSFETs, 2 diodes | 2 MOSFETs, 2 diodes | 2 MOSFETs, 2 diodes * | 2 MOSFETs, 2 diodes |
| Voltage Stresses | Switch 1: | $\frac{1}{1-D}V_{in}$ | $\frac{1}{1-D}V_{in}$ | $\frac{1}{1-D}V_{in}$ | $\frac{1}{1-D}V_{in}$ |
| | Switch 2: | $\frac{D}{(1-D)^2}V_{in}$ | $\frac{D}{(1-D)^2}V_{in}$ | $\frac{1-2D}{(1-D)^2}V_{in}$ | $\frac{D}{(1-D)^2}V_{in}$ |
| | Diode 1: | $\frac{1}{1-D}V_{in}$ | $\frac{1}{1-D}V_{in}$ | $\frac{1}{1-D}V_{in}$ | $\frac{1}{1-D}V_{in}$ |
| | Diode 2: | $\frac{D}{(1-D)^2}V_{in}$ | $\frac{D}{(1-D)^2}V_{in}$ | $\frac{D}{(1-D)^2}V_{in}$ | $\frac{D}{(1-D)^2}V_{in}$ |
| | DC link | $\frac{1}{1-D}V_{in}$ | $\frac{D}{(1-D)^2}V_{in}$ | $\frac{D}{1-D}V_{in}$ | $\frac{D}{1-D}V_{in}$ |
| Current Stresses | Switch 1: | $\frac{D^3V_{in}}{R(1-D)^4}+\frac{DV_{in}}{2L_1F_s}$ | $\frac{D^3V_{in}}{R(1-D)^4}+\frac{DV_{in}}{2L_1F_s}$ | $\frac{D\,V_{in}}{R(1-D)^4}+\frac{V_{in}D}{2F_s}\left[\frac{1}{L_1}+\frac{D}{(1-D)L_2}\right]$ | $\frac{D^3V_{in}}{R(1-D)^4}+\frac{V_{in}D}{2F_s}\left[\frac{1}{L_1}+\frac{1}{(1-D)L_2}\right]$ |
| | Switch 2: | $\frac{D^2V_{in}}{R(1-D)^3}+\frac{D^2V_{in}}{2(1-D)L_2F_s}$ | $\frac{D^2V_{in}}{R(1-D)^3}+\frac{D^2V_{in}}{2(1-D)L_2F_s}$ | $\frac{D^2\,V_{in}}{R(1-D)^3}+\frac{D^2\,V_{in}}{2(1-D)\,L_2F_s}$ | $\frac{D^2\,V_{in}}{R(1-D)^3}+\frac{D\,V_{in}}{2(1-D)\,L_2F_s}$ |
| | Diode 1: | $\frac{D^3V_{in}}{R(1-D)^4}+\frac{DV_{in}}{2L_1F_s}$ | $\frac{D^3V_{in}}{R(1-D)^4}+\frac{DV_{in}}{2L_1F_s}$ | $\frac{D^3V_{in}}{R(1-D)^4}+\frac{DV_{in}}{2L_1F_s}$ | $\frac{D^3V_{in}}{R(1-D)^4}+\frac{V_{in}D}{2F_s}\left[\frac{1}{L_1}+\frac{1}{(1-D)L_2}\right]$ |

| | | | | | |
|---|---|---|---|---|---|
| | Diode 2: | $\frac{D^2V_{in}}{R(1-D)^3}+\frac{D^2V_{in}}{2(1-D)L_2F_s}$ | $\frac{D^2V_{in}}{R(1-D)^3}+\frac{D^2V_{in}}{2(1-D)L_2F_s}$ | $\frac{D^2V_{in}}{R(1-D)^3}+\frac{D^2V_{in}}{2(1-D)L_2F_s}$ | $\frac{D^2V_{in}}{R(1-D)^3}+\frac{DV_{in}}{2(1-D)L_2F_s}$ |
| RMS Current | Switch 1: | $\frac{D^3V_{in}}{R(1-D)^4}\sqrt{D+\frac{D}{3}\left[\frac{R(1-D)^4}{2L_1F_sD^2}\right]^2}$ | $\frac{D^3V_{in}}{R(1-D)^4}\sqrt{D+\frac{D}{3}\left[\frac{R(1-D)^4}{2L_1F_sD^2}\right]^2}$ | $\frac{DV_{in}}{R(1-D)^4}\sqrt{D+\frac{D}{3}\left[\frac{R(1-D)^4}{2F_s}\left[\frac{1}{L_1}+\frac{D}{(1-D)L_2}\right]\right]^2}$ | $\frac{D^3V_{in}}{R(1-D)^4}\sqrt{D+\frac{D}{3}\left[\frac{R(1-D)^4}{2D^2F_s}\left[\frac{1}{L_1}+\frac{1}{(1-D)L_2}\right]\right]^2}$ |
| | Switch 2: | $\frac{D^2V_{in}}{R(1-D)^3}\sqrt{D+\frac{D}{3}\left[\frac{R(1-D)^2}{2L_2F_s}\right]^2}$ | $\frac{D^2V_{in}}{R(1-D)^3}\sqrt{D+\frac{D}{3}\left[\frac{R(1-D)^2}{2L_2F_s}\right]^2}$ | $\frac{D^2V_{in}}{R(1-D)^3}\sqrt{D+\frac{D}{3}\left[\frac{R(1-D)^2}{2L_2F_s}\right]^2}$ | $\frac{D^2V_{in}}{R(1-D)^3}\sqrt{D+\frac{D}{3}\left[\frac{R(1-D)^2}{2L_2F_sD}\right]^2}$ |
| | Diode 1: | $\frac{D^3V_{in}\sqrt{1-D}}{R(1-D)^4}\sqrt{1+\frac{1}{3}\left[\frac{R(1-D)^4}{2L_1F_sD^2}\right]^2}$ | $\frac{D^3V_{in}\sqrt{1-D}}{R(1-D)^4}\sqrt{1+\frac{1}{3}\left[\frac{R(1-D)^4}{2L_1F_sD^2}\right]^2}$ | $\frac{D^3V_{in}\sqrt{1-D}}{R(1-D)^4}\sqrt{1+\frac{1}{3}\left[\frac{R(1-D)^4}{2L_1F_sD^2}\right]^2}$ | $\frac{D^3V_{in}\sqrt{1-D}}{R(1-D)^4}\sqrt{1+\frac{1}{3}\left[\frac{R(1-D)^4}{2D^2F_s}\left[\frac{1}{L_1}+\frac{1}{(1-D)L_2}\right]\right]^2}$ |
| | Diode 2: | $\frac{D^2V_{in}\sqrt{1-D}}{R(1-D)^3}\sqrt{1+\frac{1}{3}\left[\frac{R(1-D)^2}{2L_2F_s}\right]^2}$ | $\frac{D^2V_{in}\sqrt{1-D}}{R(1-D)^3}\sqrt{1+\frac{1}{3}\left[\frac{R(1-D)^2}{2L_2F_s}\right]^2}$ | $\frac{D^2V_{in}\sqrt{1-D}}{R(1-D)^3}\sqrt{1+\frac{1}{3}\left[\frac{R(1-D)^2}{2L_2F_s}\right]^2}$ | $\frac{D^2V_{in}\sqrt{1-D}}{R(1-D)^3}\sqrt{1+\frac{1}{3}\left[\frac{R(1-D)^2}{2L_2F_sD}\right]^2}$ |

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**Soumya Shubhra Nag** (S'13-M'18) received B.E. in Electrical Engineering degree from Jadavpur University, Kolkata, India, in 2009, M.Tech., and Ph.D degree in Electrical Engineering from Indian Institute of Technology Kanpur, Kanpur, India, in 2011 and 2017, respectively.

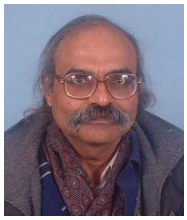
He was working as a Research Fellow in Rolls-Royce Corporate Lab, Nanyang Technological University, Singapore from January, 2017 till July, 2018. He is currently working as an Assistant Professor at Institute of Technology Delhi, New Delhi, India. His research interests include power electronic converters and PWM control techniques, transportation electrification, DC distribution system, renewable energy system.

**Ramanuja Panigrahi** (S'16) received a B.Tech. degree from Biju Pattnaik University of Technology, Odisha, India, in 2013 and an M.Tech. degree in Electrical Engineering from the Indian Institute of Technology Kanpur, Kanpur, India, in 2016, where he is currently working towards the Ph.D. degree.

His research interests include design and control of power converters, energy harvesting, power electronics for advanced grid functionality, and integration of PVs in secondary distribution network.

**Santanu K. Mishra** (S'00-M'04-SM'12) received a B.Tech. degree in Electrical Engineering from the College of Engineering and Technology, Bhubaneswar, India, in 1998, an M.Tech. degree in Energy Systems Engineering from Indian Institute of Technology, Chennai, India, in 2000, and the Ph.D. degree from the Department of Electrical and Computer Engineering, University of Florida, Gainesville, FL, USA, in 2006.

He worked as a senior application engineer with the International Rectifier Corporation in Rhode Island, USA, from 2004 to 2008. Currently, he is a MoSDE Chair Professor at the Indian Institute of Technology, Kanpur, India. During Fall of 2017, he was a Visiting Professor with Center for Power Electronics Systems (CPES), Virginia Tech., Blacksburg, VA, USA. His research interests include power converter design, implementation, control, and applications in rural scenario. He serves as an associate editor of several journals including *IEEE Transactions on Industry Applications*, *IEEE Transactions on Power Electronics*, *IEEE Consumer Electronics Magazine*, and *IET Power Electronics*.



Avinash Joshi received the Ph.D. degree in electrical engineering from the University of Toronto, Toronto, ON, Canada, in 1979.

He is currently a Professor Emeritus in Department of Electrical Engineering, Indian Institute of Technology Kanpur, Kanpur, India. From 1970 to 1973, he was with General Electric Company of India Ltd., Calcutta, India. His research interests include power electronics, circuits, digital electronics, and microprocessor systems.

**Khai D. T. Ngo** (S'82 - M'84 - SM'02 - F'15) received the B.S. degree from California State Polytechnic University, Pomona, in 1979, and the M.S. and Ph.D. degrees from the California Institute of Technology, Pasadena, in 1980 and 1984, respectively, all in electrical and electronics engineering.

He is currently a Professor of Electrical and Computer Engineering at Virginia Tech. He was a Member of Technical Staff at General Electric Corporate Research and Development Center, Schenectady, NY, from 1984 to 1988. Between 1988 and 2006, he was with the University of Florida, Gainesville. At Virginia Tech, he pursues technologies for integration and packaging of power passive and active components to realize building blocks for power electronic systems. These technologies lead to power conversion systems with higher efficiency and higher power density. He also focuses on topologies, control, emission, and integration issues for RF power converters. Other research interests include magnetic materials and components, energy reclamation, and power integrated circuits.

**Suman Mandal** was born in Bankura, India in 1990. He received the B.E. degree in Electrical Engineering from Jadavpur University, Kolkata, India in 2013. He received the M.Tech. degree in Electrical Engineering from IIT Kanpur, Kanpur, India in 2016. He is currently working towards the Ph.D. degree in the Department of Electrical Engineering from IIT Bombay, Mumbai, India.

His current research interests include converters for power transmission and distribution system and micro-grid, renewable energy system, etc.