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Title: On-chip Miniaturized Antenna in CMOS Technology for Biomedical Implant

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Abstract

Bioimplant devices need to be small to be considered safe. At the same time, one of the major challenges in its design is the size and lifetime of the battery. Therefore, replacing the battery with a miniaturized and integrated wireless power harvester aid the design of sustainable biomedical implants in smaller volumes. This study presents the design of on-chip miniaturized antenna in CMOS technology at 900 MHz for RF energy harvesting system-on-chip (SoC) application. The design approach utilizes 0.18 μm CMOS technology from SilTerra. Effect of the thickness of the SiO_2 substrate to the return loss and gain of the antenna has been evaluated. It is found that thicker substrate provides a better response, but subject to manufacturability of selected process technology. The developed antenna only occupied an area of 700 × 550 μm². The antenna has been fabricated along with integrated matching circuit and rectifier. The measured performance of the antenna deviates from simulation due to parasitic interaction between the antenna and matching circuit structure. This work shows a complete workflow from design consideration to fabrication and

measurement setup of CMOS antenna that will not only be applicable to 0.18 μm CMOS, but to other CMOS technology as well.

Keywords—RF energy harvesting, CMOS antenna, on-chip antenna, miniature antenna, RF CMOS, rectenna

1. Introduction

Bioimplants devices become advanced in accuracy and performance with the rapid progress in nanoelectronics and sensing technologies. They are not only for sensing and diagnosing, but can also deliver an appropriate drug dose as an autonomous implantable treatment [1]. Furthermore, implantable devices can send electric signals directly to the brain or to body organs with next generation bioelectronic treatments [2]. The most challenging aspects of these implantable microsystem are the devices lifetime and size, which are determined by the battery lifetime and the battery size, respectively. The external battery can be replaced by an integrated wireless RF energy harvesting system that can collect electromagnetic energy and convert it to a DC supply voltage, powering the circuits of the implants. This enable a miniaturized, battery-less device that is powered wirelessly to a remote reader, similar to RFID systems.

There are several previous research work on integrated antenna on a CMOS chip but most designs targeting very high frequencies to achieve small antenna dimensions [3-7]. Due to heavy absorption of signals in the human body, generally frequencies below 1 GHz have to be used since it has longer wavelengths [8]. This poses a design challenge in antenna miniaturization. In [9], an implantable eye-monitoring implant uses an 27 mm long off-chip monopole antenna that is too long to be considered safe for implant. In [10], the same problem has also been addressed in which antennas are too bulky for proper consideration to be implantable. Therefore, in this paper, an on-chip antenna based on CMOS technology at sub 1 GHz is proposed. An on-chip design means that the antenna itself can be fitted into a system on chip (SoC), thus making the whole system more compact, integrated and more suitable for bio-implantation.

2. Methodology

2.1 Materials

In this work, 0.18 µm RF CMOS process technology from SilTerra is utilized. The standard layering used are Metal-Insulated-Metal (MIM) as shown in Fig. 1(a). In standard manufacturing process, the top aluminum metal, M6 is the thickest at < 1 µm while the intermetals (M5-M1) are < 0.6 µm. The metal layers are separated by an insulator, Silicon Dioxide (SiO_2) which have a relative permittivity of 4.2 and thickness of < 0.6 µm. For antenna design purpose, any SiO_2 layers can be replaced with metal and vice versa. Furthermore, different metal layers can be joint using via if desired. The metal and SiO_2 layers are placed on top of a silicon substrate with thickness of 250 µm and relative permittivity of 11.9.
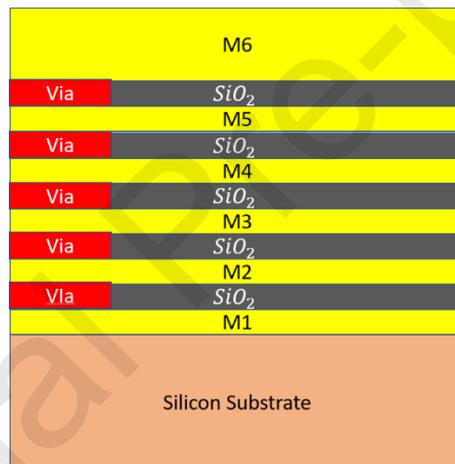

Fig. 1: The standard CMOS 0.18 µm stack-up

2.2 Design rules

CMOS technology for SoC design is limited to a few millimeter-sized design [11]. To miniaturize an antenna design for sub 1 GHz frequency, one thing to note is that it will be electrically small and will radiate in either electric or magnetic near field. Magnetic coupling is chosen over electric coupling as it is not affected when applied in human tissue [12]. This is due to reactive energy in the magnetic field mostly affected by high magnetic permeability, while the permeability of human tissue is practically equal to the magnetic permeability of

air. Therefore, the performance of magnetic coupled near field antenna in air and in human tissue should be the same, which is crucial considering biomedical purposes.

It was shown in the Maxwell-Faraday's equation that magnetic coupling can be induced by using a loop antenna, in which a time varying magnetic field that hit the normal plane of the loop induced an electromotive force along the loop. Thus, loop antenna is being considered. However, for further tuning in the sub 1 GHz range, a single loop is not sufficient, therefore the loop is modified into a spiral in which the number of turns can be manipulated to tune the frequency of the antenna. One end of the spiral is connected to the antenna feed while the other side is terminated through the ground. The electrical representation of the antenna is thus as shown in Fig. 2. The loop antenna itself is equivalent to an LC circuit, but since the overall structure consisted of a MIM layers, thus there are also parallel inductance from connecting vias as well as distributed capacitance between the substrate layers.
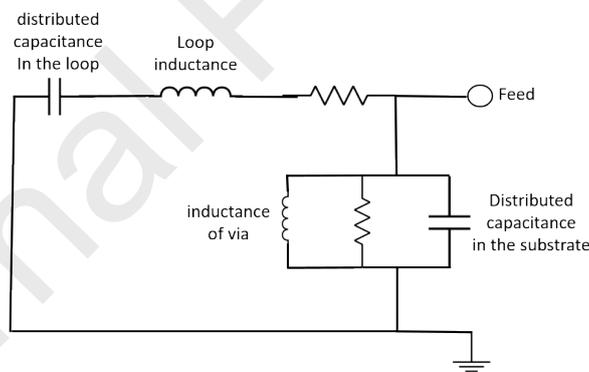

Fig. 2: Equivalent circuit model of a single loop.

The spiral is implemented as a slot, considering that slot have been well known and widely used to decrease resonant frequency of an antenna. Fig. 3(a) shows a spiral with 3 turns, to explain the basic construction of the spiral. The width of the slot is kept constant along the loop at $a = 2$ μm, while the gap between the slot spiral is kept constant at $b = 4$ μm. The optimized total number of turns is 27 turns for a pair of spiral slots as shown in Fig. 3(b).

The feed is located at each end of both slots as shown in Fig. 3(b). This design only utilizes three metal layers which are M6 for the antenna geometry and M1 for the ground, while M3 is used to connect the feed to the GSGSG pads, as shown in Fig.4(a). Figure 4(b) shows the view of the antenna in Computer Simulation Technology (CST) Microwave Studio for modelling and simulation purposes.

GSGSG pads are modelled to match the measurement probe station's standard. The dimension of each pad is 68.61 μm on each side and the distance between each pad is 150 μm from its center. A surrounding ground-ring is used to setup the excitation scheme. This setup comes close to the actual on-wafer conditions where the GSGSG probe tips excite the structure from the top . This setup is shown in Fig. 4(b) and Fig. 5, in which a vertical PEC bridge connects three ground (G) conductors together and the lumped ports (S) are used to excite the structure, as explained in [13]. Each lumped ports (S) is connected to one end of the port location as pointed in Fig. 3(b) through a connecting path constructed of metals and vias. Meanwhile, the PEC ground (G) is directly connected to the antenna's ground. The input impedance of the ports is set to 50 Ω to match the standard input impedance of the measuring probe. The overall area is set to be not exceeding 2 mm × 2 mm. This is to keep an overall compact design suitable for biomedical implant.

(a)   (b)

Fig. 3: (a) A close-up of a spiral with 3 turns, and (b) two spiral slot each with 27 turns on an aluminum top metal M6

(a)   (b)

Fig. 4: (a) The layering configuration used for the proposed antenna structure, and (b) antenna model in CST showing the surrounding ground-ring setup for feed excitation

Fig. 5: CST setup for the surrounding ground-ring excitation. Lumped ports lie across the gap between the PEC ground bridge and pad location.

3. Parametric study on the effect of SiO$_2$ thickness

As mentioned in Section 2.2, the design only utilizes three metal layers which are M6, M3 and M1. However, M3 can be neglected as its purpose is only to connect the source pad from GSGSG pad to the input feed of the antenna. Thus, only M6 and M1 are considered to be the main metal layers, and this means that the thickness of the SiO$_2$ substrate between these two layers can be adjusted to fill the space for remaining unused metal layers. The effect of SiO$_2$ thickness on the S-parameter and gain is shown in Fig 6 and Fig. 7, respectively. These figures suggest that a thicker layer of SiO$_2$ between M6 and M1 gives a better response for both S-parameter and realized gain. The bandwidth of the antenna significantly increases as the SiO$_2$ thickness increases. The rate of bandwidth increment has a mean of 0.65 GHz per 8.25 µm increment of SiO$_2$ thickness. However, this is only true for the thickness of 4.2 µm and higher, as the return loss shows a 0 dB reading when the SiO$_2$ thickness is lower than 4.2 µm.
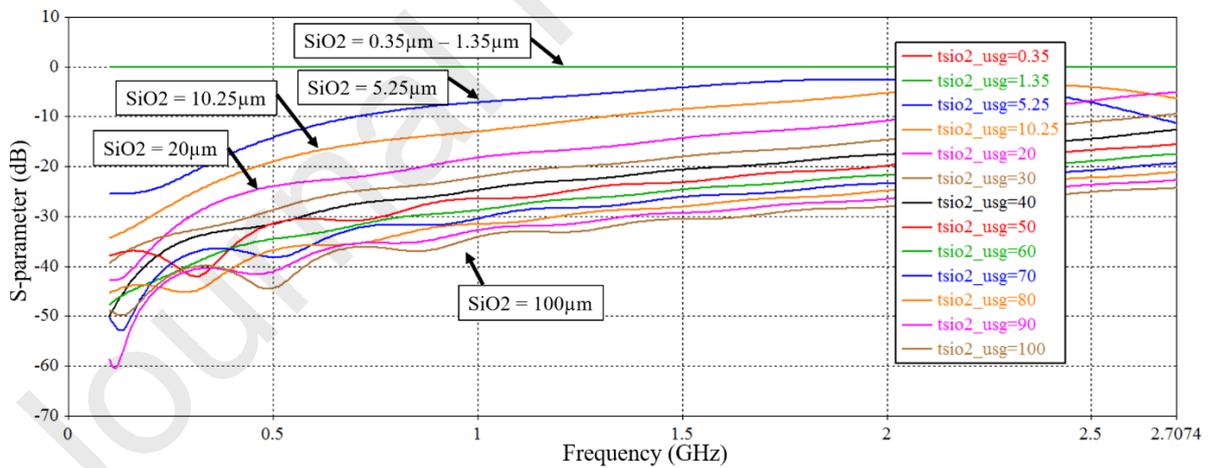

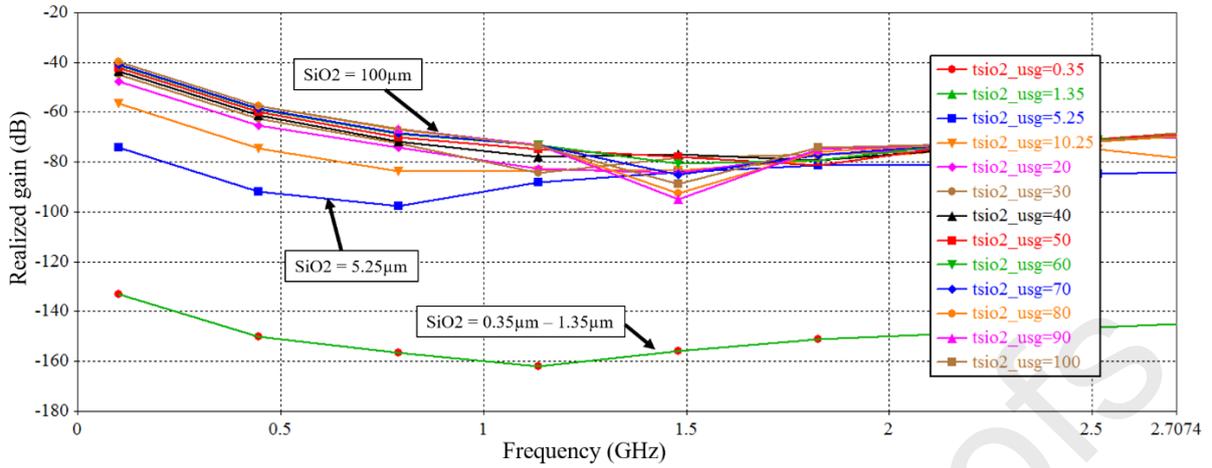Fig. 6: The simulated S-parameter for thickness of SiO$_2$ ranging from 0.35 µm to 100 µm.

Fig. 7: The simulated gain for thickness of SiO_2 ranging from 0.35 µm to 100 µm.

4. Manipulating number of turns for frequency tuning

The effect of adding and reducing the number of turns on the spiral-slot antenna can be viewed in Fig. 8. It is seen that when the number of turns is increased from 15 turns to 20 turns, the bandwidth moves to the left side, or to the higher frequency. This is desirable as it enables the bandwidth to include the frequency of interest. This holds true up to 27 turns. However, when further increased to 30 turns and above, the resonant bandwidth moves back to lower frequency, leaving the 900 MHz zone. Therefore, 27 number of spiral turns for the spiral slots is found to be optimal.
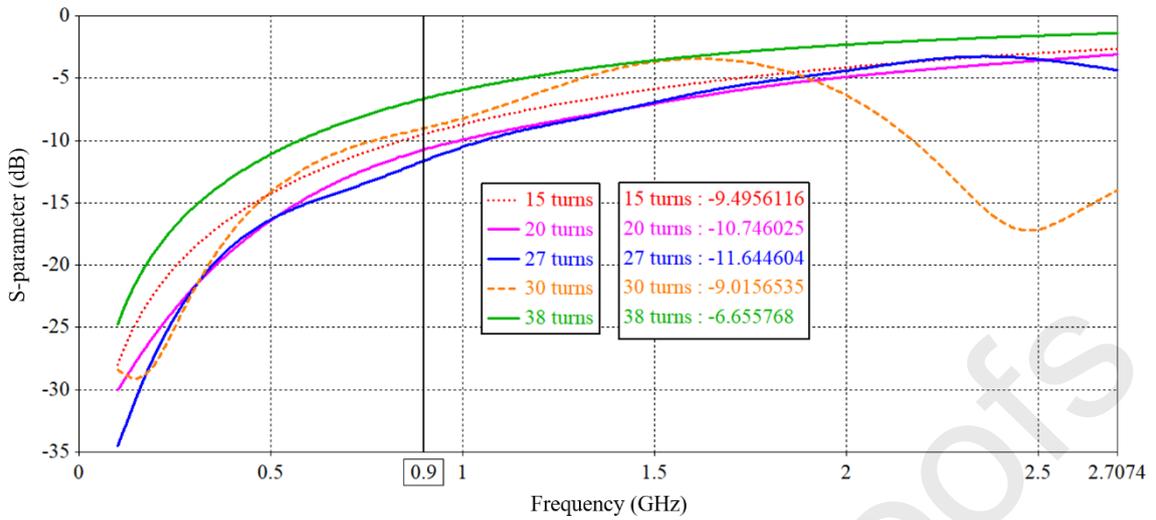
Fig. 8: The effect of adding and reducing the number of turns for spiral-slot antenna on the frequency.

5. Fabrication and measurement

For fabrication, the antenna design is being integrated with an on-chip impedance matching circuit and rectifier as shown in Fig. 9(a). The impedance matching is applied between the antenna and the rectifier to provide maximum energy transfer [14] to the circuit while the rectifier is to convert the RF signal captured by the antenna to a single DC voltage. The detail design procedure of the impedance matching circuit and rectifier has been presented in [15]. The SiO_2 thickness between M1 and M6 chosen for fabrication is 6.37 μm while the top metal (M1) thickness is 2.2 μm, and the ground (M1) thickness is 0.53 μm. It is to be noted that these thicknesses are chosen after considering the parametric study in previous section and compliance with the available manufacturing process. The layout of the integrated circuit is as seen in Fig. 9(b), while the fabricated chip under a microscope can be seen in Fig. 9(c). The total core area occupied by the whole chip is only 1998 × 1982.745 μm^2.

(a)

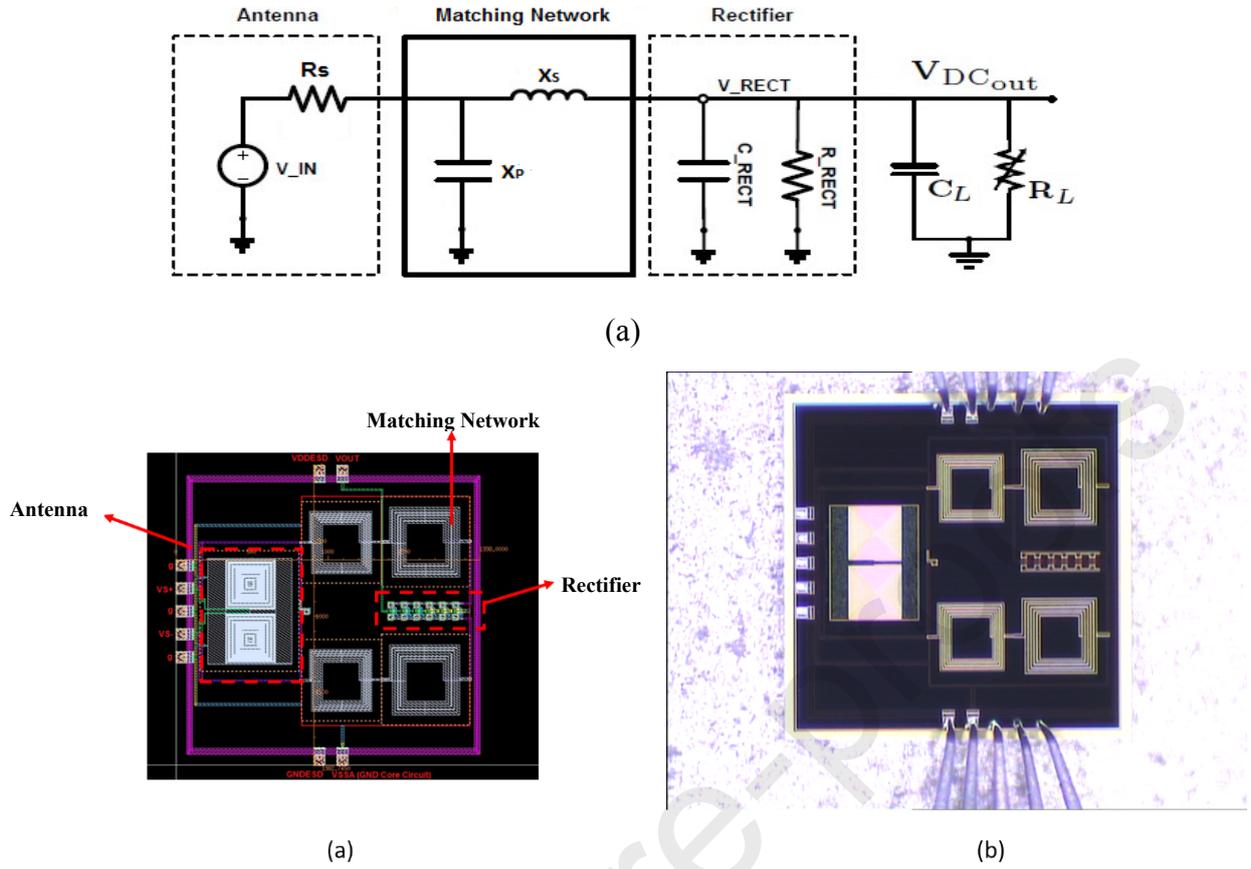(a)   (b)

Fig. 9: The integrated circuit (a) functional block diagram (b) layout and (c) micrograph of the fabricated chip.

Cascade Microtech Summit 9000 probe station are used to measure the characteristic of the antenna. The probe setup can be seen in Fig. 10(a). For return loss measurement, the probe is connected to a vector network analyzer (VNA). Meanwhile, to calculate the measured gain, a link budget based on Friis' transmission formula as shown in Eq. (1) is utilized:

$$P_r = P_t + G_t + G_r - L_p - P_{CL} \tag{1}$$

where;

P_r = power received by receiver antenna (dBm)

P_t = power transmitted by transmitter antenna (dBm)

G_t = gain of transmitter antenna (dB)

G_r = gain of receiver antenna (antenna under test) (dB)

L_p = free space path loss
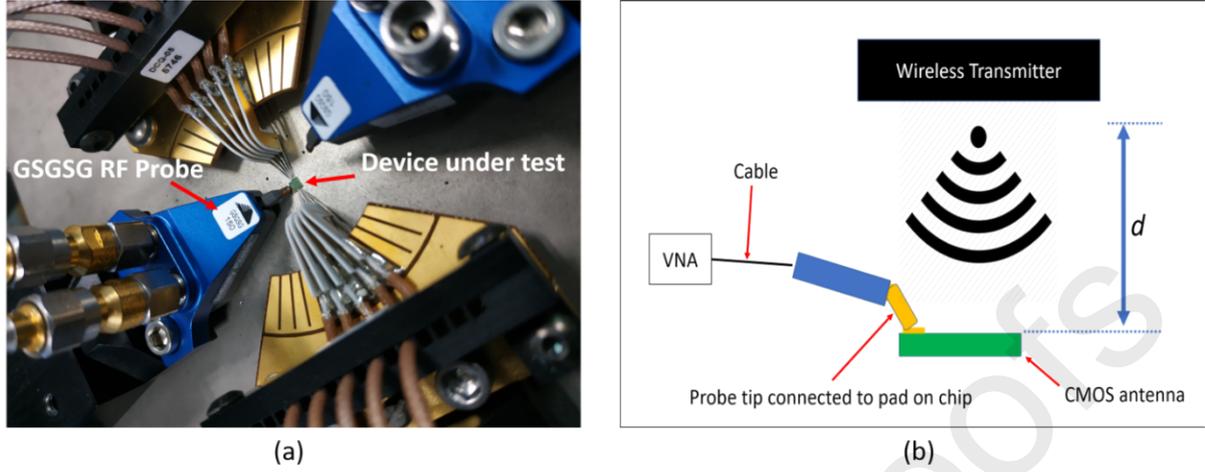
P_{CL} = cable loss (dBm)

Fig. 10: (a) Chip testing on probe station, and (b) setup of transmitting power to the antenna to measure the received power.

From Eq. (1), it can be seen that G_t, P_{CL}, and L_p are the unknowns which values need to be defined. To obtain G_t, an antenna with a known gain is used as transmitting antenna: in this case, a built-in antenna inside a PowerCast® transmitter with a gain of 27 dB is used to transmit 27 dBm of power towards the antenna by the distance d, which is as described in Fig. 10(b). Cable loss (P_{CL}) is obtained by connecting one end of the cable to a signal generator, and the other end to a signal analyzer. The power transmit is set to 0 dBm at the corresponding frequency on the signal generator, then the received power at the other end is viewed on the signal analyzer. The received power observed at the signal analyzer will show a decrease from the original input power at the signal generator. The difference in power is then defined as the cable loss, with measurement unit in dBm. Furthermore, the path loss, L_p, is the reduction in power density, or attenuation of an electromagnetic wave as it propagates through space. Path loss is defined by Eq. (2).

$$L_p = 34.21 + 20\log f + 20\log d \tag{2}$$

where,

L_p = path loss

f = operating frequency in Megahertz (MHz)

d = distance between the two antennas in kilometer

6. Measurement result

Fig. 11 shows the simulated and measured return loss plotted against frequency for the proposed CMOS spiral-slot antenna. It can be seen that for the measured return loss, major shifting of the resonating bandwidth occurs towards the right side of the graph. This difference between the simulated and measured result is most likely contributed by the on-chip inductors of the matching circuit. These inductors have not been considered in the antenna's simulation due to different design environments [15]. However, due its large surface area and spiral shape, along with the small area of the chip, it may also radiate under the illumination of signals from the wireless transmitter. Hence, it acts as a "parasitic antenna" which directly alter the response of the spiral-slot antenna.
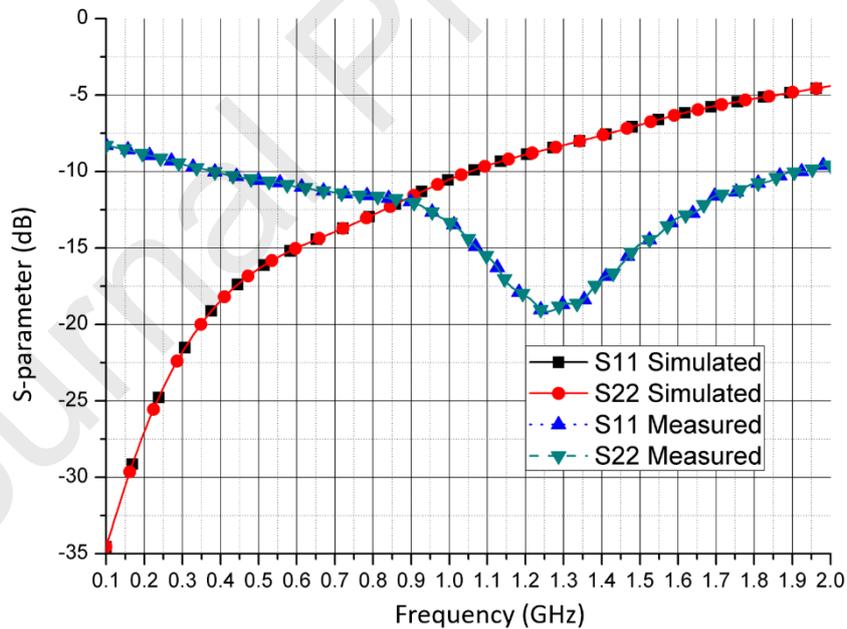

Fig. 11: The S-parameter of the proposed CMOS spiral-slot antenna.

The measured gain and received power for a distance between 5 to 15 cm between the chip and the transmitter at 900 MHz is shown in Table 1. Based on simulations in Section 3, the realized gain can be expected to be around -90 dB. However, as seen in Table 1, the

measured gain is higher compared to the expected gain, with a mean of -37.8 dB. This means that the measured gain is 40.84% better than the simulated gain. Again, this anomaly is highly suspected to be caused by the parasitic interaction between the proposed antenna structure and the on-chip inductors present in the chip. A total of 3 fabricated chips had been measured and gives quite consistent result as in Fig. 11 and Table 1.

Table 1: The measured gain and power received at 900 MHz.

Distance (cm)	Power received (dBm)	Gain (dB)
5	-13	-38.58
7	-17	-39.66
9	-17	-37.48
11	-18	-36.73
13	-20	-37.28
15	-21	-37.04
		Mean gain: -37.8

The radiation pattern measurement is heavily constrained by availability of a controlled facility. This is due to the anechoic chamber that was not designed to sustain the equipment for the probe station. Therefore, only the simulated data can be presented for the radiation pattern, as shown in Fig. 12. The simulated radiation pattern showed a uniform symmetry and is bidirectional in the *xz*-plane and *xy*-plane, while in the *yz*-plane the radiation is maximum.
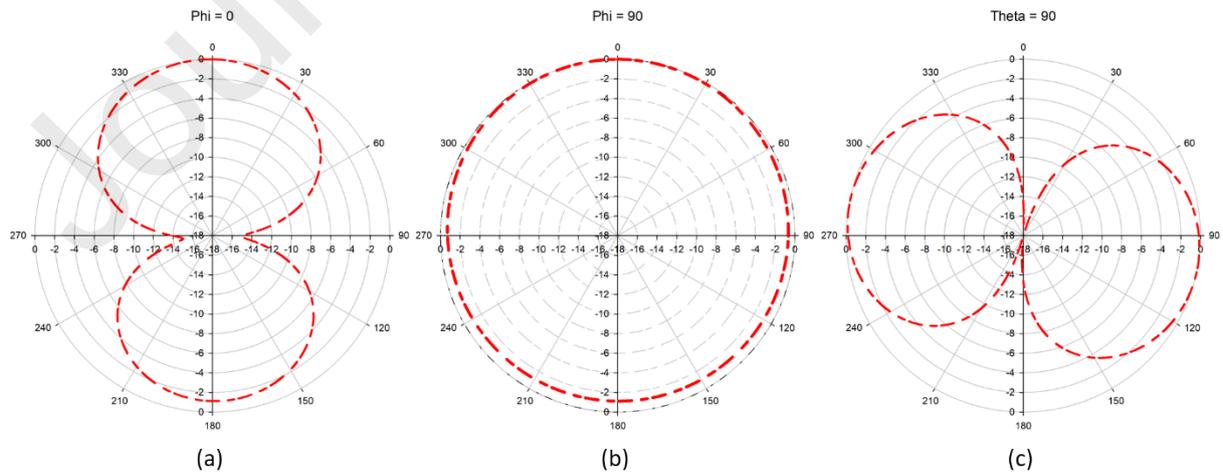

(a)   (b)   (c)

Fig. 12: The simulated radiation pattern at 900 MHz for (a) *xz*-plane, (b) *yz*-plane, and (c) *xy*-plane

Table 2 shows the comparison of recently published antenna using CMOS technology. The list has been restricted to only studies that has mentioned the application for biomedical implant. Thus, studies such as [16] and [17] are not included even though they involved studies for on-chip antenna but were not intended for biomedical purposes. From Table 2, it is seen that the proposed antenna has the smallest size at the lowest operating frequency. Implantable devices will benefit from lower frequency as the signal absorption is drastically reduced.

Table 2: Comparison of CMOS antenna design for implantable application.

Ref.	Antenna type	Technology	Frequency (GHz)	Area size	Gain (dB)
[9]	Curved monopole	Liquid crystal polymer attached to 0.13 μm CMOS	2.4	27 mm long	-6
[12]	On-chip loop antenna	0.13 μm CMOS	5	1 mm × 1 mm	-35
[18]	On-chip monopole	0.18 μm CMOS	5.2	3.2 mm × 1.5 mm	-14.5
[19]	Single loop antenna	0.35 μm CMOS	2.4	Not reported	-50.9
Proposed	Spiral slot antenna	0.18 μm CMOS	0.9	550 μm× 700 μm	-90

7. Discussions and suggestion for future work

Through Section 4 and 6, it is deduced that on-chip antenna is a very sensitive design. Since everything is very small scale in term of size and are placed in close proximity, the component can interact with each other and create undesirable noise that high likely affect each other's functions and performance. In some system, additional low noise amplifiers or other active parts will also be incorporated on the same chip. Therefore, the author highly suggests that any CMOS antenna to be designed hand in hand with its subsequent

components in the system. To do this, a finalized design of the entire system should be modelled and simulated in CST so that any effect to the antenna as well as other RF components can be observed and corrected accordingly. Additionally, a much reliable ways to measure the performance of on-chip CMOS antenna should be devised as this would lead to maturing of CMOS antenna technology.

8. Conclusion

In this paper, a miniaturized on-chip CMSO antenna at 900 MHz has been proposed for biomedical SoC RF energy harvesting. Through parametric investigation, it is found that the bandwidth of the antenna increased significantly as the SiO_2 substrate becomes thicker. The rate of bandwidth increment has a mean of 0.65 GHz per 8.52 μm increment of SiO_2 thickness. The antenna has been fabricated using SiO_2 thickness of 6.37 μm after considering fabrication requirement set by foundry and the measured S-parameter and gain show some deviation from the simulation and the possible cause and suggestion to overcome it has been discussed. A complete workflow of CMOS antenna design, fabrication and measurement has been presented. The proposed antenna is only 700 μm × 550 μm which makes it a great solution for implantable SoC devices.

Acknowledgements

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Declaration of interests

☒ The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

☐ The authors declare the following financial interests/personal relationships which may be considered as potential competing interests: