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Intrinsic Power Management Strategy based improvement of power stability in a single-phase AC–DC converter system

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ABSTRACT

Nowadays the size of the use of electronic devices like laptops, cell phone chargers, electric vehicles and UPS is rapidly increasing. So AC–DC converters need to incorporate the power factor correction along with voltage regulation. There are many AC–DC converter control methods available, but these methods do not perform well. Therefore In this paper, a smooth transformation on switching will be characterized by a high power factor in a single phase AC–DC converter by the use of intrinsic power management strategy. The proposed AC–DC converter's circuit topology is obtained by integrating a boost and buck converter. The Boost Converter's switching frequency does power factor correction to get less current harmonics at the input line. In this single phase AC–DC converter, the buck-boost converter is an important component that increases system power quality based on advanced PWM technique. So in this work, the Intrinsic Power Management Strategy (IPMS) is proposed to enhance the control over the DC–DC converter performance during unstable or transient operation. Rather than making a quick Pulse Width Modulation (PWM) signal, the computerized signal processor just creates a moderate changing DC signal to decide the PWM ramp function. The power factor correction model has been created and simulated by utilizing MATLAB programming. The simulation model demonstrates that the power factor is improved and the converter has regulated DC output voltage. To validate this simulation, a 1000 W prototype converter has been developed to feed a DC motor and the analysis of the results are presented.

1. Introduction

Nowadays single phase AC–DC converters are broadly utilized in power supplies, battery chargers for home apparatuses and Uninterrupted Power Supplies (UPS). Specifically, the power utilization of data innovation equipment has expanded quickly [1,2] Therefore, AC–DC converters are preferable to achieve high efficiency and low converter cost. The single phase AC–DC converter has been developed with a Power Factor Correction (PFC) and DC–DC Converter. The AC–DC front-end converter in the first stage is required in order to provide low-input-current harmonics so as to meet various standards. Therefore, a number of PFC converters and control methods have been investigated [3]. The simplest configuration of the ac–dc converter with a PFC function consists of a diode rectifier and a chopper circuit [4].

The basic block diagram of the AC–DC converter is shown in Fig. 1. However, the volume of the single-phase buck AC–DC converter becomes larger because the large inductor is required in order to decouple the power pulsation, which is subjected to the power supply frequency. Typically, boost-chopper type single-phase AC–DC converters require a large smoothing capacitor, such as electrolytic capacitors. Large electrolytic capacitors typically have a limited lifetime and increase the volume of the converter [5]. In contrast, for the same reason, buck chopper-type single-phase AC–DC converters require a large smoothing inductor at the dc link part. Since the energy storage density of an inductor is smaller than that of a capacitor, single phase buck AC–DC converters are larger than single-phase boost AC–DC converters. The basic concept is to use an active circuit to absorb the power pulsation from the dc link to other energy storage components, which permits a larger fluctuation of the voltage or current. Therefore, the value of energy storage components can be reduced.

So as to conquer this disadvantage, this work presents another single-phase buck type AC–DC converter with a power pulsation decoupling capacity. The proposed converter is developed dependent on a buck-boost type AC–DC topology for PFC utilizing a functioning buffer, which is made out of a single MOSFET switch. In

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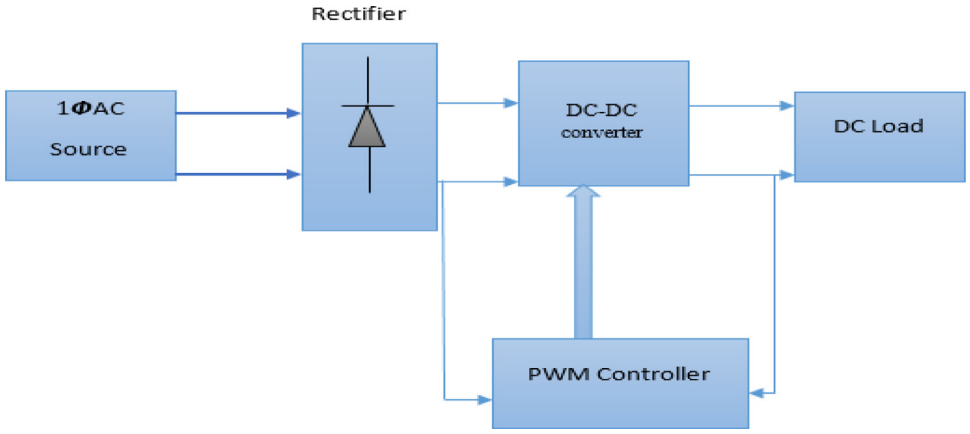


Fig. 1. Basic block diagram of AC–DC Converter.

other words, the proposed converter can control a sinusoidal current and can likewise control the low yield dc voltage swell without an enormous inductor or a huge capacitor. Therefore, the proposed converter has many advantages than conventional converters.

The remaining part of this paper is organized as, Section 2 discuss different types of existing AC–DC converter methods. Followed by section three discuss the working principle of proposed system. In section four, the simulation results and performance evaluation of proposed system are discussed. Finally section five discuss the conclusion.

2. Research background

AC grid and DC loads are essential equipment for AC–DC power converters to interface with modern industry applications. The AC–DC power converters have many applications, like Electric Vehicles, Telecommunication System and Variable Speed Drive systems [6,7]. Switching mode AC–DC converters with Power Factor Correction (PFC) are preferred nowadays in the industry to minimize the current harmonics injected into the AC grid and control the input power with the unity power factor. The galvanic isolation, which is required in applications such as EV battery chargers and telecom power supplies, is to ensure safety and reliability [8].

A high voltage DC bus, for example, the 400 V/dc is likewise profoundly required by these applications. Additional DC–DC converters are needed to expand the overall performance of the overall implementation. These applications can have load power at the range of 10 kW [9,10]. Usually, multiple single-unit modules can be used in parallel to make higher power availability. The single module power rating is around 5kW. The limit is primarily due to the ability of MOSFET current capacity as an LLC converter [11] just as the power limit of delicate switching DC–DC topology, generally utilized. The commercialized single-phase isolated AC–DC converters can be classified into two-stage conversion and single-stage conversion. It has a front-end, PFC level pursued by a confined DC–DC level. There should be two stages in the termination of a huge capacitor reserve.

The front end segment ordinarily utilizes a bridge rectifier to switch a boost or buck converter [12]. Some different topologies like a well-created phase-shifted full-bridge (PS-FB) converters are chosen on DC–DC phases of delicate transformation surfaces [13]. The benefit of this two-stage solution is that the PFC control and output voltage regulation are decoupled. Along these lines, PFC effectiveness can generally be ensured regardless of whether the information AC voltage and load limit changed [14].

A high DC rating converter inclines towards full-bridge (FB) based topologies for high power applications. Based on their circuit type, these converters can be classified buck-type [15], boost-type [16], resonant-type [17] and Dual-Active-Bridge (DAB)-type [18–20]. The buck-type FB AC–DC converter has a voltage source and full-bridge circuit on its input side and LC filter on its output side. Normally, a DC link capacitor is still required [21]. The function of a boost converter in a two-stage solution is integrated into the full-bridge circuit. Following the high frequency switching, the full-bridge can charge the input DC capacitor and regulate the voltage output at the same time.

Following high switching frequency, the whole bridge input DC capacitor charge and in the meantime voltage yield is directed. Boost-type AC–DC converter uses an input inductor on its input AC side which acts like the main boost inductor [22,23]. This switch capacity is a customary lift to the PFC circuit. In this way it has a critical THD reduction, also the yield diode voltage rating is low and since its yield side uses just the capacitors [24]. However, since the primary side DC bus also does not have any power efficiency, the leakage inductance of the transformer is hard to absorb energy. When the transition is unstable, high voltage overflow and large sounding take place for switches in place of choice. In order to solve this problem, additional adaptive circuits [25,26] or secondary side control [27,28] are used.

3. Materials and method

For improving the stability and power quality in a single phase AC–DC converter, an Intrinsic Power Management Strategy (IPMS) based controller has been implemented, this technique provides stabilized power in the AC to DC converter system with high efficiency. Fig. 2 shows the block diagram model of the proposed converter with the IPMS controller which effectively optimizes the error present in the conventional AC–DC converter system.

The proposed model has been tested and the dynamic performance of the proposed converter is analyzed. DC voltage stabilization and reduced switching losses are effectively optimized by the proposed Intrinsic Power Management Strategy (IPMS) based controller, by improving the performance of single-phase AC–DC converter based on parameters such as input power factor, voltage regulation, switching loss reduction and THD reduction.

3.1. Types of active power factor correction

There is a distorted input current waveform with increased harmonic content in the traditional off line converters with diode capacitor rectifier front-end. To meet the necessities of the above

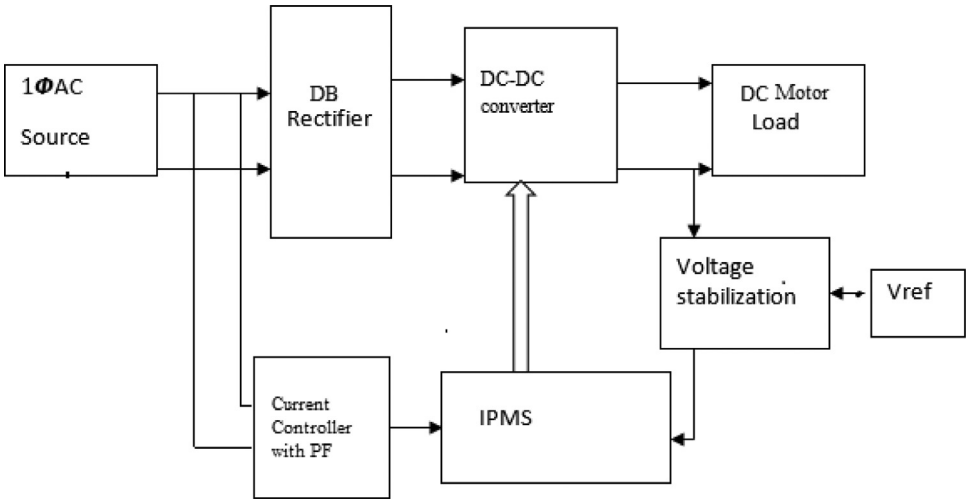


Fig. 2. Proposed block diagram for single phase AC–DC converter with DC Motor Load.

standards it is standard to include a power factor corrector in front of the separated DC–DC converter segment of the switching power supply. Again another DC–DC converter is required to get the regulated output voltage. In this way two converters are required for single-phase active power factor correction for the prerequisite of high input power factor and output voltage regulation. So in active power factor correction, there are two methodological approaches

a. **Single stage approach**
b. **Two stage approach**

The two-stage methodology is ordinarily utilized method as a part of high power applications. There are two independent power stages in the two stage approach. The frontend PFC stage is normally a boost or buck-boost or fly back converter. The DC–DC output stage is the isolated one that is executed with no less than one switch, which is controlled by an independent PWM controller to firmly regulate the output voltage. The two-stage methodology is a financially saving approach in high power applications. Its cost is more in low power applications because of the extra PFC power stage and control circuits.

A single stage plan combines the PFC circuit and DC–DC power conversion circuit into one stage. Various single-stage circuits have been accounted for lately. Contrasted with the Two-stage approach, the single stage methodology uses to stand out switch and controller to shape the input current and to regulate the output voltage. Despite the fact that for a single stage PFC converter attenuation of input current harmonics is not comparable with the two-stage approach.

3.2. Proposed buck-boost converter with PMDC motor control system

In this paper, the Intrinsic Power Management Strategy (IPMS) technique has been utilized for the DC motor control. The functional circuit diagram of the proposed system is shown in Fig. 3. The IPMS performance is judged by a linear model of the DC motor via MATLAB simulations and IPMS performance is compared with traditional controllers.

As a result of the simulation, the IPMS shows that this control is a better controller than a PID controller. The IPMS can adapt itself to the parameter variations and external disturbances, the problem of the chattering parameter, resulting from the discontinuous controller, is handled by sliding with smooth control action.

3.3. Modeling of DC motor

The functional circuit diagram of the DC motor drive model is shown in Fig. 4. These circuits comprise two parts, the first part is DC–DC converter and the second part is an equivalent of PMDC motor. The linear relationship between the back emf and speed is calculated as

$$\omega = \frac{E_b}{k_e \emptyset} \tag{1}$$

where $E_b = k_e \emptyset \omega$

$$T = k_e \emptyset I_a \tag{2}$$

where $k_e = \frac{\rho Z}{2\pi A}$

The torque function of the motor is calculated by using Eq. (3)

$$T = J.\frac{d\omega}{dt} + B\omega \tag{3}$$

The linear relationship between the back emf and armature voltage *Va* is calculated as

$$V_a = R_a i_a + L_a \frac{di_a}{dt} + E_b \tag{4}$$

$$\omega = -\frac{B}{J}\omega + \frac{k_t}{J} i_a \tag{5}$$

$$i_a = -\frac{k_a}{L_a}\omega + \frac{R_a}{L_a} i_a + \frac{1}{L_a} v_a \tag{6}$$

$$v_a = -\frac{1}{C} i_a + \frac{1}{C} i_L \tag{7}$$

$$i_L = -\frac{1}{L} v_a + \frac{v_{in}}{L} u \tag{8}$$

where

L = Inductance of Converter circuit (H)
C = Capacitance of Converter circuit (F)
R_a = Resistance value of Armature (Ω)
L_a = inductance value of Armature (H)
J = Value of Inertia constant (Nms^2/rad)
B = constants of Friction (Nms/rad)
E_b = Back emf value (V)
k_e = constant of Back emf t ($V\ s/rad$)
k_t = constant value of Torque (Nm/A)
V_{in} = Input Voltage (V)

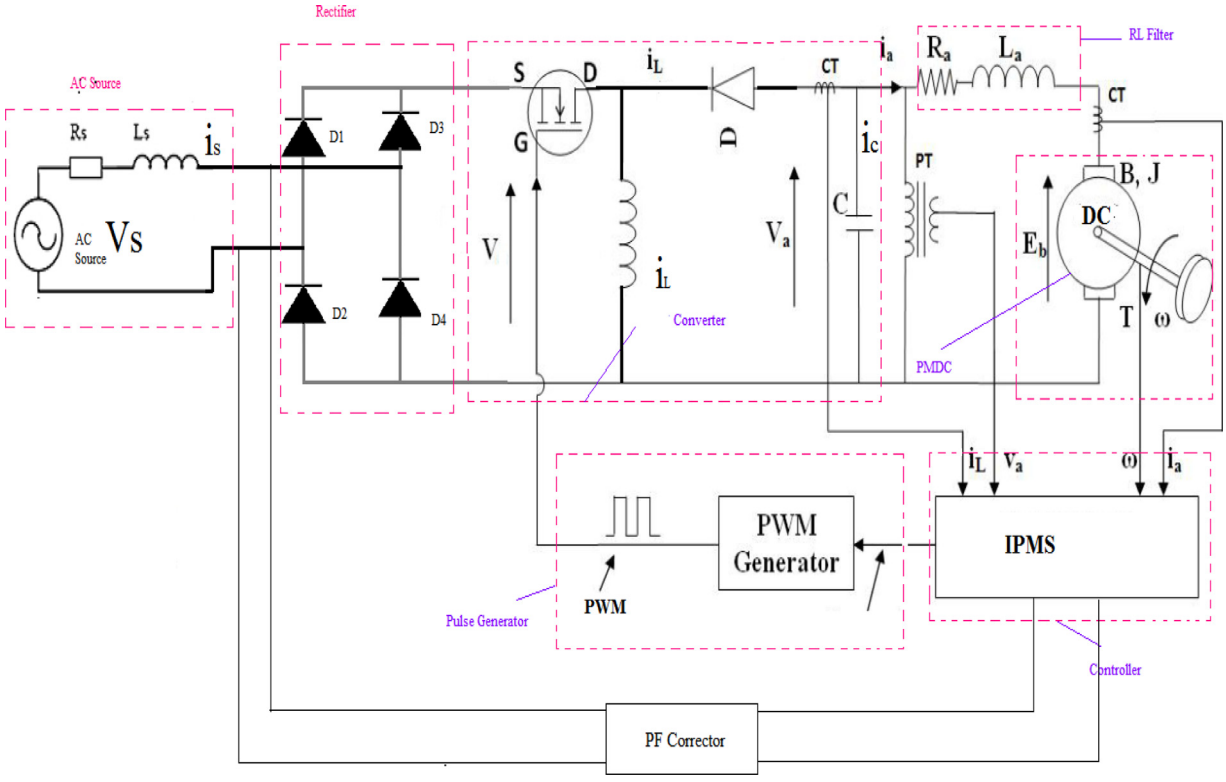


Fig. 3. Block diagram IPMS DC motor control.

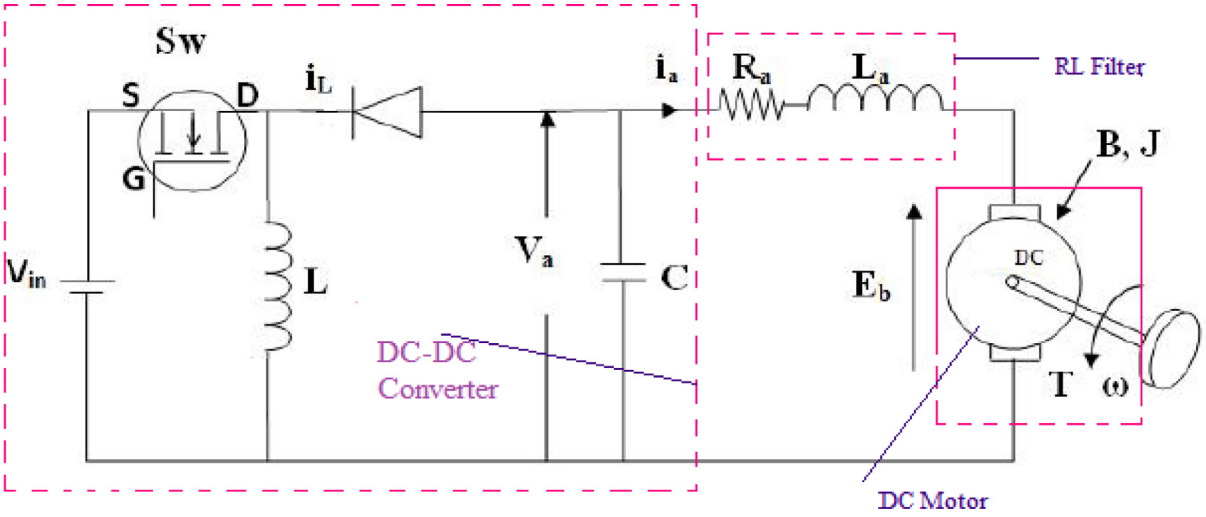


Fig. 4. Circuit diagram for PMDC motor fed With DC–DC Converter.

v_a = Voltage of Armature (V)
ω = Motor Speed (rad/s)
i_a = Current value of Armature (A)
i_L = Current Value in Inductor (A)

The mathematical model of DC motor along with converter is obtained using Eqs. (1–8)

3.4. optimization and analysis of single phase AC to DC converter using intrinsic power management strategy

The power or Energy management is the major need in the AC to DC converter system. During the power conversion, source side imbalance or load variation will affect the system. So an adaptively optimized technique is implemented to stabilize the overall system efficiently with low losses in the circuit. This work proposes to be a natural and systematic framework for the design of this type of power management controls. More importantly, the proposed system produces new results based on classical theory, with the optimum control that allows real time-effect solving the problem of control. More specifically, the Intrinsic Power Management Strategy is first used to find solutions that are slightly advantageous for solving power management issues.

The proposed controllers have expanded voltage gain, and system stability is more. So IPMS controller is utilized to control the DC-interface voltage for Speed control. This method is employed to measure the rotor position and depend upon the status detected, the switches for Speed control are activated. Thus, the sev-

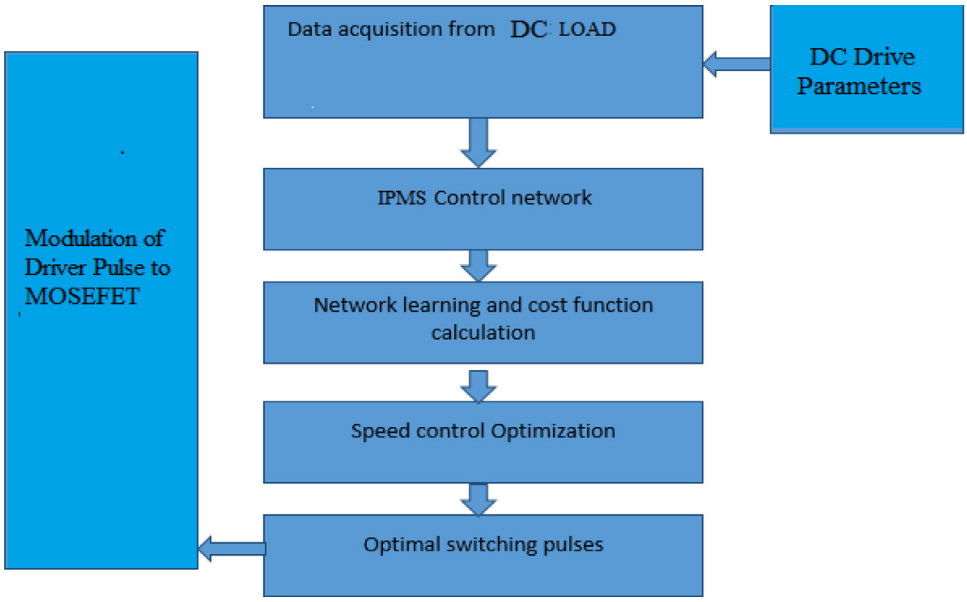


Fig. 5. Proposed IPMS Controller model flow.

eral switching angles that arrived at the converter stages will bring about a greater extent of low order harmonics.

The proposed methodology concentrates on the determination of switching schemes to remove the little order harmonics using IPMS. At first, the IPMS instrument is used to obtain different flux linkage data sets for the unique arrangement of the peak voltage, which creates the voltages Vα and Vβ. These voltages are the contributions to the IPMS to generate the switching pulses for the Speed control.

The obtained datasets are used for developing the proposed IPMS control model in Fig. 5. The proposed IPMS structure is then achieved to make the relating switching angles to control speed by PWM generation based on the DC motor peak voltages. The training dataset required for the IPMS control is obtained by knowing the harmonics distortion considering the different DC motor Parameters. The reduced Harmonic distortion conditions are obtained during the non-linear control of DC drive.

3.4.1. Optimal selective harmonic elimination using IPMS

IPMS controllers have been used to avoid complex problems in typical pulse width modulation technologies. The proposed regulatory framework implements the flexible back propagation protocol with the status of an equal nonlinear system. Subsequently, nonzero system harmonics are removed by reduction using change angles. In this case, the neural system resilient is set to change the angle of a switch in an approach to eliminate the second order harmonics without learning the angle of switching to the desired switching algorithm. Resilient Back Propagation (RBP) is the effect of the transition from the learning process to the IPMS, ie the effect of optimal change of switching pulses.

The IPMS method based on optimal selective harmonic cancellation is shown in Fig. 6. The back propagation error is calculated, based on this error rate IPMS automatically controls the switching frequency of MOSFET. The desired 48V dc output is achieved based on IPMS switching activity. Using the IPMS, the first synchronization of the angles are compared. This comparison eliminates the repetitive training between the solutions of the nonlinear equations that have been expected.

3.4.2. IPMS training procedure

The proposed program must use the network contains an input layer, a hidden layer, and an output layer. Changes are provided as pulse learning sources, and the outputs of their real voltages are taken. IPMS is used to control the switched pulses in the neurotransmission slot. An IPMS approach is an efficient auto tuned application without the need for specific functional control.

The IPMS-based neurological system has developed the most controlled features. The imagination resilience is composed of three input units for reproduction design, n, hidden and output layers are shown in Fig. 7.

The below mentioned steps are discussed about the training features.

Step1: First to generate the random weights of w_{min}, w_{max} and assign it's to the hidden and output layer. Allocate a single weight with input layer neurons.

Step 2: To calculate the Resilient Back Propagation (RBP) error, that it will take the database D and contribute to the system takes after

$$e = V_r - V_{out}, \tag{9}$$

where

V_r = Objective Function
V_{out} = Network outputs

Step 3: For each and every Neuron output has been calculated as

$$V_h = \sum_{n=1}^{N_{Hid}} w_{nh} y_n \ldots\ldots \tag{10}$$

$$\text{where}, y_n = \sum_{j=1}^{N_I} \frac{w_{jn}}{1+e^{-ikl}}$$

N_{Hid} = Number of neurons in hidden
w_{nh}= weight of the *n-h* link of the network
V_h = hth output neuron
y_n = n^{th} hidden neuron.

Step 4: By obtaining the RBP error thus, controlling the weight adjustment

$$\Delta w = \gamma . Vout.e \ldots\ldots \tag{11}$$

Where, the knowledge function γ is commonly changed from 0.11 to 0.415.

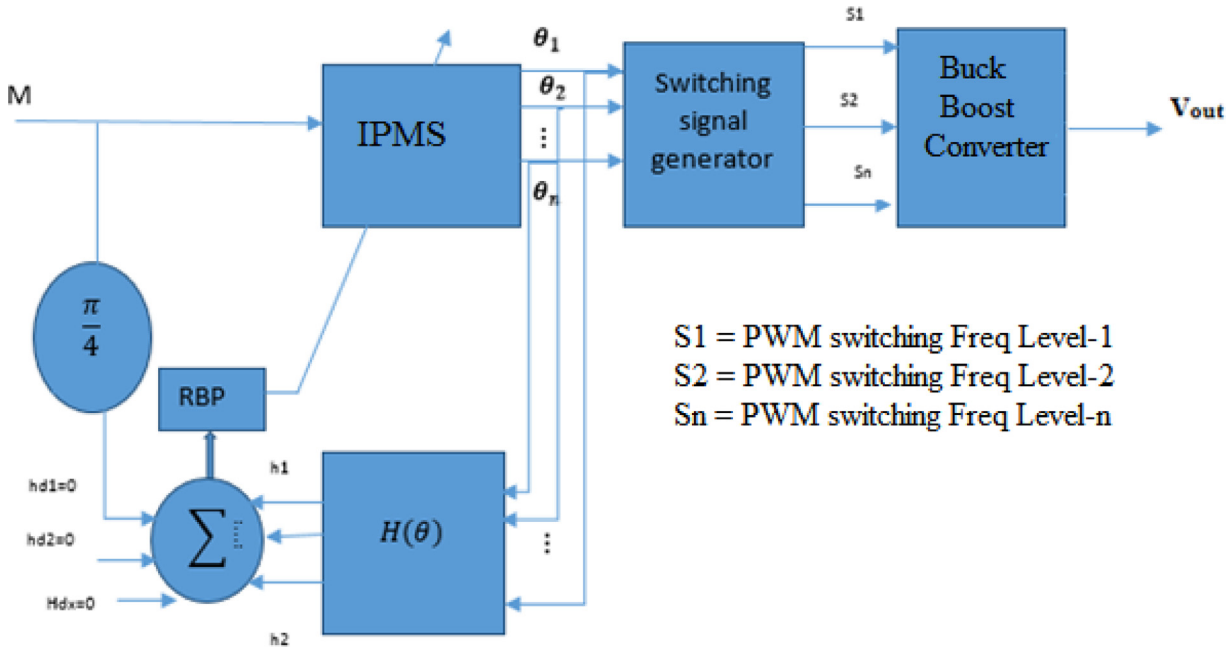


Fig. 6. IPMS model for Optimal Selective Harmonic Elimination.

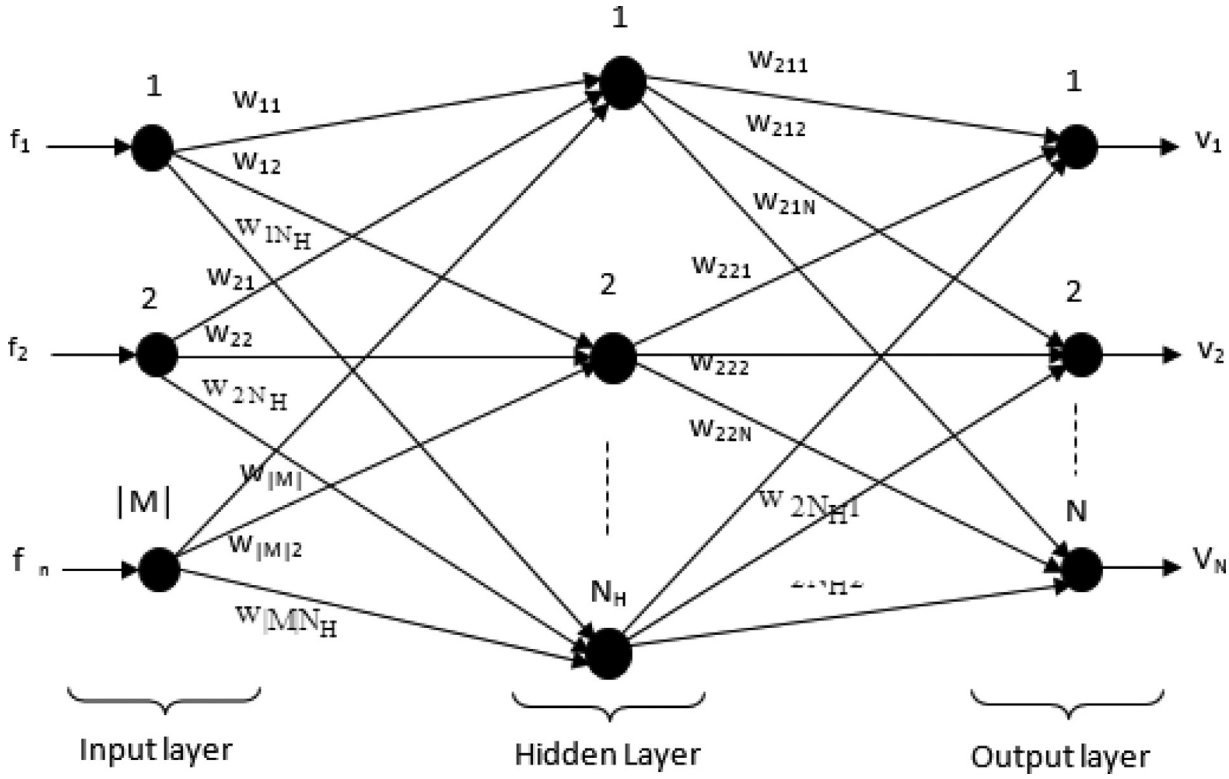


Fig. 7. Training Structure of IPMS.

Step 5: The basic weight regulation is as follows:

$$w = w + \Delta w \ldots. \tag{12}$$

Step 6: The RBP error is <0.1, which is most likely to be satisfied until at least the value is reduced and goes to step 2. Once the instruction process is done, the network receives well-prepared to evaluate any unknown data.

Training process restricted final pulses have been entered several times to reach an average network. During the validation process, speed control areas are also detected using controlled lentils for switches to the topology. The IPMS algorithm has been clarified that the following steps are being made to go through. The Testing Prosecute of IPMS is discussed below.

3.5.1. Hysteresis current controller

To achieve the perfect result like a reduction of harmonics, Reactive power balance, and the Power factor, the DC-link voltage is sensed and compared with the reference DC-link voltage shown

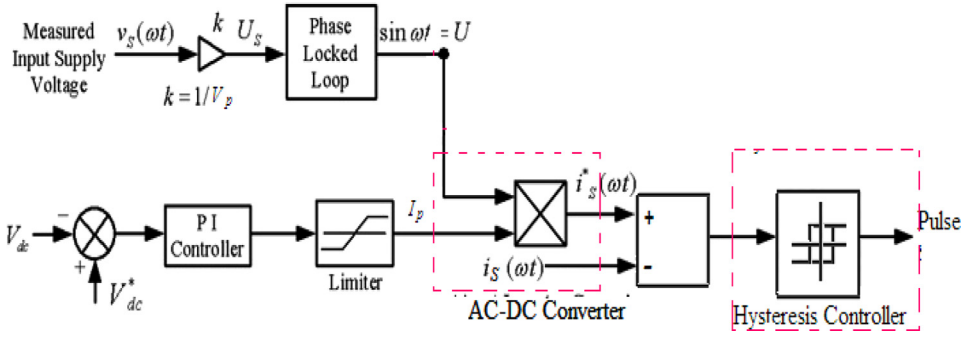


Fig. 8. Hysteresis Current Controller.

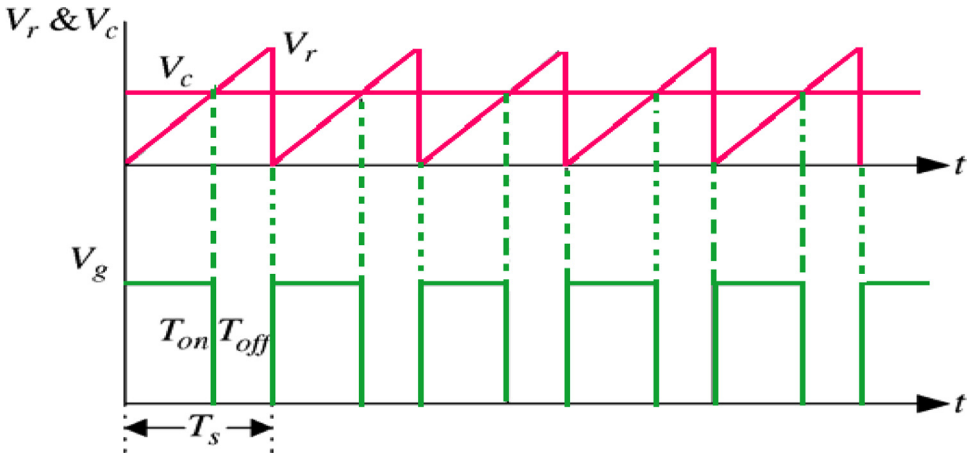


Fig. 9. Generation of PWM.

in Fig. 8. The error is given to the hysteresis controller to carry out the Pulse Width Modulation (PWM) operation and a produced pulse is given to MOSFET. This is the switching scheme of series active filter. The generated reference source current signal is then compared with actual source current to perform PWM operation and produced pulses are given as it is the same for a series active filter.

The complete block diagram of the Hysteresis controller based on the single-phase system is shown in Fig. 8. The error is then processed by a PI controller. The output of the PI controller can be represented as Ip, which should be drawn from the supply in order to maintain DC-link voltage at a constant level and to supply losses associated with AC source. Thus, by multiplying Ip, with unit vector template of Eq. (13), gives the reference source current signal that the source should supply.

$$i_s^* = I_P Ua = I_P \sin(\omega t) \tag{13}$$

where,

i_s^* = Reference source current
I_P = Peak amplitude of fundamental input current

The significant advantage of this approach is that it does not require complex transformations and it is easy to implement for real time applications.

3.6. Modes of operation

The proposed IPMS based buck-boost converter comprises a diode bridge with only one switching device as shown in Fig. 9, a reactor in the dc link, a series connection of a diode and a capacitor parallel to the dc reactor. In this configuration, the inductor acts as an energy storage/transfer element and step up and step-down characteristics of the output voltage can be easily obtained by an appropriate switching scheme for the controlled power semiconductor switch.

3.6.1. PWM switching strategy and DC voltage control

The generation of the MOSFET driving signal is accomplished by comparing a dc reference signal, having a variable amplitude v_c, with a saw tooth carrier wave, having a fixed amplitude v_r and frequency f_s, known as the switching frequency. The ratio between v_c and v_r is called the duty cycle, $D = v_c/v_r$, which is defined as the ratio of the on time t_{on} to the total switching period $t_s = t_{on} + t_{off}$. The average output voltage is varied by changing through the variable v_c to control the duty cycle D (Fig. 9).

3.6.2. Modes of operation

The operating modes and the equivalent circuits during these modes of the buck-boost converter fed dc motor depends on the switching conditions of both the switching device and the diode D. Depending on the state of the switching device and the diode, each chopping cycle comprises two or three different sub modes of conduction. Fig. 10 shows these three possible modes for one switching cycle for the positive supply voltage. These modes are as follows.

Charging mode (mode 1)

During the charging mode, the switching device is turned on, therefore, the diode D is reverse biased so the absolute value of the supply voltage appears across the inductor. The inductor current i_L will rise and flows through the input side, as shown in Fig. 10a, causing energy to be stored in the inductor. In this mode, the loop of the motor terminals and the output capacitor are isolated from the supply. Therefore, the capacitor charge, accumulated from the

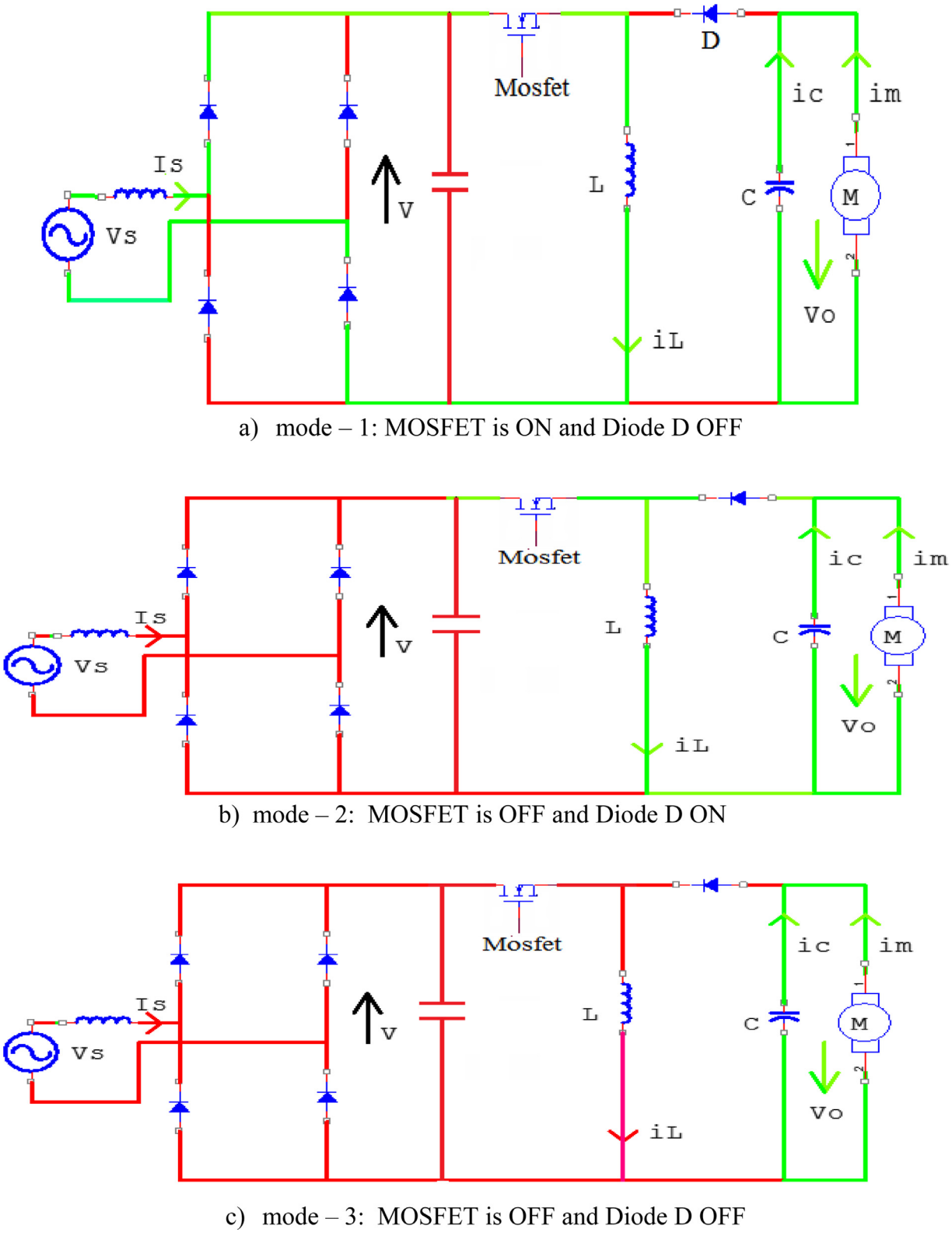
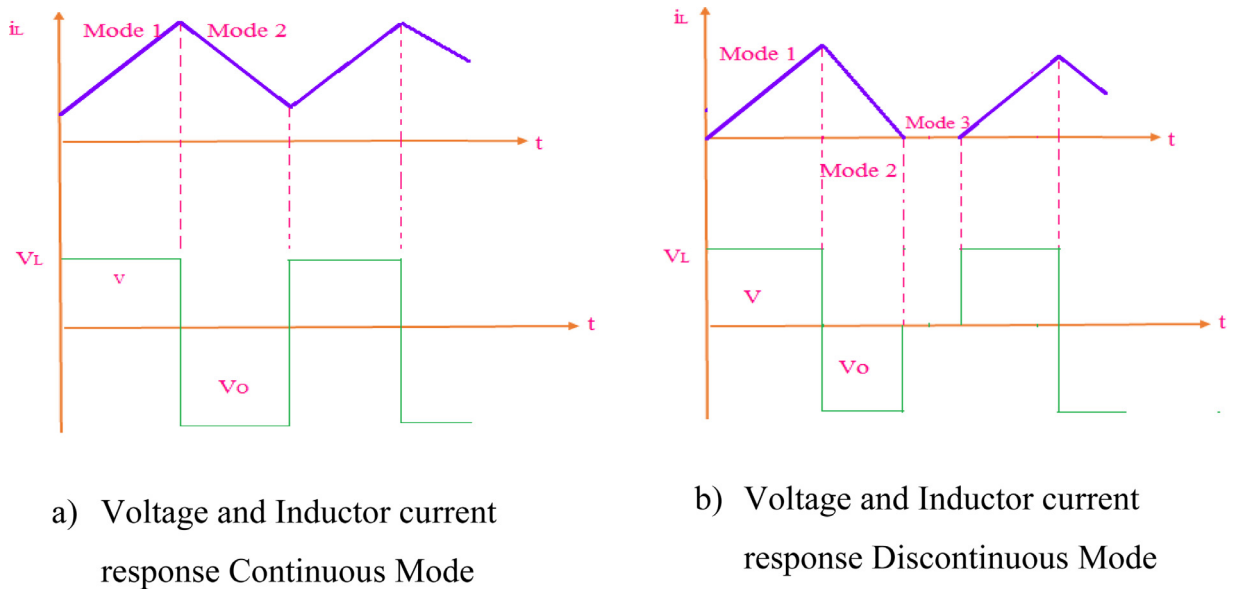


Fig. 10. Modes of Operation.

previous period, will be discharged through the armature winding. The system will stay in this mode for the turn on a period of the switching cycle of the switching device. The dark lines in Fig. 10a shows the possible current paths of the inductor and motor currents during the charging mode.

Discharging mode (mode 2)

The discharging mode is complementary to the charging mode. The system is transferred to this mode when the switching device is turned off and the diode D will be forward biased. The inductor current *iL* falls through the output side and flows through the



a) Voltage and Inductor current response Continuous Mode

b) Voltage and Inductor current response Discontinuous Mode

Fig. 11. Output Voltage and Inductor current response during one duty cycle.

output capacitor C and the dc motor as shown in Fig. 10b. The inductor voltage reverses its polarity and it forward biases the diode D. The energy stored in the inductor would be transferred to the motor and the inductor current will fall until the switching device is switched on again in the next cycle or until inductor current decreases to zero (mode 3). The capacitor is charged according to a decrease in the inductor current.

Mode 3

In mode 3, the switching device is still off but the circuit conditions may cause the inductor current *iL* to fall to zero such that the diode D becomes reverse biased. This mode lasts until the switching device is turned on again. The system will stay in the discharging mode for a period determined by the system parameters. Of course, this period does not exceed the off period of the switching device. If the inductor current *iL* is assumed flows continuously, mode 3 disappears. Fig. 10c shows the equivalent circuit during this operation mode.

3.6.3. Inductor current and voltage response during one switching cycle

Fig. 11 shows the steady state inductor current and voltage waveforms during one complete switching cycle for a continuous and discontinuous inductor current in both continuous (Fig. 11a) and discontinuous mode (Fig. 11b). Due to the use of high switching frequency, the input voltage can be assumed constant during the switching period.

The equivalent circuit model also supports us in computing the converter efficiency (Fig. 3). The converter input power is

$$P_{in} = (V_s)(I_s) \tag{14}$$

The load current is equal to the current of PMDC motor, or hence, the model predicts that the converter output power is

$$P_{out} = (V_a)(I_L) \tag{15}$$

Therefore, the converter efficiency is

$$\eta = \frac{P_{out}}{P_{in}} = \frac{(V_0)(I_0)}{(V_a)(I_L)} \tag{16}$$

where

V_S = Source Voltage
I_S = Source Current
V_a = Load Voltage
I_L = Load Current

The efficiency of proposed IPMS with hysteresis current controller based PMDC motor can be evaluated as

$$\beta = \frac{P_{out}}{P_{in}} \tag{17}$$

$$P_{in} = i_a V_a \tag{18}$$

$$P_{out} = i_o V_o \tag{19}$$

In this work, the utilization of the IPMS takes the control of the DC load. The performance is evaluated in various emphasis levels of the different load conditions.

The working flow chart of proposed system is shown in Fig. 12 and the following parameters are used to evaluate the performance of proposed system.

Peak Overshoot: This is largest value of the step response. One can also calculate the overshoot as the maximum amount that the response overshoots its final value, divided by the final value.

$$M_p = -C(\infty) \tag{20}$$

Where

M_p = Maximum Peak Overshot Voltage
$C(t_p)$ = Peak Value of the response
$C(\infty)$ = Final Value of the response

Recovery Time: The recovery time it takes for the error between the response output (t) and the steady-state response. Recovery time includes a propagation delay, plus the time required for the output to slew to the vicinity of the final value, recover from the overload condition associated with slew, and finally settle to within the specified error

Steady State Error (rpm): The difference between the input step value (dashed line) and the final value.

$$S_s = R_s - RV_s \tag{21}$$

where

S_s = Steady state error

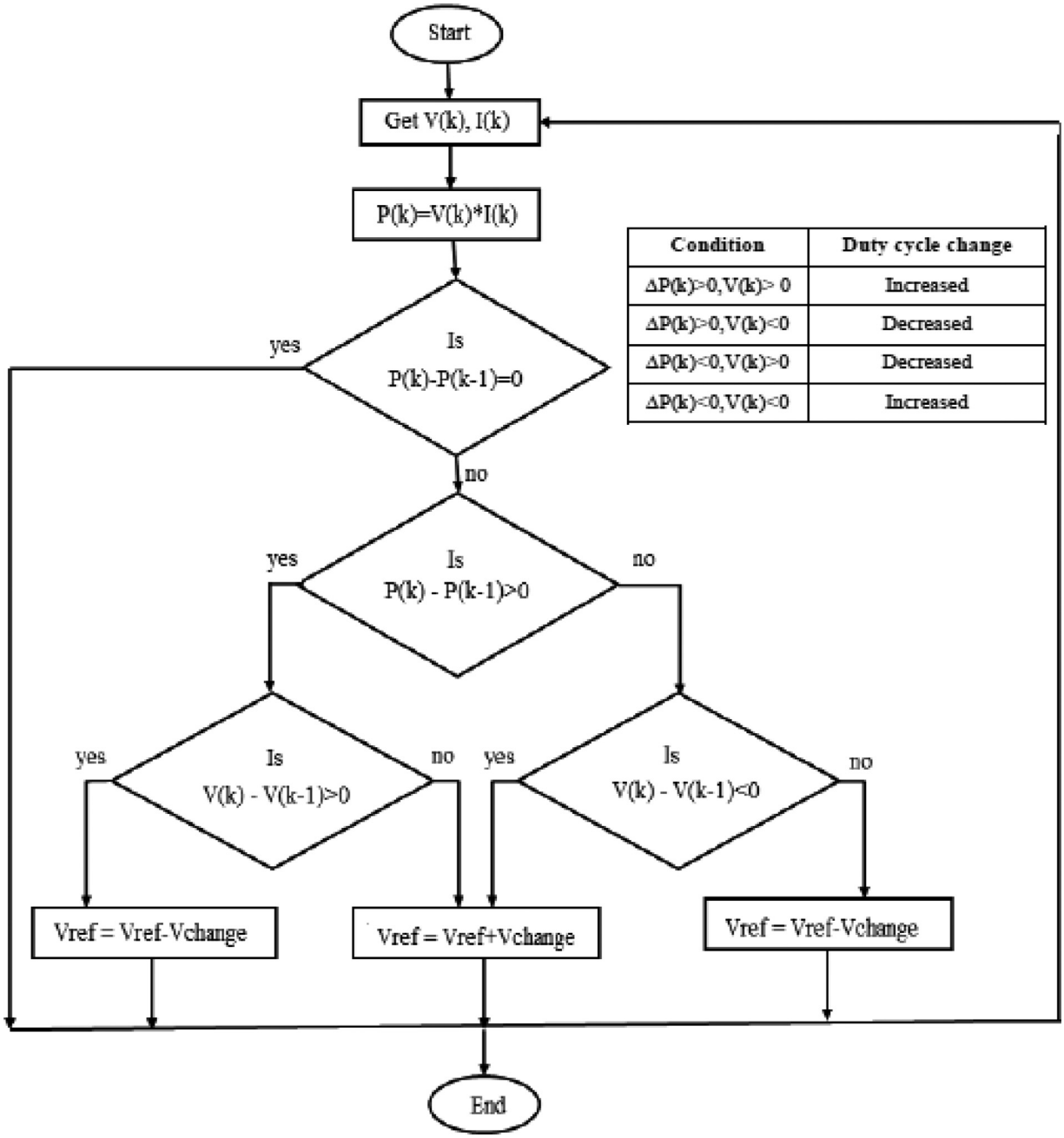


Fig. 12. Flow Chart of Proposed system.

V_s = Reference State
RV_s = Running Speed

Settling time: Another measure of performance is the settling time of the response, defined as the time required for the response to get to within a certain percentage of its final value and stay there.

Table 1
Design parameters ranges for proposed AC/DC converter.

Parameters	Values
V_{in} (RMS)	230 ± 10% V
V_{out}	48 V
Maximum Load	1000 W
MOSFET Switching Frequency	5 kHz
Motor	PMDC, 1500RPM, 1000 W
Simulation tool	Matlab

4. Results and discussion

The Proposed IPMS's Control strategies are simulated in the MATLAB software, then the simulation circuit and the obtained results are represented in below tables and figures. In this section, the IPMS is used for improving the performance results when compared with the existing methods.

Table 1 describes the Design parameters and then ranges of the proposed converter model. In this system, lesser components are used to make energy efficient converter.

Fig. 13 represents the proposed simulation model for a single phase AC/DC converter with R-Load using advanced IPMS control

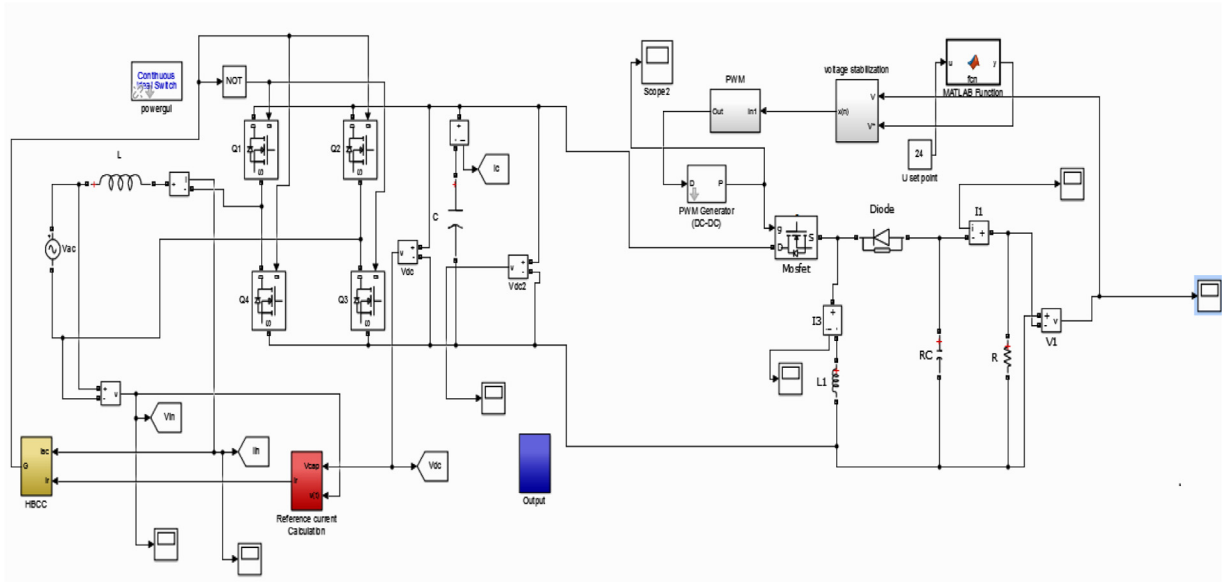


Fig. 13. Simulation Model of the Proposed AC to DC converter with R-Load.

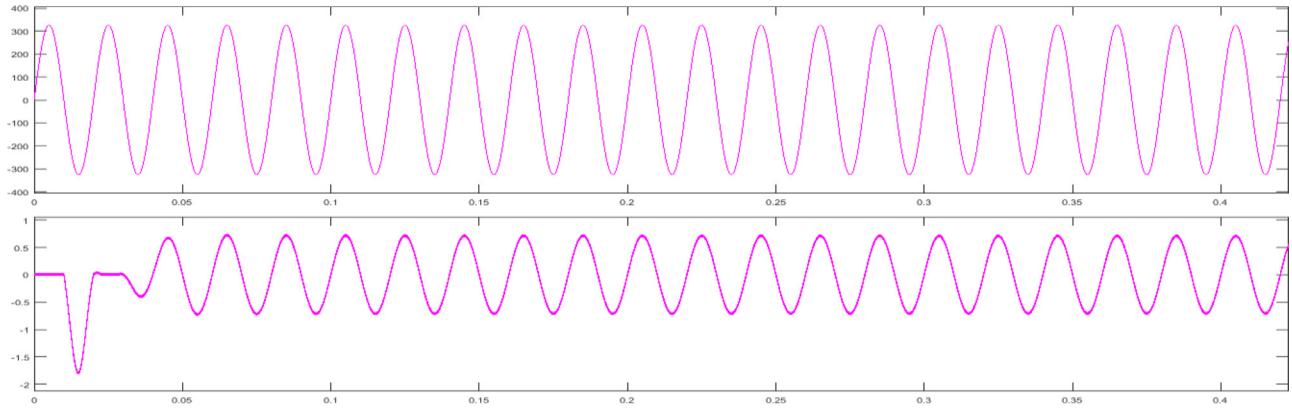


Fig. 14. Source Voltage and Current Waveforms with R-Load.

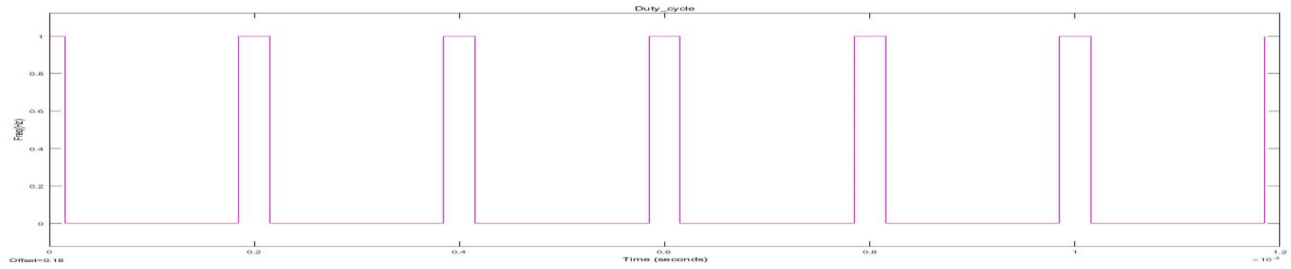


Fig. 15. Duty Cycle generation by IPMS controller.

strategy which effectively improves the performance parameters as seen in waveforms and graphs. In this work the input 230 V AC is a converter to 48 V DC.

Fig. 14 illustrates source current and voltage waveform both are in phase with each other under the differential time period. The waveforms confirm the power factor is unity with respect to any load and the duty cycle of the proposed IPMS is shown in Fig. 14.

The IPMS controller based duty cycle generation is shown in Fig. 15.This duty cycle is directly fed to MOSFET's gate pin. Based on the load condition the duty cycle is automatically changed and maintains the constant 48 V DC.

Fig. 16 shows the DC–DC converter output voltage from the conversion of the source voltage. The *y*-axis shows the converted DC voltage =48 V with respect to time.

The THD analysis of the proposed AC–DC converter with the Resistive load is shown in Fig. 17 using the IPMS method. By using the IPMS method to achieve low THD equivalent to 0.26% and a major component at 50 Hz. In the typical waveforms of Figs. 14, 16 and 17 of the proposed single phase AC–DC converter gives buck/boost voltage gain. In this work the input voltage 230 V AC and the output voltage is 48 V DC. The proposed circuit gives near unity power factor and the spectrum of the input currents indicates that the harmonic components are lower than the fundamen-

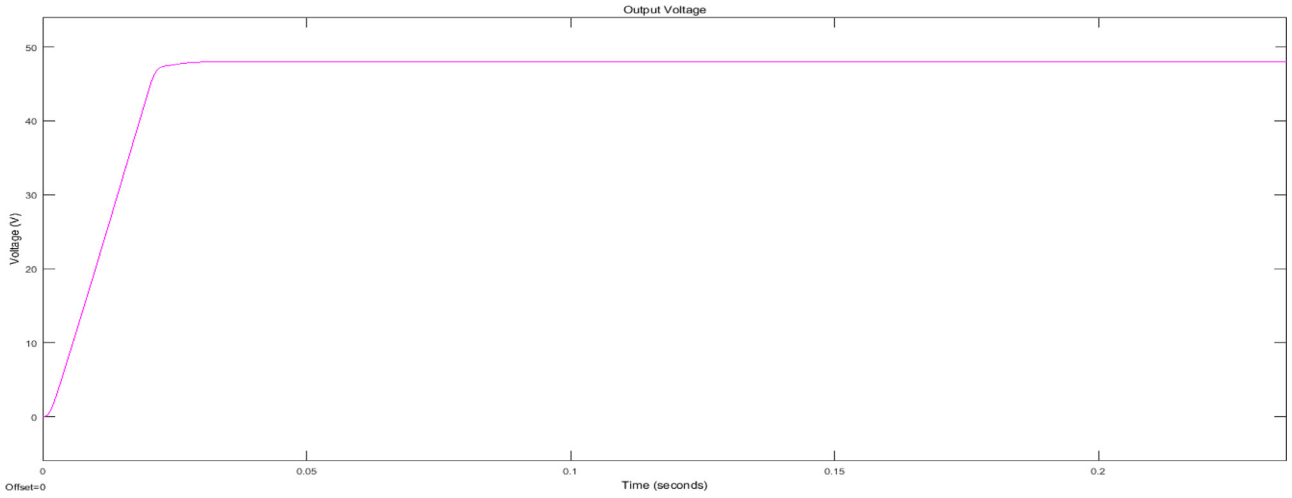


Fig. 16. DC–DC converter output voltage with R-Load.

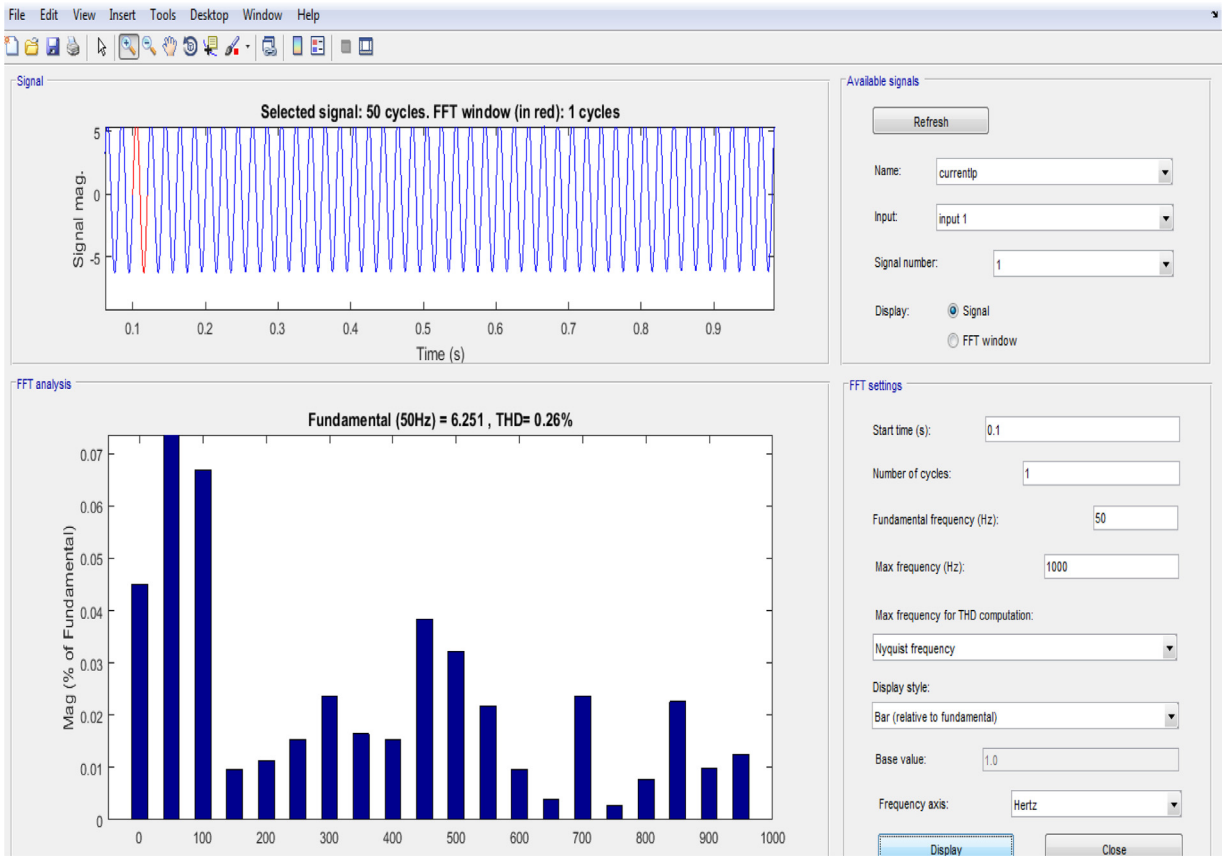


Fig. 17. THD analysis for proposed System.

tal frequency component producing very low input current THD (0.26%) when operating in the buck-boost region of operation.

Fig. 18 represents the proposed simulation model for a single phase AC/DC converter using advanced IPMS control strategy with PMDC motor load which effectively improves the performance of transient response and stability of the system.

Fig. 19 illustrates source current and voltage with PMDC motor load waveform both are in phase with each other under the differential time period. The waveforms confirm the power factor is unity with respect to any load and the duty cycle of the proposed IPMS is shown in Fig. 19.

Fig. 20 shows the DC–DC converter output voltage from the conversion of the source voltage with a PMDC motor. The *y*-axis shows the converted DC voltage =48 V with respect to time.

The speed response of the proposed Intrinsic Power Management Strategy (IPMS) based DC–DC converter with PMDC is depicted in Fig. 21.

Fig. 22 discusses the electromagnetic torque and rotor angle response of the proposed IPMS based PMDC control system. The electromagnetic torque depends mainly on the load angle and the magnitude of the stator flux.

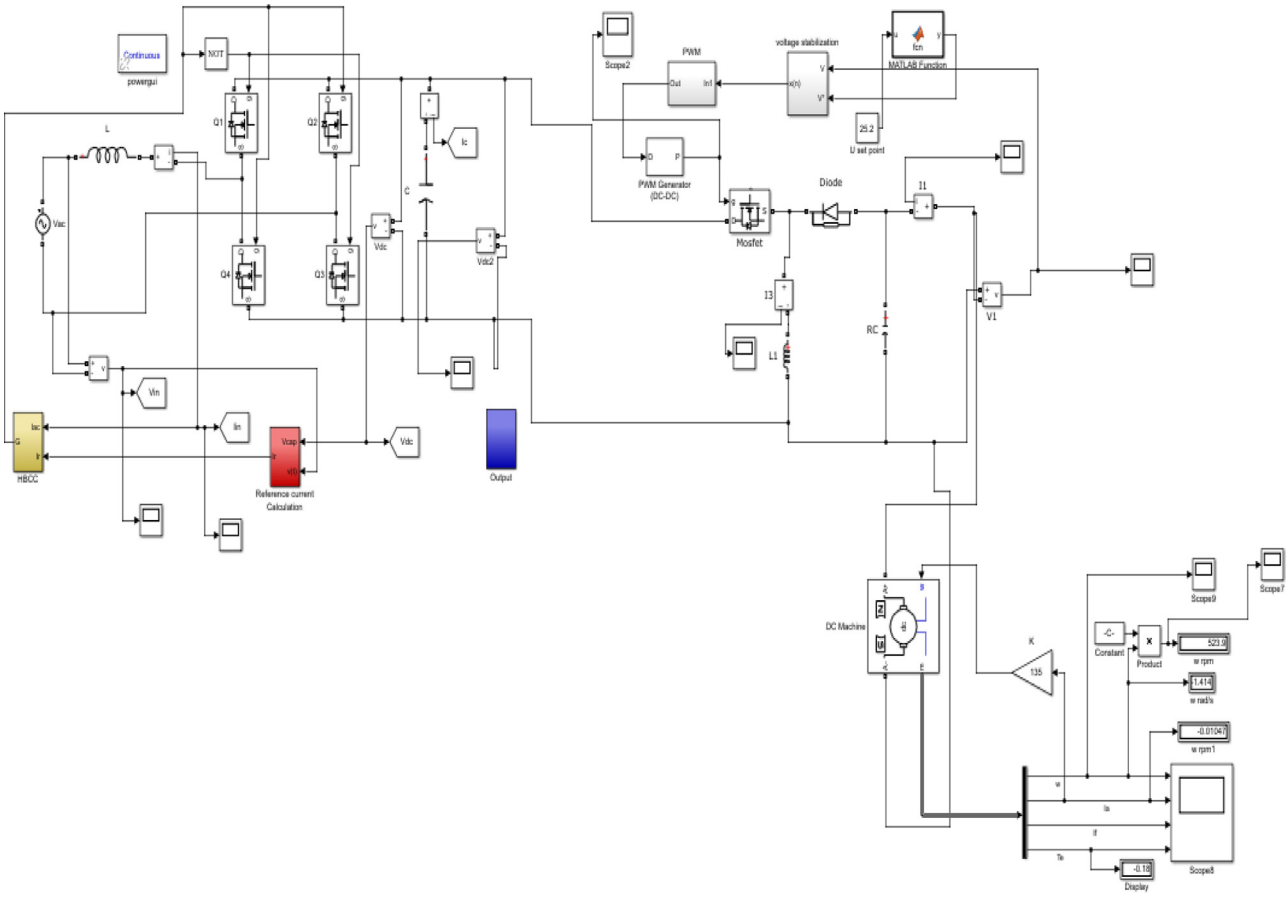


Fig. 18. Simulation Model of the Proposed AC to DC converter with PMDC Motor.

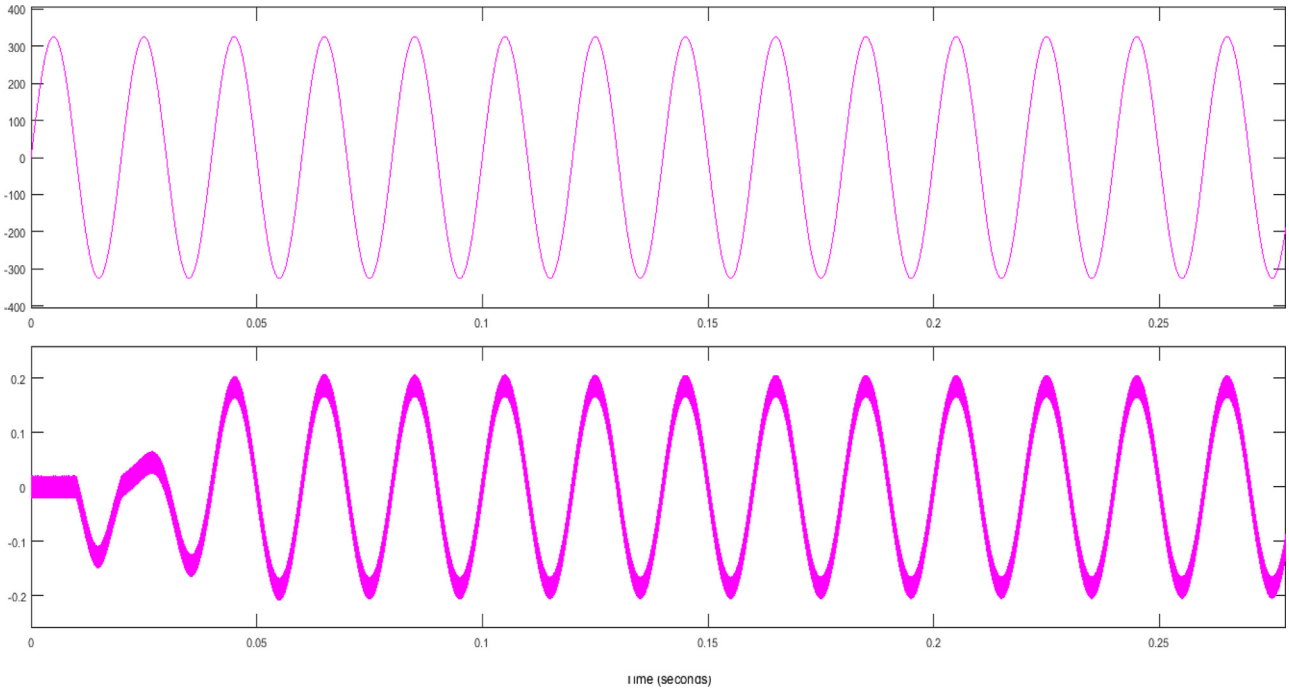


Fig. 19. Source voltage and source current with PMDC Motor Load.

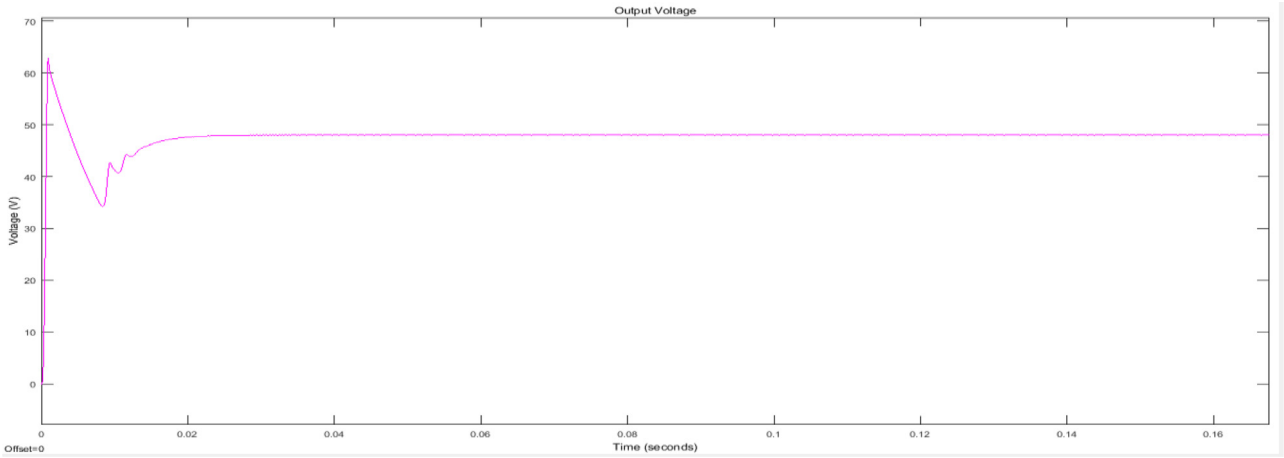


Fig. 20. DC-DC converter output voltage with PMDC motor.

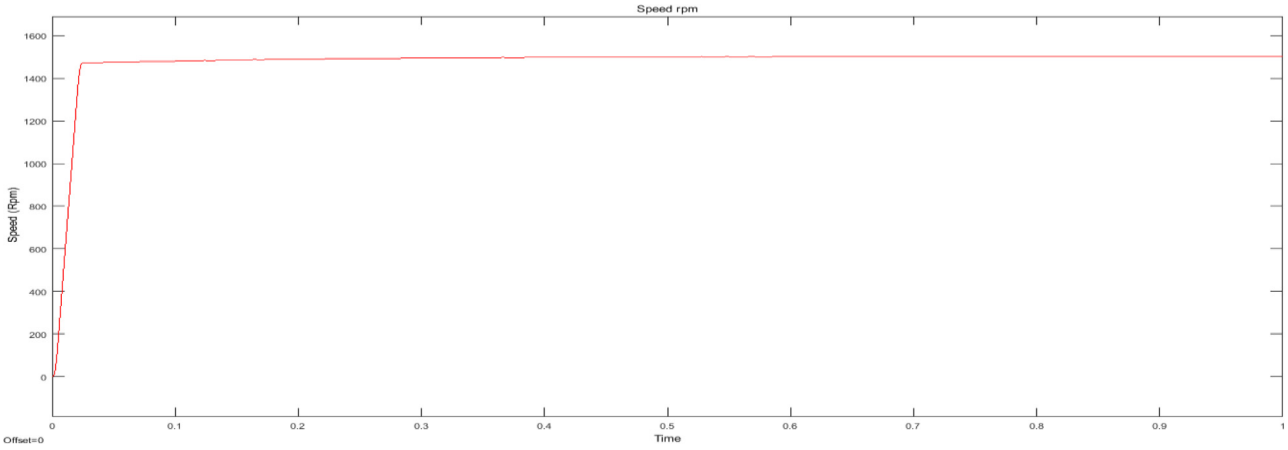


Fig. 21. Speed Response of PMDC Motor.

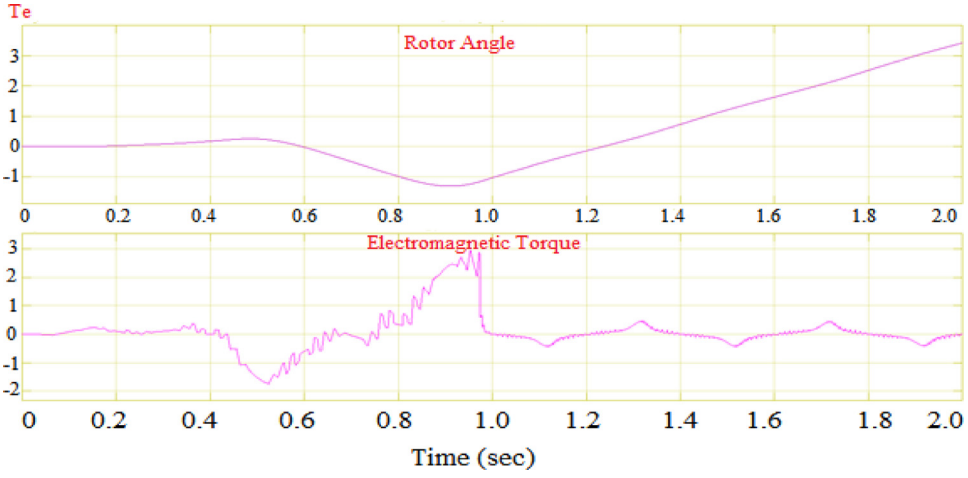


Fig. 22. Rotor angle and Electromagnetic torque of direct axis.

The THD analysis of the proposed AC–DC converter with a PMDC motor load is shown in Fig. 23 using the IPMS method. By using the IPMS method to achieve low THD equivalent to 2.58% and a major component at 50 Hz. The typical waveforms of the proposed AC–DC converter with PMDC motor drive are shown in Figs. 19–21. In this work the input voltage 230 V AC and the output voltage is 48 V DC. The proposed circuit gives near unity power factor(as referred in Fig. 19 both voltage and current are there in the same phase) and the spectrum of the input currents indicate that the harmonic components are lower than the fundamental frequency component producing very low input current THD (0.26%) when operating at in buck-boost region of operation of 48 V.

Table 2 demonstrates the comparison of power factor variation esteems got from the proposed Versatile Power Balanced Control (VPBC) and Intrinsic Power Management Strategy (IPMS) based

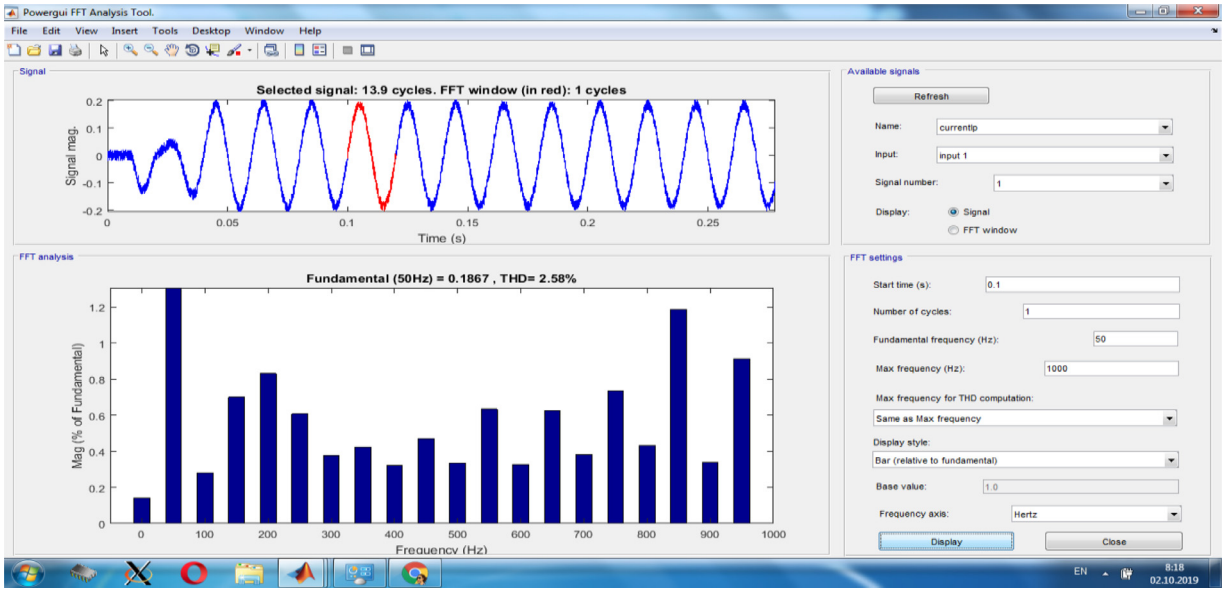


Fig. 23. THD analysis for proposed System.

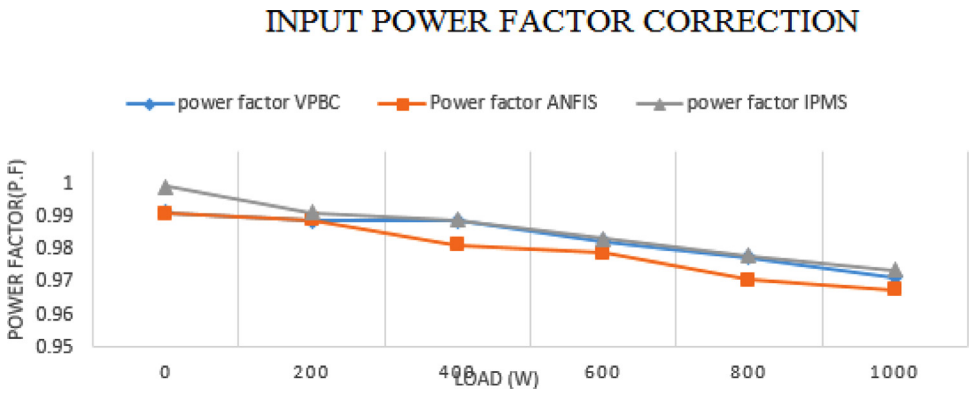


Fig. 24. Power Factor analysis for the existing and proposed techniques.

Table 2
Comparison of Power factor correction with an existing controller for single stage AC/DC converter system.

S. No	Load(W)	Power factor (P.F) when different Controller Used		
		ANFIS	VPBC	IPMS
1	0	0.9908	0.9989	0.9990
2	200	0.9889	0.9910	0.9912
3	400	0.9814	0.9886	0.9889
4	600	0.9789	0.9823	0.9833
5	800	0.9705	0.9775	0.9781
6	1000	0.9675	0.9715	0.9736

AC/DC single stage converter with a conventional technique like Adaptive Neuro-fuzzy (ANFIS).

Fig. 24 describes the comparative study for power factor correction with different Control strategies, for example proposed Intrinsic Power Management Strategy (IPMS), Versatile Power Balanced Control (VPBC) technique, Adaptive Neuro-fuzzy (ANFIS) technique. As compared with existing controllers the proposed IPMS method shows improvement in converter parameters.

Table 3 describes the Efficiency analysis of the proposed model for different load power in watts. The proposed Intrinsic Power Management Strategy (IPMS) produced an effective result of 98.73% of efficiency for Full load conditions.

Table 3
Efficiency Comparison for AC/DC converter with different controllers

Load(watts)	ANFIS controller efficiency (%)	VPBC efficiency (%)	IPMS (%)
0	0	0	0
200	63.45	67.6	70.81
400	74.25	77.2	88.04
600	83.47	85.00	93.76
800	84.98	85.71	96.99
1000	89.56	91.11	98.53

Table 4
Control system parameters for PMDC load condition.

Methods	Settling time (sec)	Peak overshoot (%)	Recovery time (sec)	Steady state error (rpm)
PID	0.75	4.2	0.365	10
PID-ANN	0.5	2.8	0.14	8
IPMS	0.05	1.6	0.02	6

Fig. 25 Shows the Efficiency analysis of the proposed converter model. The waveform clearly describes the Efficiency improvement of the proposed model for the load power (0–1000) watts.

The performance analysis different parameters such as steady state error, peak time, and peak overshoot time and recovery time are discussed in Table 4. As compared with conventional methods the proposed IPMS method gives the best result.

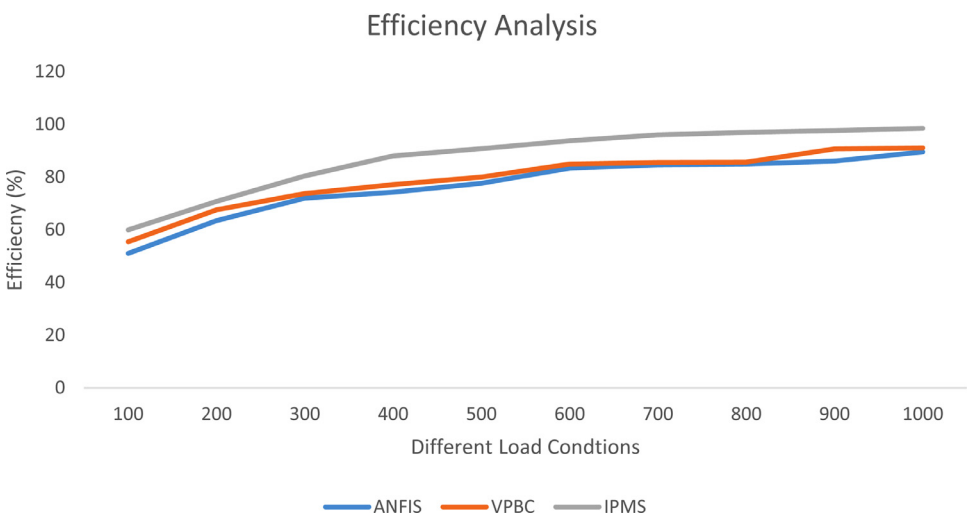


Fig. 25. Efficiency analysis of the proposed system.

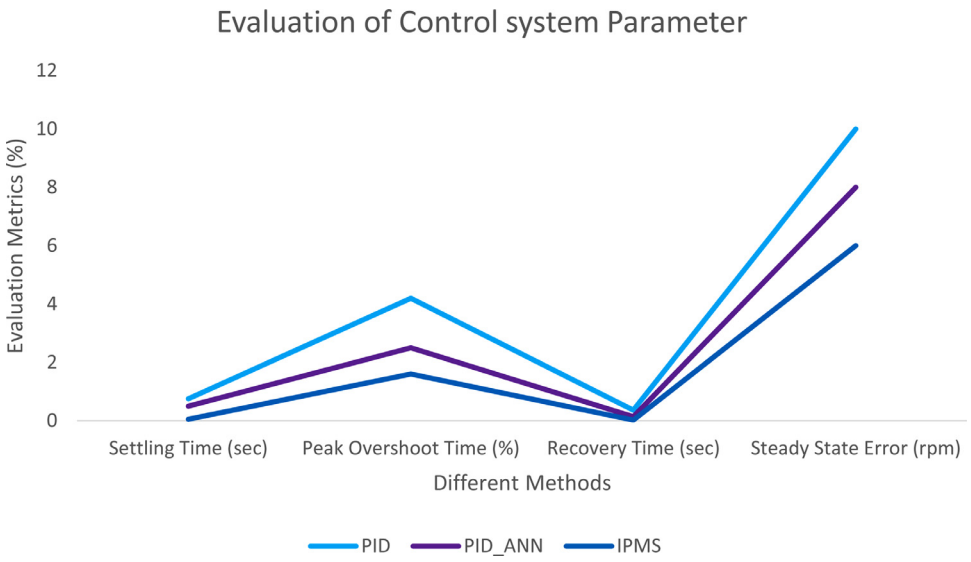


Fig. 26. Performance Analysis of Control system Parameter.

Fig. 26 discusses the Performance Analysis of Control system Parameter using different algorithms, such as PID [29], PID_ANN [29] and IPMS. As compared with Existing PID [29] and PID-ANN [29] the proposed IPMS gives the perfect results against all parameters, for example the Settling time of IPMS is 0.05Sec, peak overshoot of IPMS is 1.6% sec and Steady state error is 6rpm.

5. Conclusion

This work presents the design and evaluation of a single-phase AC/DC converter for Power factor correction with a buck boost converter for the supply of permanent magnet DC motors. MATLAB software was used to simulate the proposed converter. Simulation results for converter performance were analyzed for PFC, efficiency and THD. Finally to conclude the proposed Intrinsic Power Management Strategy (IPMS) is the better solution to control the power balance in the AC to DC converter system with its cost-effectiveness. It provides an efficiency of 98.73% and the THD is 0.26% against resistive load and 2.56% against PMDC motor load. As compared with Existing PID and Fuzzy the proposed IPMS gives improved results against all Control system Parameters with PMDC motor load**,** for example settling time of IPMS is 0.05Sec, peak overshoot of IPMS is 1.6% sec and Steady state error is 6 rpm. In future, design with deep learning method to improve the response of AC–DC converter will be the utmost focus.

Declaration of Competing Interest

As compared with Existing PID and Fuzzy the proposed IPMS gives improved results against all Control system Parameters with PMDC motor load**,** for example settling time of IPMS is 0.05Sec, peak overshoot of IPMS is 1.6% sec and Steady state error is 6 rpm. In future, design with deep learning method to improve the response of AC–DC converter will be the utmost focus.

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