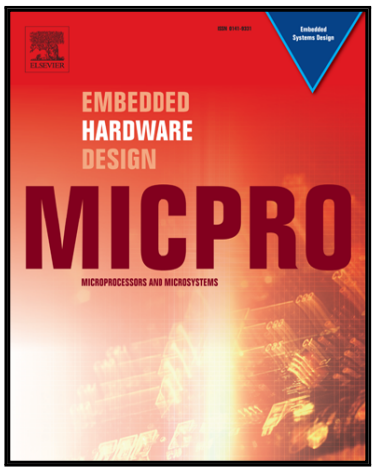
Journal Pre-proof



A modified Asymmetric Cascaded Multilevel DC-AC converter with Switched Diodes with FPGA processor implementations

D. Arun Prasad , K. Mahadevan , M. Arul Prasanna

PII: S0141-9331(19)30578-2
DOI: https://doi.org/10.1016/j.micpro.2020.103019
Reference: MICPRO 103019

To appear in: *Microprocessors and Microsystems*

Received date: 1 November 2019
Revised date: 10 January 2020
Accepted date: 6 February 2020

Please cite this article as: D. Arun Prasad , K. Mahadevan , M. Arul Prasanna , A modified Asymmetric Cascaded Multilevel DC-AC converter with Switched Diodes with FPGA processor implementations, *Microprocessors and Microsystems* (2020), doi: https://doi.org/10.1016/j.micpro.2020.103019

This is a PDF file of an article that has undergone enhancements after acceptance, such as the addition of a cover page and metadata, and formatting for readability, but it is not yet the definitive version of record. This version will undergo additional copyediting, typesetting and review before it is published in its final form, but we are providing this version to give early visibility of the article. Please note that, during the production process, errors may be discovered which could affect the content, and all legal disclaimers that apply to the journal pertain.

© 2020 Published by Elsevier B.V.

Journal Pre-proof

A modified Asymmetric Cascaded Multilevel DC-AC converter with Switched Diodes with FPGA processor implementations

Arun Prasad D [1*], Mahadevan K [2], Arul Prasanna M [3]

[1, 2, 3]Department of Electrical and Electronics,PSNA College of Engineering and Technology, Dindigul, India.
arunprasadphd2019@gmail.com

Abstract: A modified cascaded multilevel DC-AC converter using switched diodes is presented in this paper. This DC-AC converter produces great amount of voltage levels with minimized components by using hybrid modulation. It has two DC-AC converters coupled in cascade. First one is high frequency DC-AC converter and second one is low frequency DC-AC converter. The high frequency DC-AC converter is only capable to generate two levels with high frequency but the low frequency DC-AC converter is capable to produce great amount of voltage level by utilizing switched diodes. It reduces switching losses, size, cost and volume. Simulation of the circuit is done through MATLAB. The switching algorithm is realized by Spartan 6 FPGA processor board. Simulation outcomes are validated through experimental setup.

Keywords: FPGA processor board, DC-AC converter, Cascaded multilevel inverter (CMLI), hybrid modulation, reduced switches, and switched diodes.

1. Introduction

As multi-level DC-AC converters have potential to generate waveforms with good harmonic range and voltage, they are getting increased attention. Many applications like AC power supplies, drive systems, power grid, and solar system uses multilevel DC-AC converter.

The multilevel commences from three levels. Total Harmonic Distortion of the output waveform draws near to zero, if the amount of levels extent to infinity. One of the important favours of multilevel configuration is without curtailing the output power of DC-AC converter it can reduce harmonics in the output waveform. But, the issues like voltage unbalance, requirement of voltage clamping, circuit packaging and design constraints limit the attainable voltage level.

Numerous traditional multilevel DC-AC converters is available out there. (i) Neutral Point Clamp (NPC) (ii) The Cascaded H-Bridge (CHB) (iii) The Flying Capacitor (FC) multilevel DC-AC converter [1]-[3]. Traditional multilevel DC-AC converters has unique demerits like high amount of switches for getting greater amount of output voltage levels that may demand excessive effort for the installation, the switching complexity, increased quantity of gate driver circuits and the size. Various multilevel DC-AC converter configurations brought together to curtail the switch count, gate drivers, dc sources and the voltage rating of the switches [4] – [9]. Quite a few control methods studied to curtail the harmonics in output [10]. Pulse Width Modulation (PWM) is broadly in a job to regulate the DC-AC converter's output. PWM DC-AC converters are capable to regulate their output voltage and frequency together by carving the wave personalized to distinct needs of applications [11]-[14]. And thereby can lessen the harmonic factors in output. These feature have made them strong contender in numerous power conversion systems.

In the know, there are many control methods, which are employed in multilevel DC-AC converters [15]-[19]. In particular, for Cascaded Multi level DC-AC converter hybrid modulation technique serve the demands [20]-[22].Hybrid modulation stands for the blend of Fundamental frequency PWM (FPWM) and Multi-level Sinusoidal PWM (MSPWM), in order that the output inherits reduction in switching loss from FPWM, and commendable harmonic characteristics from MSPWM. The cascaded multilevel DC-AC converter using capacitors, for voltage dividing, has difficulty in balancing the capacitor voltages [23]. And it demands more efforts to balance the capacitor voltages [24-26].Hence isolated DC sources can be a better choice.

When compared to symmetric multilevel DC-AC converters, asymmetric multilevel DC-AC converters are capable of producing greater amount of output levels using at most equal amount power electronic switches since isolated dc sources are distinct in values. Consequently the installation space and cost are comparatively low [27-28].

In this paper, an asymmetric cascaded multilevel DC-AC converter configuration is proposed with a reduced amount of switches. This configuration is also able to produce the supreme quantity of output voltage levels by cascading and it is appropriate for high and medium power applications.

2. Proposed System

Figure1 introduces the generalized structure of the proposed asymmetric cascaded multilevel DC-AC converter. It comprises a low frequency DC-AC converter with switched diodes placed at the bottom and high frequency DC-AC converter placed at the top in cascade, in order to get required multi-level output. DC voltage sources v_{dc} – $2^n v_{dc}$ are independent to one another. The magnitude of the first voltage source of low frequency DC-AC converter is twice the high frequency DC-AC converter and each voltage source of the low frequency DC-AC converter is twice the magnitude of the preceding voltage source. It has eight primary switches (PS_1-PS_8) and n number of ancillary switches (AS_1 - AS_n) with n number of DC sources and switched diodesin low frequency DC-AC converter.

With the help of Figure2, working principle of a single-phase fifteen-level DC-AC converter (n=2) is explained. It is a modified version of a multi-level DC-AC converter with series/parallel connection of DC sources (MLISPC) [22]. Low frequency DC-AC converter unit is

replaced with the one developed in [4]- [7]. Existing system (MLISPC) is compared with proposed system which is shown in Table1.

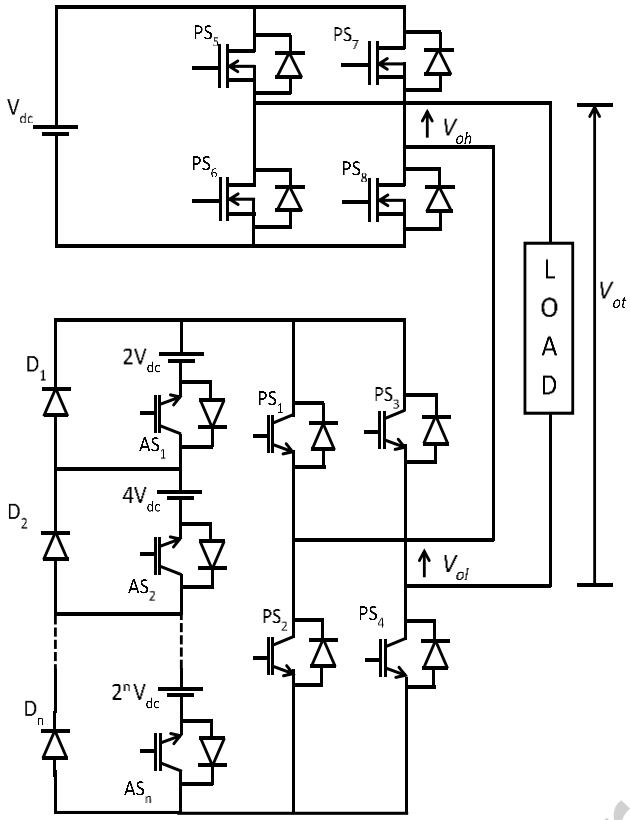


Figure 1. Proposed generalized single-phase cascaded Multi level DC-AC converter structure

The high frequency DC-AC converter comprises of four MOSFET switches PS_5, PS_6, PS_7 and $PS_8$are connected in a bridge fashion with a single DC voltage source which is isolated type. The high frequency gate pulses which is coming out of hybrid modulation for switching PS_5-$PS_8$and corresponding output voltages is displayed in Table 3. The generation of reference wave shape and high frequency gate pulses are explained in detail in segment 3.

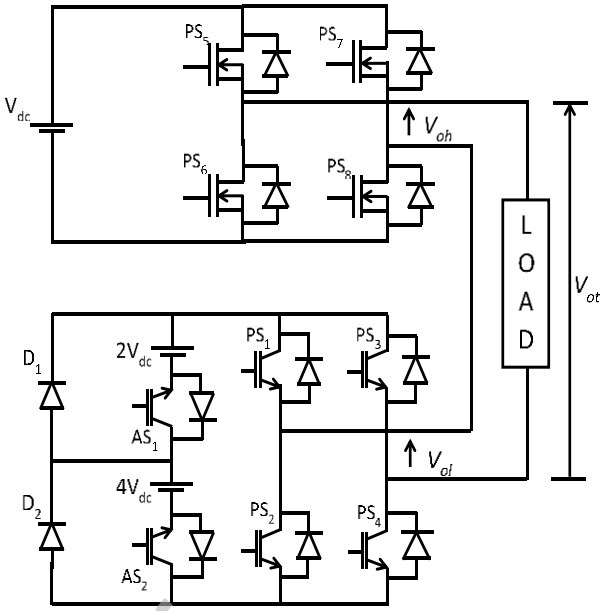


Figure 2. Proposed single-phase cascaded Multi level DC-AC converter structure for 15 level

The low frequency DC-AC converter comprises of six IGBT switches, out of which two of them(AS_1,AS_2) act as ancillary switches and two diodes which is used to switch the sources in order to get multilevel output.

The PWM strategy is designed to operate thePS_1 – PS_4 and AS_1, AS_2 with low frequency, PS_5 – PS_8 withhigh frequency that ultimately reduces the switching losses for the overall circuit operation.

For better comprehension of the circuit operation, the low frequency DC-AC converterappeared in Figure3 is taken for study under various working modes in order to accomplish a number of output voltage levels. The low frequency DC-AC converter was made up of 6 IGBT switches, and 2 Diodes so as to deliver seven different levels of output voltages which is cascaded with the high frequencyDC-AC converter with four MOSFET Switches to deliver a 15 level output voltage with reduced harmonic level.

Table 1 Comparison between two cascadedDC-AC converter structures

Parameters	CMLI[22]			Proposed DC-AC converter		
	Low frequency	**High frequency**	**Total**	**Low frequency**	**High frequency**	**Total**
$\mathbf{N_{switch}}$	3n+1	4	3n+5	n+4	4	n+8
$\mathbf{N_{Level}}$	2n+1	2	4n+3	2^{n+1} - 1	2	2^{n+2} - 1

Where,

n= number of isolated DC sources of low frequency DC-AC converter

N_{Level}= Total number of output voltage levels

= 2(Low frequencyDC-AC converter output levels) + 1

N_{switch}= Total number of switches

Journal Pre-proof

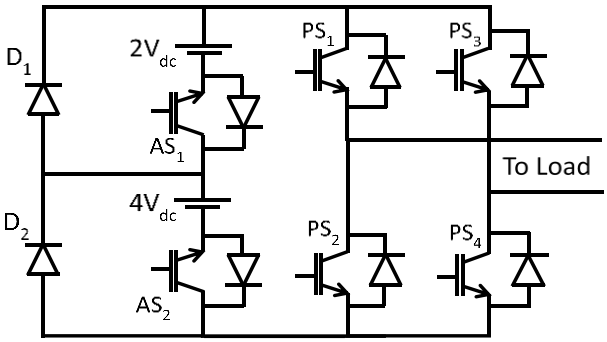


Figure3. Low frequency DC-AC converter

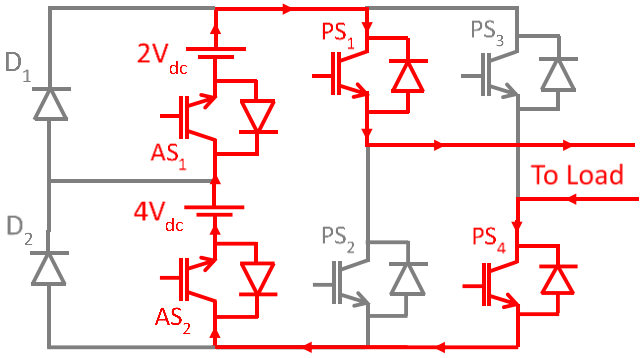
Switches / Voltages	AS_1	AS_2	PS_1	PS_2	PS_3	PS_4	Reference
6 V_{dc}	1	1	1	0	0	1	Figure4(a)
4 V_{dc}	1	0	1	0	0	1	Figure4(b)
2V_{dc}	0	1	1	0	0	1	Figure4(c)
0	1	0	1	0	1	0	Figure5
- 2V_{dc}	0	1	0	1	1	0	Figure6(a)
- 4 V_{dc}	1	0	0	1	1	0	Figure6(b)
- 6 V_{dc}	1	1	0	1	1	0	Figure6(c)

Table 2 Hybrid PWM Switching pattern for low frequency DC-AC converter

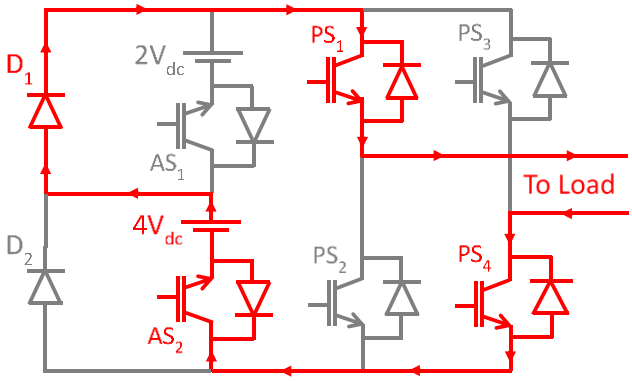
Table 3 Switching pattern for cascaded Multi level DC-AC converter

High frequency DC-AC converter Switches				Low frequency DC-AC converter Switches						Consequent Output Voltage		
PS_5	PS_6	PS_7	PS_8	PS_1	PS_2	PS_3	PS_4	AS_1	AS_2	V_{oh}	V_{ol}	$V_{ot}=V_{oh}+V_{ol}$
1	0	0	1	1	1	1	0	0	1	0 to V_{dc}	6 V_{dc}	6V_{dc} to 7V_{dc}
0	1	1	0	1	1	1	0	0	1	-V_{dc} to 0	6 V_{dc}	5V_{dc} to 6V_{dc}
1	0	0	1	1	0	1	0	0	1	0 to V_{dc}	4V_{dc}	4V_{dc} to 5V_{dc}
0	1	1	0	1	0	1	0	0	1	-V_{dc} to 0	4 V_{dc}	3V_{dc} to 4V_{dc}
1	0	0	1	0	1	1	0	0	1	0 to V_{dc}	2V_{dc}	2V_{dc}to3V_{dc}
0	1	1	0	0	1	1	0	0	1	-V_{dc} to 0	2V_{dc}	V_{dc} to2V_{dc}
1	0	0	1	1	0	1	0	1	0	0 to V_{dc}	0	0 to V_{dc}
0	1	1	0	1	0	1	0	1	0	0 to -V_{dc}	0	0 to -V_{dc}
1	0	0	1	0	1	0	1	1	0	$V_{dc}$to 0	-2V_{dc}	-V_{dc} to -2V_{dc}
0	1	1	0	0	1	0	1	1	0	0 to -V_{dc}	-2V_{dc}	-2V_{dc} to -3V_{dc}
1	0	0	1	1	0	0	1	1	0	$V_{dc}$to 0	-4V_{dc}	-3V_{dc} to -4V_{dc}
0	1	1	0	1	0	0	1	1	0	0 to -V_{dc}	-4V_{dc}	-4V_{dc} to -5V_{dc}
1	0	0	1	1	1	0	1	1	0	$V_{dc}$to 0	-6V_{dc}	-5V_{dc} to -6V_{dc}
0	1	1	0	1	1	0	1	1	0	0 to -V_{dc}	-6V_{dc}	-6V_{dc} to -7V_{dc}

The hybrid PWM switching pattern for obtaining low frequency multilevel voltages (seven) is shown in Table 2. Corresponding operating modes of low frequency DC-AC converter are displayed in Figure4 (positive levels), Figure5 (zerolevel) and Figure6 (negative levels).

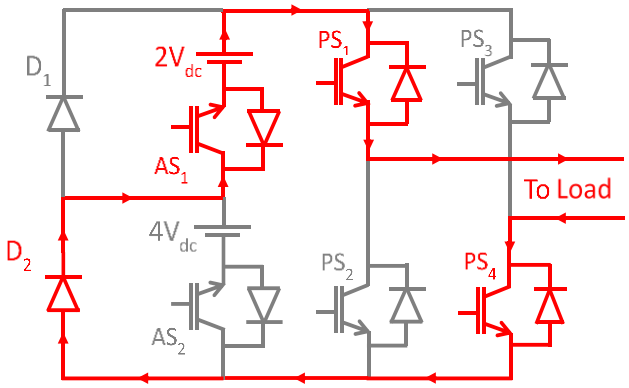


(a)



(b)

Journal Pre-proof



(c)

Figure4. Operating modes and output levels of low frequency DC-AC converter (a) = +6Vdc, (b) = +4Vdc,(c) = +2Vdc

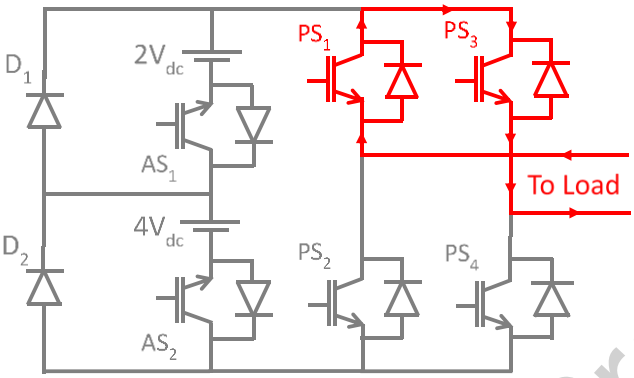
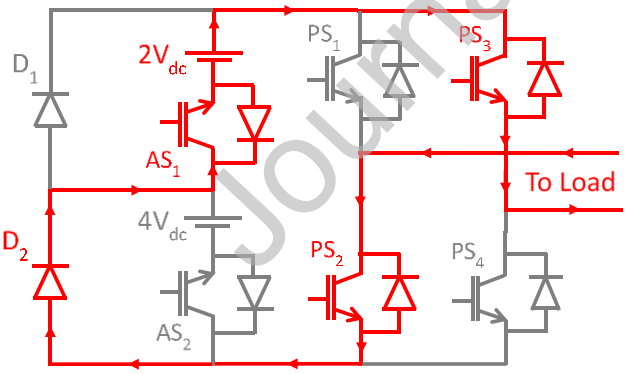
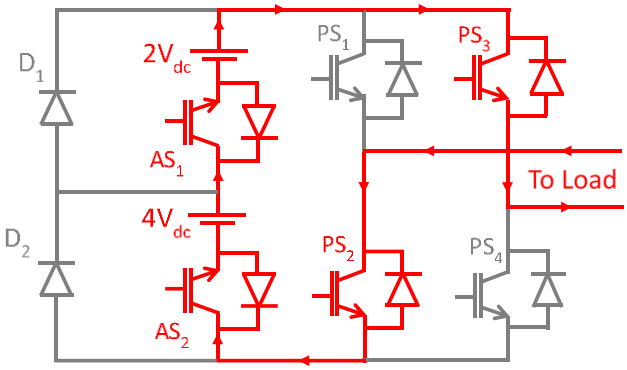


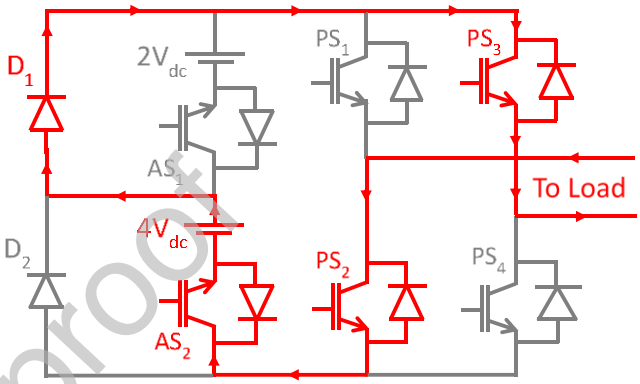
Figure5. Operating mode and output level of low frequency DC-AC converter for V_{dc}= 0



(a)



(b)



(c)

Figure6. Operating modes and output levels of low frequency DC-AC converter (a) = -2Vdc, (b) = -4Vdc, c) = -6Vdc

3. Switching Technique

In the proposed configuration, both high and low frequency switching signals are used. Minimum number of switches operated at high frequency and maximum number of switches operated at low frequency.

This minimizes the losses of switching. The hybrid modulation technique of the proposed converter configuration is described for fifteen levels. Switches PS_5 and PS_8 are driven by contrasting the reference wave R1 with carrier wave C. Switches PS_6 and PS_7 are switched by contrasting the reference wave R2 and the carrier wave C. This high frequency switching is shown in Figure7. Ancillary switches AS_1, AS_2 are switched as displayed in Table 3.

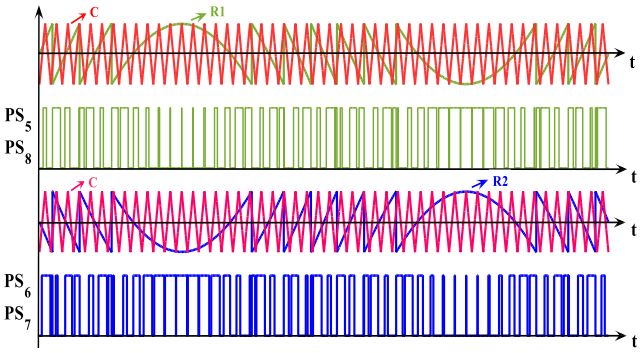


Figure7. Switching sequence of high frequency DC-AC converter

Journal Pre-proof

The first step is to generate reference waveform for the low frequency DC-AC converter, so that the switching patterns for the low frequency DC-AC converter is generatedby comparing reference pulse with the carrier wave.

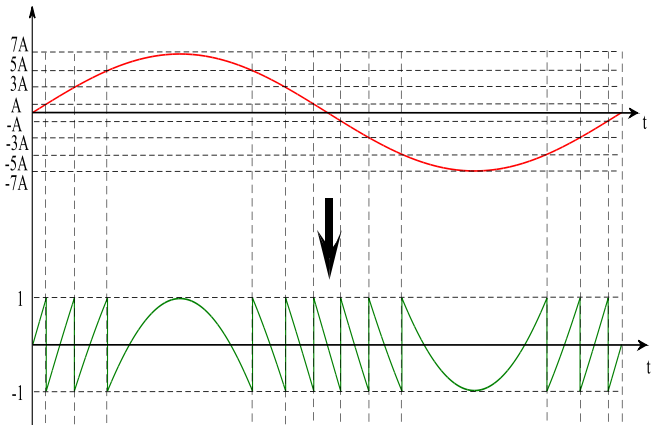


Figure8. Reference Wave formation for a 15 Level DC-AC converter.

The reference wave shape is formed by slicing on the amplitude of the sine wave shape. The aggregate reference wave is created as appeared in Figure 8 and described in (1).

$$V_{ref} = MSin(\omega t) \qquad (1)$$

Where M is the highest amplitude value of the reference waveform. (M = 7 in place of 15 level DC-AC converter). The above condition is downsized as presented in (2).

$$V_{ref,s} = \frac{V_{ref}}{M} \qquad (2)$$

The modulation index M_a is outlined as

$$M_a = \frac{A_r}{MA_c} \qquad (3)$$

Where, M = (N_{level} – 1)/2, N = 15, 31…etc.

A_c = Carrier Amplitude,

A_r = Reference Amplitude.

The above equations can be utilized for higher DC-AC converter levels by means of just altering the value of M. For instance, M = 7 in place of 15 levels, M = 11 in place of 31 levels just to say a couple.

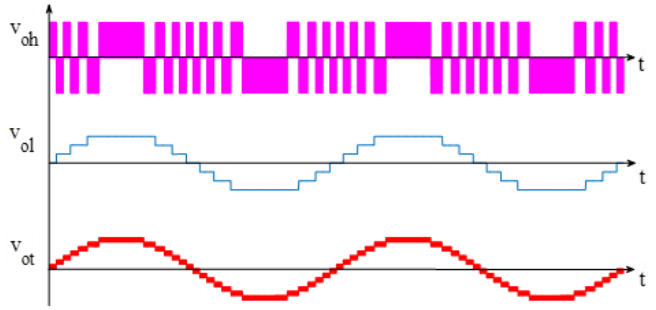


Figure9. Output Waveform Generation for a 15 Level DC-AC converter.

As per the Table 2, with the help of modes in Figure4,Figure5 and Figure6 couple of cases discussed here.

When AS_1 is ON, AS_2 is OFF and PS_1, PS_4 are ON, PS_2, PS_3 are OFF, v_{ol} becomes

$$v_{ol} = 4V_{dc} \qquad (4)$$

When AS_1, AS_2 are ON, PS_1, PS_4 are ON, and PS_2, PS_3 are OFF, v_{ol} becomes

$$v_{ol} = 2V_{dc} + 4V_{dc} = 6V_{dc} \qquad (5)$$

When AS_1 is ON, AS_2 is OFF and S_{C1} are OFF, and PS_2, PS_3 are ON and PS_1, PS_4 are OFF, v_{ol}becomes

$$v_{ol} = -(2V_{dc} + 4V_{dc}) = -6V_{dc} \qquad (6)$$

When AS_1, AS_2 are ON, PS_2, PS_3 are ON and PS_1, PS_4 are OFF, v_{ol}becomes

$$v_{ol} = -4V_{dc} \qquad (7)$$

As needs be, the output voltage waveform of the low frequency DC-AC converter $v_{ol}$and the output voltage waveform of the high frequency DC-AC converter v_{oh}appears as showed up in Figure9.

This segment decides the switching function to produce the fifteen levels in the proposed DC-AC converter. A hybrid PWM switching scheme is utilized to produce the PWM gating pulses. A similar method may be reached out to infer the switching procedure for attaining required output levels. The above equations can be used to generate different levels by simply changing the value of M. For example, M = 7 for 15 and M=5 for 11 levels.

4. Losses Calculation

The mean switching loss P_{sloss} inside the switch produced all through the progress of switch is given by,

$$P_{sloss} = \frac{1}{2} V_{dc} I_{dc} f_s \left(t_{c(on)} + t_{c(off)}\right) \qquad (8)$$

Where $t_{c(on)}$ and $t_{c(off)}$ stands for the switch on and switch off time intervals, correspondingly. For additional transparency, the proposed circuit with fifteen levels is weighed with the known and analogous configurations below. For generalization, the proposed method and also the familiar DC-AC converter circuits are expected to be functioned at the identical switch on and switch off limit intervals and at an equivalent I_{DC}. Then, the mean switching loss P_{sloss} is directly proportional to V_{DC} and f_s.

$$P_{sloss} \alpha\ V_{dc} f_s \qquad (9)$$

The quantity of main switching devices needed for producing 15 levels within the proposed DC-AC converter is 12 and also the voltage over these switches is $V_{dc}$for high frequency DC-AC converter switches (4 no's.), $6V_{dc}$ for low frequency DC-AC converter switches (4 no's.), $2V_{dc}$ for supplementary switches (3 no's.) and $4V_{dc}$ for supplementary switch (1 number). The high frequency DC-AC converter changes its states at high frequency f_s, the low frequency DC-AC converter changes its states at fundamental frequency f_m and also the ancillary switches are driven at double of the fundamental frequency ($2f_m$). Hence, the proposed DC-AC converter's switching losses may be written as,

Journal Pre-proof

$$P_{sloss\,(proposed)} = 4V_{dc} f_s + 4(6V_{dc}) f_m + 3(2V_{dc})(2 f_m) + 1(4V_{dc})(2 f_m) = 4V_{dc}\left[f_s + 6 f_m + 3 f_m + 2 f_m\right] = 4V_{dc}\left[f_s + 11 f_m\right] \quad (10)$$

In the same way, the amount of main switching devices needed for producing 15 levels in MLISPC DC-AC converter is 14 and also the voltage over these switches is V_{dc} for high frequency DC-AC converter switches (4 no's), $6V_{dc}$ for low frequency DC-AC converter switches (4 no's) and $2V_{dc}$ for series/parallel switches (6 no's). The high frequency DC-AC converter changes its states at high frequency f_s, the low frequency DC-AC converter changes its states at fundamental frequency f_m and also the series/parallel switches, switch doubly at the fundamental frequency ($2f_m$). Therefore, the switching losses of the DC-AC converter in[22] may be obtained as,

$$P_{sloss} = 4V_{dc} f_s + 4(6V_{dc}) f_m + 2(4V_{dc})(2 f_m) = 4V_{dc}\left[f_s + 6 f_m + 6 f_m\right] = 4V_{dc}\left[f_s + 12 f_m\right] \quad (11)$$

The switching losses of the DC-AC converter in [23] may be composed as:

$$P_{sloss} = 4V_{dc} f_s + 4(6V_{dc}) f_m + 2(4V_{dc})(2 f_m) = 4V_{dc}\left[f_s + 6 f_m + 4 f_m\right] = 4V_{dc}\left[f_s + 10 f_m\right] \quad (12)$$

In this, however, the number of diodes (8 no's) is not considered for the estimate, in the event that it is taken into the notion, the losses may be more than previous estimates. Likewise, for conventional CHB (symmetrical) DC-AC converters, the switching losses may be found as,

$$P_{sloss\,(symm,CHB)} = 28V_{dc} f_s \quad (13)$$

For asymmetrical cascaded H bridge DC-AC converter with 1:2:4configurations, the switching losses can be attained as,

$$P_{sloss\,(asymm,CHB)} = 28V_{dc} f_s \quad (14)$$

Since $f_s >> f_m$ and from equations (8) - (14), it is obvious that amongst the different well-known configurations, the proposed configuration has the least switching losses while weighed with alternate configurations. In the proposed DC-AC converter, anytime, the maximum amount of switches in operation is just 6 (2 from the high frequency DC-AC converter and utmost 4 from the low frequency DC-AC converter). In this way, the conduction losses P_{closs} of the proposed DC-AC converter are:

$$P_{closs(Max)} = 6 R_{ON} I^2 \quad (15)$$

Where R_{ON} is the inside protection of the individual switch and I is the current flowing the switch. On account of the MLISPC configuration, the quantity of operating switches rises as the amount of levels rises. This as a consequence, magnifies the conduction losses. The same is valid for the almost all of the noteworthy configurations. Subsequently, the conduction losses are bring down on account of the proposed topology when weighed with the MLISPC, the regular symmetrical CHB and asymmetrical CHB DC-AC converters.

5. Simulation Results

The feasibility of the proposed topology is verified using MATLAB/SIMULINK. The simulation is done with the switching algorithm stated in segment 3 and the same technique can be pushed to any necessary number of levels. Thus at high frequency, low voltage rated switches are operated and at fundamental frequency, high-voltage rated switches are operated. Generally high frequency switches are having low voltage rating comparatively and vice versa. This is the generalized model that is low frequency levels can also be generated by varying the amplitude. High frequency DC-AC converter is operated in the range of 40kHz and low frequency DC-AC converter is operated in the range of 50 Hz.

The Load voltage of the 15 level DC-AC converter with High frequency and low frequency converters are simulated and presented in Figure10 and Figure11 respectively.

Table 4 Simulation Parameters and Values

PARAMETERS	LEVEL 15	LEVEL 31
VALUE OF M	7	15
HIGH FREQUENCY DC-AC CONVERTER	47V	22V
LOW FREQUENCY DC-AC CONVERTER	94V	44V
		88V
	188V	176V
LOAD	100Ω &50MH.	

To yield a greater amount of output voltage levels without increasing the quantity of converters and the switching frequency, asymmetric configuration is used. If the number of levels increases, sinusoidality of output waveform will be increased. This model provides the flexibility for the expansion of voltage levels without any introduction of complexity in the power circuit.

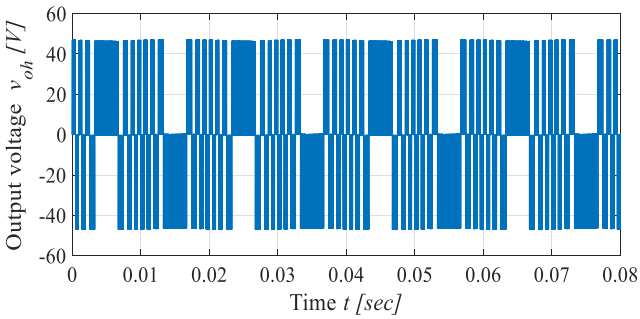


Figure10. Voltage across the high frequency DC-AC converterV_{oh}.

Journal Pre-proof

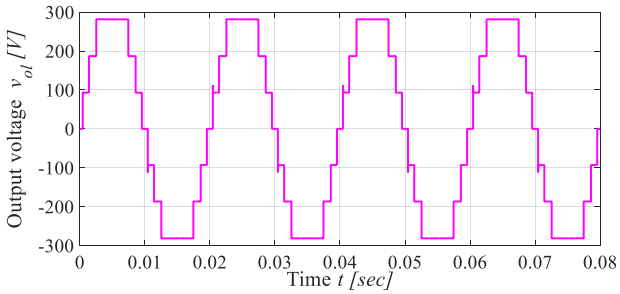


Figure 11. Voltage across the low frequency DC-AC converterV_{ol}

Figure12. Displays the Simulation outcomes of 15-Level output Voltage. By adding the voltage waveforms produced from the low frequency and high frequency DC-AC converter, the aggregate output voltage v_{ot} waveform can be generated.The increased amount of levels results the pure sinusoidal waveform as output. The output current waveform is more similar to the ideal sinusoidal waveform because the R-L load acts as a low-pass filter as shown in Figure13.The proposed DC-AC converter outputs 13 level voltage as displayed in Figure14by just adjusting to M_a=0.85 from 0.99.Output inherits the features of switching-loss reduction and good harmonic performance from hybrid modulation. It is obvious that the more numbers of levels, the lesser the quantity of THD becomes. The magnitudes of harmonics of both voltage and current waveforms are low.

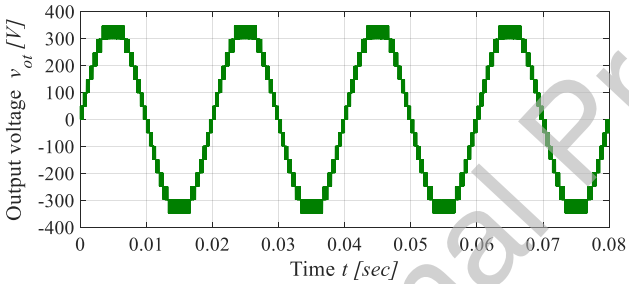


Figure12. Output voltage over the load (15 Levels) withM_a=0.99

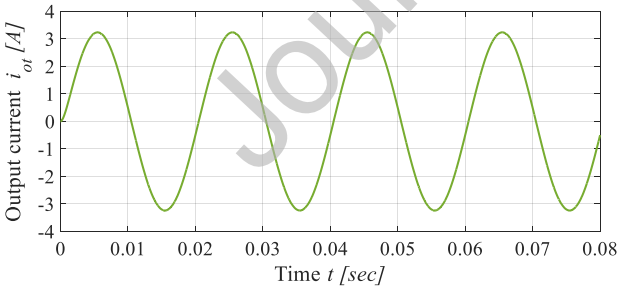


Figure 13. Load Current waveform of the proposed DC-AC converter (15 Levels)

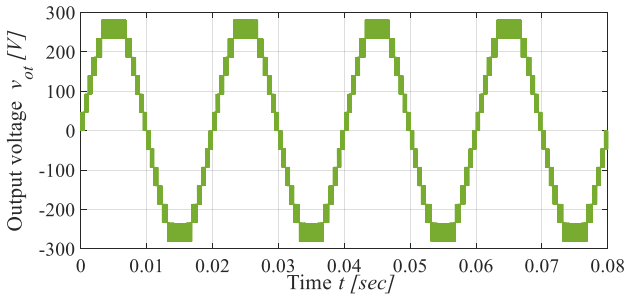


Figure 14. Output voltage over the load (13 Levels) with M_a =0.84

6. Experimental Results

The proposed cascaded multi-level DC-AC converter is prototyped using FPGA SPARTAN 6 through Xilinx and the hardware schematic organisation for fifteen level output voltage is shown in Fig 15. It has two different DC-AC converters in cascade. Both the DC-AC converters are operating at different frequency as the name suggests low frequency DC-AC converter and the high frequency DC-AC converter. The high frequency DC-AC converter is fitted out using a separate DC source which is of isolated type and the low frequency DC-AC converter using another set of DC sources, which are of isolated type with distinct values. Each of the DC-AC converters is getting PWM switching pulses individually from the FPGA module.

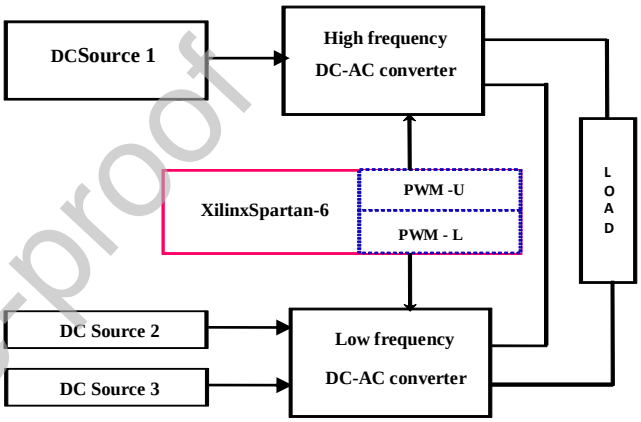
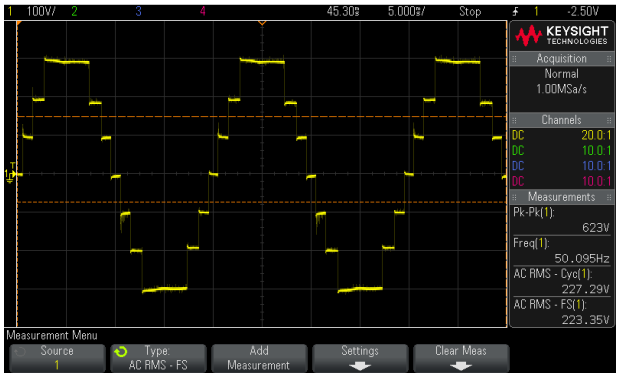
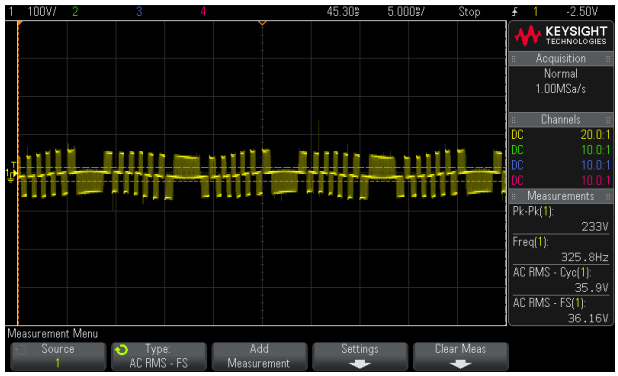


Figure15. Hardware schematic organization of the proposed cascaded DC-AC converter for 15 Levels



(a)

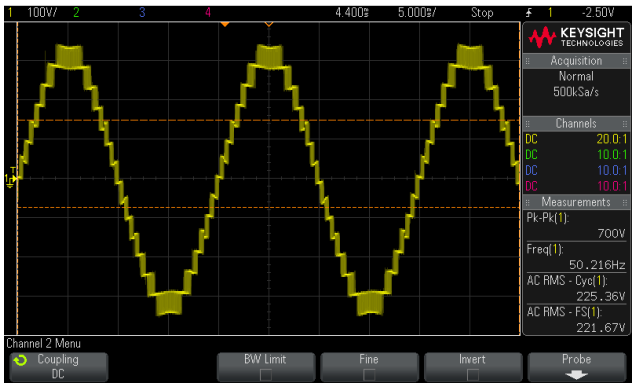


(b)

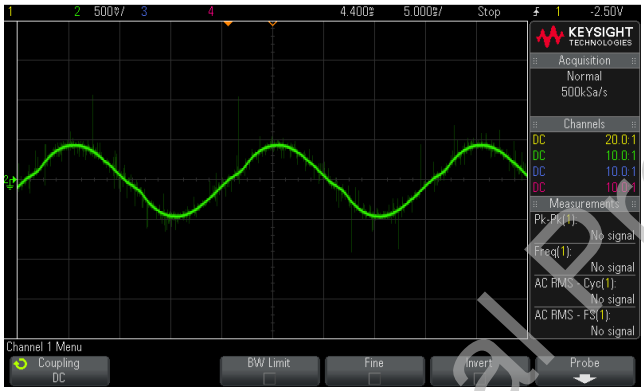
Journal Pre-proof

Figure16. Experimental results (a)Voltage over the low frequency DC-AC converterV_{ol} (b) Voltage over the high frequency DC-AC converterV_{oh}

For the proposed DC-AC converter (15 levels) the Xilinx Spartan 6 Controller delivers 10 individual pulses of PWM type for 10 switches in the DC-AC converter of 4 in high frequency level and 6 in the low frequency level. Four pulses of high frequency type is delivered by PWM-U and six pulses of low frequency type is delivered by PWM-L.



(a)



(b)

Figure17. Experimental results (a) Output voltage over the load (15 Levels) (b) Output current waveform through the load, for modulation index M_a=0.99.

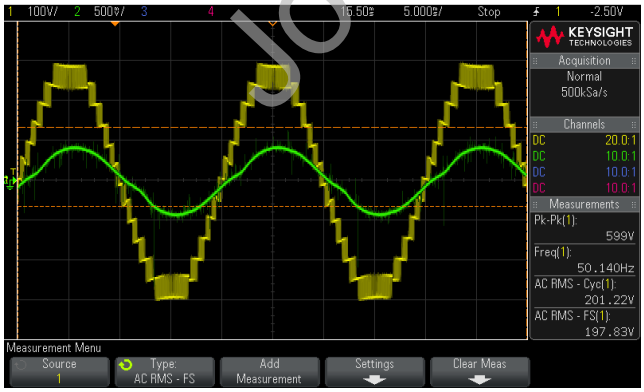


Figure18. Output voltage over the load (13 Levels) and Output current waveform through the load, for modulation index M_a=0.85.

The Output voltage of low frequency and high frequency DC-AC converter is depicted in Figure 16. The Output voltage and Current with load is shown in Figure 17. The Output voltage and current waveform through the load, for reduced modulation index (Ma=0.85) is shown in Figure 18.

The simulation results are validated in Figure 16, Figure 17 and Figure 18.

7. Conclusion

In this paper, a modified asymmetric cascaded multilevel DC-AC converter structure is presented and a hybrid PWM strategy was designed and is upgraded into a new asymmetrical cascaded multilevel DC-AC converter structure. The proposed structure generates a 15 -level output voltage with minimum amount of switches. The proposed method proves that there is a substantial improvement in the sinusoidality by means of greater amount of output voltage level. Also this paper proposes a new approach, which focuses on the effectiveness and importance of the PWM control strategy on the performance of the single phase asymmetric multilevel DC-AC converters. In the proposed structure, low frequency DC-AC converter basic units can be cascaded for high voltage applications. Therefore, the proposed cascaded asymmetric structure is recommended for medium and high voltage applications.

Conflict of Interest

This paper has not communicated anywhere till this moment, now only it is communicated to your esteemed journal for the publication with the knowledge of all co-authors.

Ethical approval

This article does not contain any studies with human participants or animals performed by any of the authors.

REFERENCES

[1] J. Rodriguez, Jih-Sheng Lai and Fang ZhengPeng, "Multilevel inverters: a survey of topologies, controls, and applications," in IEEE Transactions on Industrial Electronics, vol. 49, no. 4, pp. 724-738, Aug. 2002.

[2] J. Rodriguez, S. Bernet, P. K. Steimer and I. E. Lizama, "A Survey on Neutral-Point-Clamped Inverters," in IEEE Transactions on Industrial Electronics, vol. 57, no. 7, pp. 2219-2230, July 2010.

[3] M. Malinowski, K. Gopakumar, J. Rodriguez and M. A. Perez, "A Survey on Cascaded Multilevel Inverters," in IEEE Transactions on Industrial Electronics, vol. 57, no. 7, pp. 2197-2206, July 2010.

[4] E.Babaei, Sara Laali, Zahra Bayat, “A Single-Phase Cascaded Multilevel Inverter Based on a New Basic Unit with Reduced Number of Power Switches”,

in IEEE Transactions on Industrial Electronics,2015, vol. 62, no. 2, pp. 922-929.

[5] E. Babaei, S. Alilu, and S. Laali, "A new general topology for cascaded multilevel inverters with reduced number of components based on developed H-bridge," IEEE Trans. Ind. Electron., 2014,vol. 61, no. 8, pp. 3932–3939.

[6] EbrahimBabaei, Mohammad FarhadiKangarlu, FarshidNajatyMazgar," Symmetric and asymmetric multilevel inverter topologies with reduced switching devices" in Electric Power Systems Research, May 2012, Volume 86, pp 122-130

[7] E. Babaei, S. H. Hosseini, G. B. Gharehpetian, M. TarafdarHaque, and M. Sabahi, "Reduction of dc voltage sources and switches in asymmetrical multilevel converters using a novel topology," Elect. Power Syst. Res., 2007, vol. 77, no. 8, pp. 1073–1085.

[8] Madan Kumar Das, Kartick Chandra Jana, Akanksha Sinha, "Performance evaluation of an asymmetrical reduced switched multi-level inverter for a grid-connected PV system" IET Renewable Power Generation, Volume 12, Issue 2, February 2018, p. 252 – 263

[9] S.A. Ahamed Ibrahim, AnbalaganPalanimuthu, M.A. JagabarSathik, "Symmetric switched diode multilevel inverter structure with minimised switch count" The Journal of Engineering, Volume 2017, Issue 8, 2017 , p. 469 – 478

[10] P.D. Evans, P.R. Close, " Harmonic distortion in PWM inverter output waveforms" IEE Proceedings B (Electric Power Applications), Volume 134, Issue 4, 1987 , p. 224 – 232

[11] A. A. Boora, A. Nami, F. Zare, A. Ghosh, and F. Blaabjerg, "Voltage sharing converter to supply single-phase asymmetric four-level diode clamped inverter with high power factor loads," IEEE Trans. Power Electron., 2010,vol. 25, no. 10, pp. 2507–2520.

[12] S.BusquetsMonge,J.Rocabert,P.Rodriguez,S.Alepuz,J.Bordonau,"Multilevel Diode Clamped Converter for Photovoltaic Generators With Independent Voltage Control of Each Solar Array," IEEE Trans. on Industrial Electronics,2008, vol. 55, no. 7, pp. 2713-2723.

[13] Rekha Agrawal, Shailendra Jain , "Multilevel inverter for interfacing renewable energy sources with low/medium- and high-voltage grids" IET Renewable Power Generation, Volume 11, Issue 14, December 2017, p. 1822 – 1831

[14] T.W. Chun, Q.V. Tran, H.H. Lee, H.G. Kim, E.C. Nho, "A simple capacitor voltage balancing scheme for the cascaded five-level inverter fed AC machine drive" 6th IET International Conference on Power Electronics, Machines and Drives (PEMD 2012), 2012, p. 104 – 104

[15] S. Bifaretti, L. Tarisciotti, A. Watson, P. Zanchetta, A. Bellini, J. Clare," Distributed commutations pulse-width modulation technique forhigh-power AC/DC multi-level converters" IET Power Electronics, Volume 5, Issue 6, 2012 , p. 909 – 919

[16] A.M. Massoud, S.J. Finney, A. Cruden, B.W. Williams, " Mapped phase - shifted space vector modulation for multi - level voltage - source inverters" IET Electric Power Applications, Volume 1, Issue 4, 2007 , p. 622 – 636

[17] R. Rabinovici, D. Baimel, J. Tomasik, A. Zuckerberger, " Series space vector modulation for multi-level cascaded H-bridge inverters" IET Power Electronics, Volume 3, Issue 6, 2010 , p. 843 - 857

[18] Chung-Ming Young, Sheng-Feng Wu, " Selective harmonic elimination in multi-level inverter with zig-zag connection transformers " IET Power Electronics, Volume 7, Issue 4, 2014 , p. 876 – 885

[19] A.M. Khalkho, S. Das, A.K. Chattopadhyay, " Phase disposition PWM Five Level inverter short switch diagnosis using DWT and Ann" Michael Faraday IET International Summit 2015, 2015, p. 70 (7.) - 70 (7.)

[20] Ki-Mok Kim, Won-Shik Choi, Ki-Hyeon Park, "Novel carrier-based hybrid pulsewidth modulation method for cascaded capacitor -clamp multilevel inverter" IET Power Electronics, Volume 7, Issue 10, 2014, p. 2678 – 2686.

[21] C. Govindaraju ," Efficient sequential switching hybrid modulation techniques for multi phasemulti level inverters " IET Power Electronics, Volume 4, Issue 5, 2011 , p. 557 – 569.

[22] Y. Hinago and H. Koizumi, "A single-phase multilevel inverter using switched series/parallel DC voltage sources," IEEE Trans. Ind. Electron., 2010, vol. 57, no. 8, pp. 2643–2650.

[23] M. Kaliamoorthy, V. Rajasekaran, I. G. C. Raj, and L. H. T. Raj, "Experimental validation of a cascaded single phase H-bridge inverter with a simplified switching algorithm," Journal of Power Electronics, Vol. 14, No. 3, pp. 507-518, May 2014.

[24] SR Ponnusamy, M Subramaniam, GCR Irudayaraj, K Mylsamy,"An Improved Switching Topology for Single Phase Multilevel Inverter with Capacitor Voltage Balancing Technique", Journal of Power Electronics, Vol. 17, No. 1, pp. 115-126, January 2017.

[25] T.W. Chun, Q.V. Tran, H.H. Lee, H.G. Kim, E.C. Nho, "A simple capacitor voltage balancing scheme for the cascaded five-level inverter fed AC machine drive" 6th IET International Conference on Power Electronics, Machines and Drives (PEMD 2012), 2012, p. 104 – 104.

[26] M. Khazraei, H. Sepahvand, K. A. Corzine and M. Ferdowsi, "Active Capacitor Voltage Balancing in Single-Phase Flying-Capacitor Multilevel Power Converters," in IEEE Transactions on Industrial Electronics, vol. 59, no. 2, pp. 769-778, Feb. 2012.

Journal Pre-proof

[27] A. Mokhberdoran and A. Ajami, "Symmetric and Asymmetric Design and Implementation of New Cascaded Multilevel Inverter Topology," in IEEE Transactions on Power Electronics, vol. 29, no. 12, pp. 6712-6724, Dec. 2014.

[28] C. Dhanamjayulu and S. Meikandasivam, "Implementation and Comparison of Symmetric and Asymmetric Multilevel Inverters for Dynamic Loads," in IEEE Access, vol. 6, pp. 738-746, 2018.

[29] Shuvo, S., Hossain, E., Islam, T., Akib, A., Padmanaban, S., & Khan, M. Z. R. (2019). Design and Hardware Implementation Considerations of Modified Multilevel Cascaded H-Bridge Inverter for Photovoltaic System. *Ieee Access*, *7*, 16504-16524.

[30] Chokkalingam, B., Bhaskar, M. S., Padmanaban, S., Vigna, K. R., & Iqbal, A. (2019). Investigations of Multi-Carrier Pulse Width Modulation Schemes for Diode Free Neutral Point Clamped Multilevel Inverters. J. *Power Electron*, *19*, 702-713.

Arun Prasad Deenadayalan was born on June 02, 1985. He received his B.E. in Electrical and Electronics Engineering in 2006 and M.E. in Power Electronics and Drives in 2011 from Anna University, Chennai, Tamil Nadu, India. He is currently pursuing his Ph.D. in Power Electronics and Drives at Anna University, Chennai, Tamil Nadu, India. His research interests include Multi-level inverters, switching strategies, and their applications. He is currently an Assistant Professor at the Department of Electrical and Electronics Engineering at the PSNA College of Engineering and Technology, Dindigul, Tamil Nadu, India.

Dr.K.Mahadevan is Professor of Electrical and Electronics Engineering, PSNA College of Engineering and Technology, Dindigul, India. He graduated in Electrical and Electronics Engineering in 1993 and Post graduated in Industrial Engineering in 1997 and PhD in 2006 from Madurai Kamaraj University, Tamilnadu, India. He has more than 22 years of teaching experience. He has published several papers in peer reviewed international journals of high reputed and has presented research papers in more than 35 national and international level conferences. His field of interest includes Electrical circuits, Electromagnetic Fields, Power system engineering and Optimization Techniques.

Arul Prasanna Mark was born on May 18, 1985. He received his B.E. in Electrical and Electronics Engineering in 2006 and M.E. in Power Electronics and Drives in 2008 from Anna University, Chennai, Tamil Nadu, India. He received his Ph.D. from Anna University, Chennai, Tamil Nadu, India in 2015. His research interests include Power Electronics and Drives, Current Source Inverters, Embedded Automation, AC drives and their applications. He is currently working as an Associate Professor in the Department of Electrical and Electronics Engineering at the PSNA College of Engineering and Technology, Dindigul, Tamil Nadu, India.

Journal Pre-proof