Synaptic Weight Coverage and Potential Output in Synaptic Pass-Transistors

Yeonsu Kang, Danyoung Cha
Department of Electronics Engineering
Pusan National University
Pusan 46241, Republic of Korea
yskang96@pusan.ac.kr

Sungsik Lee
Department of Electronics Engineering
Pusan National University
Pusan 46241, Republic of Korea
sungsiklee@pusan.ac.kr

***Abstract*— In this work, we present the study on a weight modulation of a synaptic transistor with a charge trapping layer, demonstrating the voltage-to-voltage transfer by employing a load resistor at the output and the pass-transistor operation concept. The synaptic weight as a transfer-efficiency is defined with the synaptic output in terms of the equivalent transistor resistance and load. Since the channel resistance of synaptic transistor can be modulated by the charge trapping, the synaptic plasticity is explained with a relative dominance of the transistor's resistance with the fixed load resistance. To show the weight modulation following the theoretical analysis, respective simulations for the depression and facilitation are conducted.**

Keywords—Charge trapping layer (CTL), potential output, pass-transistor, synaptic weight plasticity, synaptic transistor.

I. INTRODUCTION

A synaptic device is a major component comprising a neuromorphic circuit for a brain-like computing, which mimics a synapse. Here, the connection between neurons is called a synapse, where the action potential transmission is controlled, depending on its signal experiences. The control appears as a variation of synaptic connection strength, i.e. weight [1, 2].

One of the several synaptic devices emulating the biological synapse, a synaptic transistor has the three terminals available for the synaptic input, output, and back-propagation (BP) signal. The experience-based transfer regulation has been demonstrated by inserting an additional insulating layer below the gate metal, where the charges are caught or pushed out depending on an input and back-propagated signal [3,4].

However, the synaptic transistor alone produces the current output. Since a biological synapse transmits the action potential [5, 6], we here provide the analysis and simulations on a synaptic-transistor weight-plasticity with a resistor at the output for the voltage-to-voltage transfer, rather using the current-to-voltage conversion circuit.

II. THEORETICAL SYNAPTIC OPERATION

A. Synaptic voltage output

The synaptic transistor is a transistor with a charge trapping layer (CTL) between the gate and channel layer, as shown in Fig.1(a), and here a resistor (R_L) is connected to the source output. The terminals of a synaptic transistor are corresponded to synaptic signals, e.g. the input (V_I) to drain, BP-input (V_{BP}) to the gate, and output (V_O) to source terminal. The operation of the circuitry in Fig.1(a) is called the pass-transistor operation, where the voltage signal transfer is passed or blocked by the gate bias (V_G) and threshold voltage (V_T) [7]. Following the pass-transistor concept, the synaptic output is represented as follows [8],

$$V_O = V_G - V_T = V_{BP} - V_T . \quad (1)$$

Note that, this formula is applicable only for the synaptic transistor operating in the above-threshold regime. In (1), with CTL, V_T can be modulated by the trapped charges. For the case

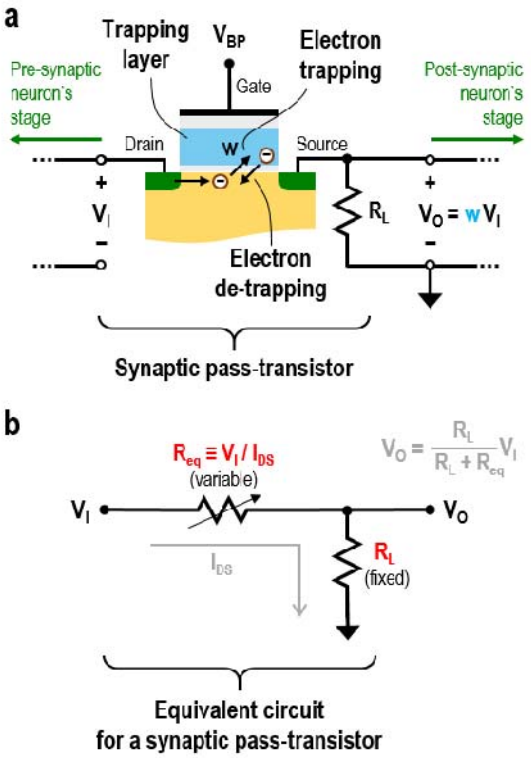

Fig.1. (a) Schematic diagram of a synaptic transistor with a trapping layer and resistor load for a potential output and (b) equivalent representation for synaptic pass-transistors as a series of two resistors.

of n-channel metal-oxide-semiconductor field-effect transistor (i.e. n-MOSFET, n-MOS), where electrons are the majority carriers, V_T as a function of electron charge (Q_{TL}) is defined as follows,

$$V_T = V_{T0} - \frac{|Q_{TL}|}{C_i}. \quad (2)$$

Here, V_{T0} is an initial V_T, and C_i is a gate-insulator capacitance per area.

Since (1) is valid only for the above-threshold operation, macroscopically, this can be represented as the two resistors in series shown in Fig.1(b) to consider the sub-threshold operation together. R_{eq} is the equivalent resistance of SPT defined as

$$R_{eq} \equiv V_I / I_{DS}. \quad (3)$$

Note that, what affects R_{eq} is the Q_{TL}, assuming the given signals on the synaptic transistor terminals, e.g. V_I and V_{BP}, are fixed. From Fig.1(b), simply employing the voltage distribution law, V_O can be deduced as follows,

$$V_O = \frac{R_L}{R_{eq} + R_L} V_I. \quad (4)$$

B. Synaptic weight

As mentioned above, the potential-signal transfer in a synapse is regulated by its weight. The received signal can be fully transferred to the post-synaptic neuron, however, it can also be blocked. Thus, the weight (w) is a transfer-efficiency between the input and output signal, which can be represented as,

$$V_O = wV_I. \quad (5)$$

According to (4) and (5), w of the synaptic transistor becomes

$$w = \frac{R_L}{R_{eq} + R_L}. \quad (6)$$

From (6), w can be zero when $R_{eq} >> R_L$, while it becomes unity when $R_{eq} << R_L$. Here, R_{eq} is the variable resistance which can be modulated by the inputs and trapped charges. However, R_L should be determined as a certain value, considering the post-synaptic stages following the synaptic devices. Therefore, we suggest an R_L selection rule. Under fixed V_I and gate read bias (V_{read}), R_L should be at least 2 orders of magnitude bigger than R_{eq} for w=1, as well as at least 2 orders of magnitude smaller than R_{eq} for w=0. The two extreme cases (i.e. w=1, w=0) correspond to a fully-facilitated and fully-depressed state, respectively.

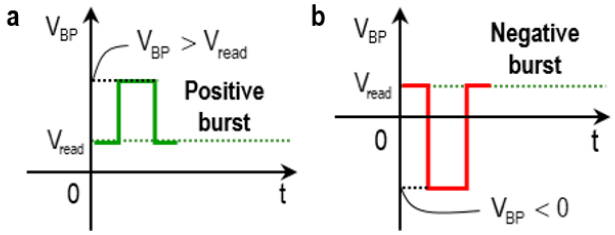

Fig.2. (a) a positive burst and (b) a negative burst with a basis of gate read-bias (V_{read}) required for the depression and facilitation.

C. Synaptic Plasticity

The experience-based weight plasticity varies with charge trapping or de-trapping. Assuming a fixed positive V_I, V_{BP} should be the pulsed signal to make electrons trapped with sufficient energy. The respective bursts are shown in Fig.2 for weight depression and facilitation in an n-MOS SPT. Following the selection rule, after a certain time for the repeated positive bursts, the R_{eq} would reach the maximum for the same V_{read}, thus $R_{eq}>>R_L$ and full-depression. From the zero-charged initial and fully de-trapped state, R_{eq} would become zero by the repeated negative bursts, thus $R_{eq}<<R_L$ and the full-facilitation.

III. Simulations and Results

The synaptic plasticity simulations and results are shown to examine the R_L selection rule and weight modulation with the potential transfer. The structural and material parameters of an n-MOS SPT to be simulated are shown in Fig.3. Here, 1MΩ load is given at the output, based on the R_L selection rule. The certain R_L is determined by the current-voltage sweep test for the initial synaptic transistor without R_L, before the plasticity simulation. With V_I = 0.1V and V_{read} = 0.2V, the initial R_{eq} calculated with (3) is found as nearly 10kΩ. Thus, R_L 2 orders bigger than R_{eq} becomes 1MΩ, as the R_{eq} expected at the full-depression to be 100MΩ.

The pulses for the depression and facilitation are shown in Fig.4(a) and (d), respectively. The same V_I and V_{read} are applied, while the positive or negative pulses are applied for depressing or facilitating SPT with the basis of V_{read}. Note that, to see the progress from unity to zero weight and its inverse, the facilitation is simulated after the full-depression. The respective

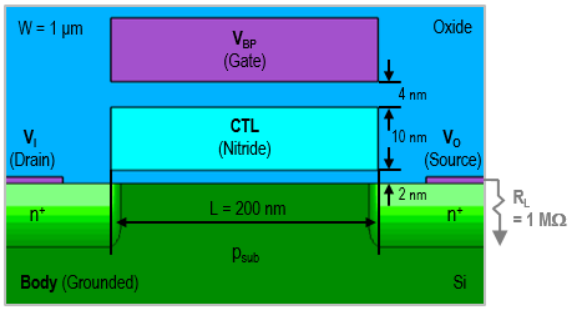

Fig.3. Device structure and signals of a synaptic pass-transistor with a nitride charge trapping layer (CTL) for simulations. Here, 1 MΩ load is connected to the source terminal. Silicon doping densities for the source / drain diffusion layers (n^+) and substrate (p_{sub}), are $n^+ = 5\times10^{17}$ /cm^3 and $p_{sub} = 5\times10^{14}$ /cm^3, respectively.

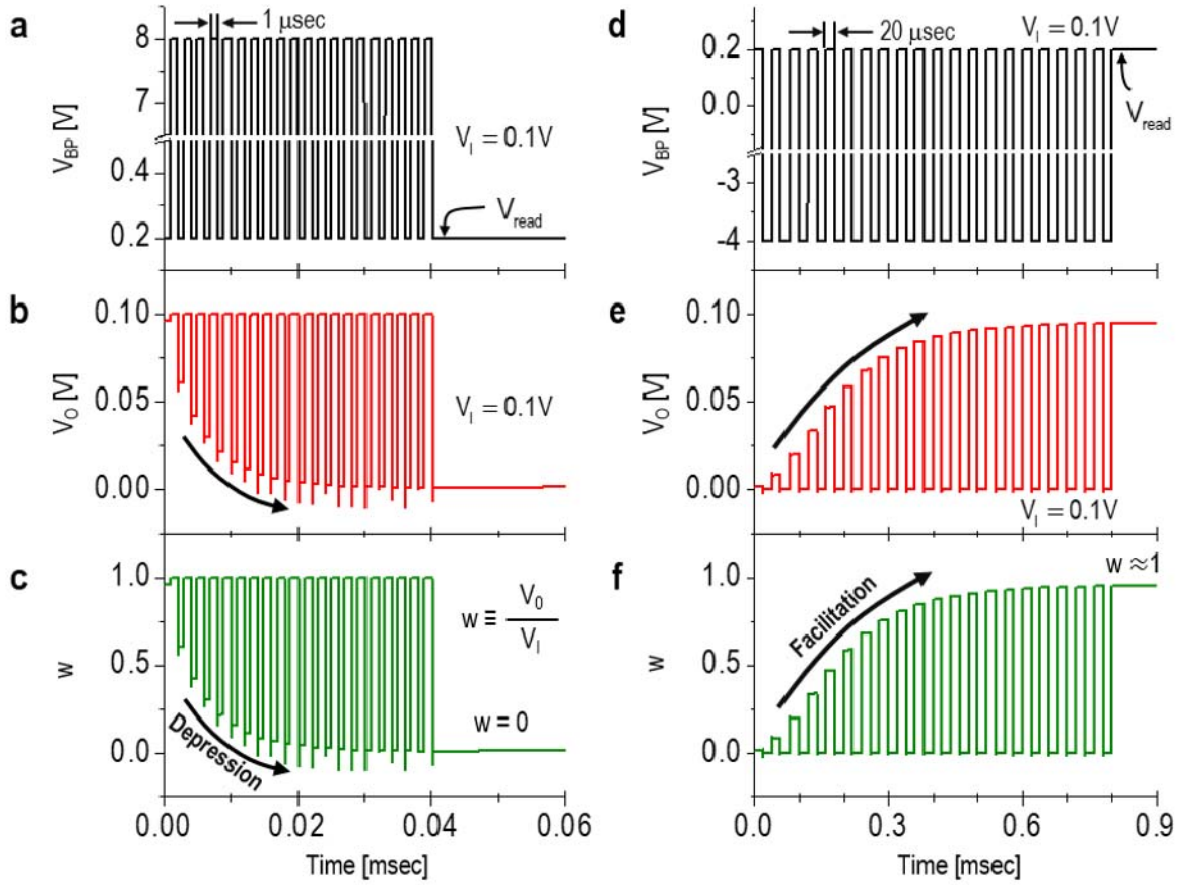

Fig.4. (a) Applied BP-signal for depression, (b) following voltage output, and (c) weight depression until $w = 0$. From (d) to (f), BP-signal for facilitation, voltage output, and weight facilitation, respectively.

outputs and weight variations are shown below the BP-signals. In Fig.4(c), the weight values at every read-voltage period decrease along the time, and finally achieves a full-depression. On the other hand, in Fig.4(f), w increases as the pulses are repeated and it reaches almost unity, thus a full-facilitation.

From the full-depression and full-facilitation results, it can be said that the two-order-magnitude difference between R_L and R_{eq} at w=0 and w=1 is suitable for the general weight modulation in SPT. The given simulation and results show the validity of the selection rule macroscopically, however, more can be studied to examine the load selection rule. The study on electron trapping or de-trapping with simulations, e.g. charge concentration or threshold voltage variations, are expected for more precise physical analysis.

IV. Conclusion

Considering the synaptic weight as a transfer-efficiency, the weight modulation of SPTs has been theoretically analyzed and confirmed with simulations. It is found that the synaptic plasticity is similar to the pass-transistor operation which allows the synaptic transistor to transfer the potential, like a biological synapse. Employing the R_L selection rule suggested, the weight modulation with charge trapping was analyzed. Besides, the synaptic plasticity simulation results are shown. Finally, it is found that the synaptic pass-transistor concept allows the voltage transfer, as well as almost full-range of modulation from full-depression to full-facilitation.

Acknowledgment

This research was supported in part by Samsung Electronics (201900610001) and the Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Science, ICT & Future Planning (NRF-2018R1C1B6001688). And authors thank to the Creative Human Resource Development Program for IT Convergence of BK21PLUS.

References

[1] R. Thompson, "The neurobiology of learning and memory," *Science,* vol. 233, no. 4767, pp. 941-947, 1986.
[2] D. O. Hebb, *The organization of behavior: A neuropsychological theory*. Psychology Press, 2005.
[3] C. Diorio, P. Hasler, A. Minch, and C. A. Mead, "A single-transistor silicon synapse," (in English), *Ieee T Electron Dev,* vol. 43, no. 11, 11, pp. 1972-1980, 1996.
[4] S. Ramakrishnan, P. E. Hasler, and C. Gordon, "Floating Gate Synapses with Spike-Time-Dependent Plasticity," *IEEE Transactions on Biomedical Circuits and Systems,* vol. 5, no. 3, pp. 244-252, 2011.
[5] B. Katz and R. Miledi, "Further study of the role of calcium in synaptic transmission," *The Journal of Physiology,* vol. 207, no. 3, pp. 789-801, 1970.
[6] M. Ludwig and Q. J. Pittman, "Talking back: dendritic neurotransmitter release," *Trends in Neurosciences,* vol. 26, no. 5, pp. 255-261, 2003.
[7] A. S. Sedra and K. C. Smith, *Microelectronic Circuits*. Oxford University Press, 2010.
[8] C. Chiasson and V. Betz, "Should FPGAS abandon the pass-gate?," in *2013 23rd International Conference on Field programmable Logic and Applications*, 2-4 Sept. 2013 2013, pp. 1-8.