A Novel Current Controller for Grid-Connected Voltage-Source-Inverters

Hua F. Xiao, *Senior Member, IEEE*, Mingming Li, Liliang Wu, and Ming Cheng, *Fellow, IEEE*

***Abstract*—In this paper, a new open-loop current controller based on model prediction method for grid-connected Voltage-Source-Inverters (VSIs) is proposed, which consists of two proportional factors and a delay part (Proportional-Proportional-Delay, PPD). Firstly, the working principle of the PPD controller is explained from the combined step response perspective based on a L-R load, and parameter constraints of PPD controller are derived and discussed from the time domain and differential-integral transform perspectives, respectively. After that, parameter design rules of PPD controller are given by considering the constraint of switching frequency. Due to the sensitivity of the model prediction method to non-ideal factors, such as voltage drops of semiconductor devices, sampling and driving delays, etc., influences of these non-ideal factors on performance of PPD controller are discussed in this paper, and corresponding compensation strategies are given as well. Finally, the effectiveness of proposed PPD controller and its compensation strategy against non-ideal factors are verified by experimental results from a 3kW prototype in laboratory.**

***Index Terms*—Open loop, PPD controller, Parameter design, Compensation strategy**

I. Introduction

In recent years, depletion of traditional fossil energy and environment pollution have been gaining increasingly concern. Renewable energy sources, such as wind and solar power generations, are expanding around the globe at record rates. Taking China as example, both of wind and solar power generations take the first place in the accumulative installation capacity around the world since 2015. As main interface units between renewable energy and power utility, Voltage Source Inverters (VSIs) have been commonly used [1-3]. Therefore, the quality of grid-in currents and operation safety of the inverters are dominated by the control performance of VSIs.

Currently, there are some common current controllers, such as hysteresis controller, Proportional-Integral (PI) controller, Proportional-Resonant (PR) controller, repetitive controller, etc. used in grid-connected VSIs. Hysteresis controller features simplicity and fast dynamic performance but unfixed switching frequency, which results in difficulty of filter designs [4-5]; PI controller in stationary coordinate is mature in industry applications, but its static tracking and harmonic suppression performance are not acceptable in advanced applications. However, PI controller in rotating coordinate improves the static tracking performance but increases the intercoupling of channels, as a consequence, the dynamic performance is limited [6-7]. PR controller has been extensively studied for grid-connected VSIs in recent decade. This controller has infinite gain at designed resonance point in theory, and is able to track sinusoidal current without static errors. However, PR controller is sensitive to components' parameters, for example, the frequency deviation would cause significant decrease of control precision [8-9]. Repetitive controller based on internal model principle is also able to track sinusoidal current, but its dynamic performances is poor [10-12].

As a new branch of grid-in current controllers, model predictive control (MPC) calculates the optimal switching combination upon inverter model, current state and reference information, etc. and features fast dynamic performance and flexibility but heavy calculation burden, model dependent, and unfixed switching frequency[13-20]. A MPC strategy with reduced calculation burden was proposed in [18], which establishes a series of rules to identify the redundant switching states at switching frequency scale, therefore, the complexity of MPC is reduced. However, the switching frequency is still not constant, and the control precision will be affected if the identify rules are not reasonable.

In order to maintain constant switching frequency of MPC, an improved continuous current MPC strategy with integrator and Kalman filter was proposed in [19]. Compared with traditional MPC, this method can reduce the computational burden and improve the quality of grid-in current. However, the control strategy is complicated and control parameters are difficult to be settled. In [20], digital differentiators with forward difference and backward difference are used to replace the differential operator in the equations of state, as a result, this strategy does not need to construct the objective function, and also maintain constant frequency control. However, high frequency noises are introduced into the control system, and the calculation burden is still high.

Manuscript received July 02, 2019; revised October 23, 2019; accepted November 25, 2019. This work was supported in part by the National Natural Science Foundation of China Under Grant 51577033, in part by the Natural Science Foundation of Jiangsu Province BK20171360, in part by the Fundamental Research Funds for the Central Universities.

The authors are with the College of Electrical Engineering, Southeast University, Nanjing 210096, China (e-mail: xiaohf@seu.edu.cn).

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2019.2962441, IEEE Transactions on Industrial Electronics

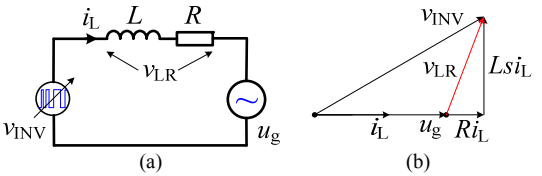


Fig. 1. Equivalent circuit and vector diagram for grid-connected VSIs. (a) Equivalent circuit. (b) Vector diagram of key variables.

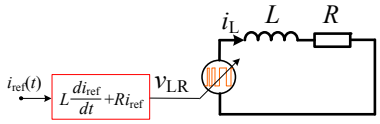


Fig. 2. Ideal current controller for grid-connected VSIs.

In order to face above challenges and develop a new kind of MPC without aforementioned disadvantages, this paper has proposed a new open-loop current controller, which combines the advantages of MPC and conventional PWM modulation. The modulation signal is calculated by simple proportional and delay algorithms while driving signals are still obtained by a conventional PWM model. As a result, this controller has advantages of fast dynamic response, fixed switching frequency, small calculation load, and high frequency noises immune.

The paper is organized as follows. Section II analyses the work principle of the new open-loop current controller. In section III, parameters design method is presented for the controller proposed in section II. Section IV discusses the influences of non-ideal factors on the proposed controller, and their compensation strategies are given as well. Stability analysis, dynamic characteristics, and control performance of proposed controller is discussed in Section V. Experimental results are presented in section V to verify the effectiveness of the proposed PPD controller. Finally, a conclusion is given in Section VI.

II. Working Principle of the New Controller

A gird-connected single-phase VSI is taken as an example to analyze the working principle of the new controller in this section. To simplify the analysis, the output voltage of inverter bridge is equivalent to be a PWM voltage source, whose pulse width is adjustable by the duty cycle of SPWM. The equivalent circuit of the single-phase VSI is plotted in Fig.1 (a), where, L is the filter inductor, R is the equivalent resister, i_L is the current through inductor L and v_{LR} is the voltage across L-R, v_{INV} is the PWM voltage of inverter bridge, u_g is the grid voltage. It is worth noting that L-R combination is the lumped inductance-resistance parameters between v_{INV} and u_g.

Fig.1 (b) shows the vector diagram of variables in Fig. 1 (a). It is shown that output voltage v_{INV} of the inverter bridge is the vector sum of v_{LR} and u_g. From perspective of control implementations, u_g can be obtained by feedforward of grid voltage. Assuming that the current flowing through L-R accurately tracks reference current i_{ref}, then voltage u_{LR} applied to L-R can be expressed in (1),

$$u_{LR} = L\frac{di_{ref}(t)}{dt} + Ri_{ref}(t) \tag{1}$$

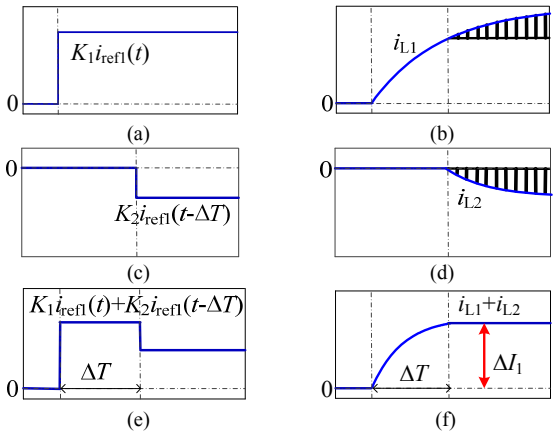


Fig.3. Step inputs and response currents. (a) Positive step input. (b) Response output of (a). (c) Negative step input. (d) Response output of (c). (e) Combined step input. (f) Response output of (e).

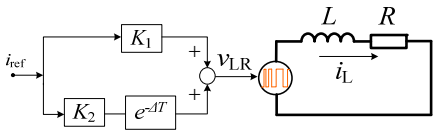


Fig.4. Structure of PPD controller.

Further, the theoretical expression of control variable v_{LR} is presented in Fig. 2 when the feedforward part counteracts grid voltage completely.

It is reasonable that control voltage u_{LR} could be calculated by an ideal differentiator and a proportional part shown in red block of Fig. 2. However, the reality is that the differentiator is not easy to fulfil in neither analog nor digital means, and is sensitive to high frequency noises [21]. Therefore, it is necessary to find a way to implement the differentiator for VSIs' controllers. An equivalent implementation method of the differentiator has been realized based on combined step responses in this paper, as shown in Fig. 3.

From Fig. 3(a), step input voltage $K_1 i_{ref1}(t)$ is applied on a L-R load with zero initial state at t=0; as a result, corresponding response current $i_{L1}(t)$ is shown in Fig. 3(b), which can be expressed in (2),

$$i_{L1}(t) = \frac{K_1 i_{ref1}(t)}{R}(1 - e^{-\frac{R}{L}t}) \tag{2}$$

Similarly, an opposite step input voltage $K_2 i_{ref1}(t\text{-}\Delta T)$ is applied on a L-R load with zero initial state at t=ΔT; the response current curve of $i_{L2}(t)$ is shown in Fig. 3(d), and can be expressed in (3),

$$i_{L2}(t) = \frac{K_2 i_{ref1}(t\text{-}\Delta T)}{R}(1 - e^{-\frac{R}{L}(t-\Delta T)}) \tag{3}$$

In Fig. 3(e), a combined step input composed of Fig. 3(a) and 3(c) is applied on the same L-R load at t=0, and t=ΔT, respectively. It is able to be expected that the response current of Fig. 3(e) reaches a constant value after instant t=ΔT if the shadow areas of Fig. 3 (b) and (d) are equal. Therefore, a setting current change ΔI_1 can be obtained by adjusting step inputs, for example, changing parameters K_1, K_2, and ΔT in Fig. 3(e) individually or together. Finally, control voltage u_{LR} of Fig. 2 can be equivalently obtained by combined step block instead, as shown in Fig. 4, if ΔI_1=$i_{ref}(K)$-$i_{ref}(K\text{-}1)$.

It can be seen from Fig. 4 that two control branches composed of proportional K_1, and proportional K_1 plus delay

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2019.2962441, IEEE Transactions on Industrial Electronics

part ΔT, respectively, are easy to be implemented based on digital control platform. Here, the abbreviation "PPD" is used to represent the new controller in incoming sections of this paper.

III. Parameter Design Rules of PPD Controller

There are three parameters, proportional factors K_1 and K_2, and delay part ΔT, needed to be set in proposed PPD controller. This section discusses these parameters' relationship from time domain and differential-integral transform perspectives, respectively.

A. Calculation Method 1 of Response Current Change ΔI_1

By reconsidering the precondition of equivalence between PPD controller and ideal differentiator discussed in Section II, i.e. the shadow areas in Fig. 3 (b) and Fig. 3 (d) are equal in time domain, a new equation can be obtained,

$$i_{L1}(t)_{t=\infty} - i_{L1}(t)_{t=\Delta T} = i_{L2}(t-\Delta T)_{t=\infty} \tag{4}$$

By substituting expressions (2) and (3) into equation (4), the relationship between K_1 and K_2 can be obtained,

$$K_2 = -K_1 e^{-\frac{R}{L}\Delta T} \tag{5}$$

Further, amplitude change ΔI_1 of current response generated by PPD controller can be expressed in (6),

$$\Delta I_1 = i_{L1}(t) + i_{L2}(t-\Delta T) = \frac{K_1 i_{ref1}(t)}{R}\left(1 - e^{-\frac{R}{L}\Delta T}\right) \tag{6}$$

It can be seen from (6) that amplitude change ΔI_1 is a constant value after ΔT, therefore, the connection of PPD controller and switching frequency is fined out if delay part ΔT is less than one switching period. In other words, one action of PPD controller has to be finished in one PWM switching period.

B. Calculation Method 2 of Response Current Change ΔI_1

This sub-section recalculates response current change ΔI_1 in second way from differential-integral transform perspective. In the first step, a differential operator is applied on the combined step input of Fig. 3 (e), as a result, a combined impulse input can be obtained, and this process is shown in Fig. 5 (a); in the second step, the same differential operator is applied on the step response current of Fig. 3 (f), a differential response is consequently obtained in Fig. 5 (b).

Because the *L*-*R* load is a linear system, the response of impulse input of Fig. 5(a) is an approximate rectangle curve of Fig. 5 (b). Therefore, the response current change ΔI_1 can be calculated from area *S* of the approximate rectangle.

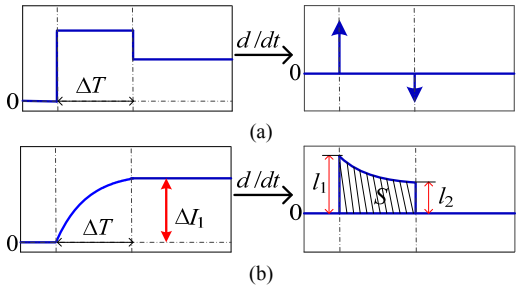


Fig. 5. Differential relationships of step voltage and response current. (a) Excitation inputs. (b) Response outputs.

There are two length parameters l_1 and l_2 in Fig. 5 (b) needed to be figure out. Referring to Fig. 3(b), l_1 represents the slope of the response current at t=0, as expressed in (7),

$$l_1 = \frac{di_{L1}(t)}{dt} = \frac{K_1 i_{ref1}(t)}{L} \tag{7}$$

Similarly, l_2 represents the slope of the response current at $t=\Delta T$ from Fig. 3 (d), as expressed in (8),

$$l_2 = \frac{di_{L2}(t)}{dt} = \frac{K_1 i_{ref1}(t)}{L} e^{-\frac{R}{L}\Delta T} \tag{8}$$

In order to simplify the calculation of area *S*, the shadow in Fig. 5(b) can be treated as a rectangle when ΔT is small enough. The width of this rectangle is ΔT, and the height can be chosen as l_1, or l_2, respectively.

1) When l_1 is chosen as the height, the response current change ΔI_1 can be expressed as

$$\Delta I_1 = S = \frac{K_1 i_{ref1}(t)}{L}\Delta T \tag{9}$$

2) When l_2 is chosen as the height, the response current change ΔI_1 can be expressed as

$$\Delta I_1 = S = \frac{K_1 i_{ref1}(t)}{L} e^{-\frac{R}{L}\Delta T}\Delta T \tag{10}$$

By setting (6) = (9), and (6) = (10) respectively, two solutions can be obtained, as shown in (11),

$$\begin{cases} K_1 = \dfrac{L}{\Delta T} \\ K_2 = -\left(\dfrac{L}{\Delta T} - R\right) \end{cases} \text{ or } \begin{cases} K_1 = \dfrac{L}{\Delta T} + R \\ K_2 = -\dfrac{L}{\Delta T} \end{cases} \tag{11}$$

Considering the fact that the impedance of equivalent resistance *R* of inverter circuits is quite small compared with the impedance of inductance *L* in quantity, the difference between the two solutions is negligible.

C. Setting Consideration of ΔT

Through the analysis in the sub-section *B*, a conclusion is that smaller ΔT is able to make l_1 and l_2 closer. In inverter design, ΔT should be determined according to the switching frequency, as discussed in Section II.

The bottom line is that PPD controller should finish one action during a switching period and fallows the restrain in formula (4). Thus, the maximum value of ΔT is the switching period T_S.

Considering the requirement of combined step input shown in Figure 3(e), the minimum value of ΔT can be close to zero but not zero. In addition, for the convenience of digital implementation, the value of ΔT can be set as $T_S/2^N$, where N is an integer. Therefore, ΔT can be chosen as follows,

$$T_S/2^N \le \Delta T \le T_S \tag{12}$$

Switching frequency is a key parameter to guide the choice of ΔT. For example, ΔT can be set at T_S when the switching frequency is higher than 10 kHz; on the contrary, ΔT can be set at $T_S/2^N$.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2019.2962441, IEEE Transactions on Industrial Electronics

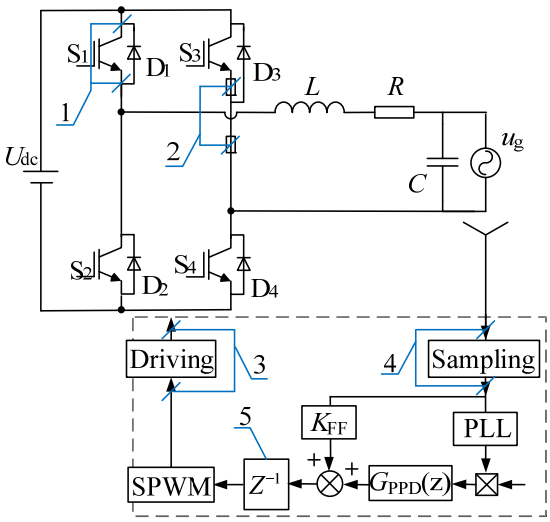


Fig. 6. Non-ideal factors in VSIs.

IV. Error Analysis and Compensation Strategies

From the principle analysis and parameters design in the former sections, it can be concluded that PPD controller is essentially a predictive open-loop controller based on the model *L*-*R*. Apart from requirements of precise inductance *L* and resistance *R*, whose effects and corresponding compensation strategies will be discussed in an incoming paper, the power stage and control unit of VSIs have to be performed in an ideal state, such as no conduction voltage drops with semiconductor devices, no delay times with sampling and PWM module in digital implementation, no driving delay and dead time. However, these non-ideal factors are unavoidable in real VSIs, this section analyzes their affects on PPD controller and presents corresponding compensation strategies.

Fig.6 shows the non-ideal factors that might occur in a VSI, Factor 1 is caused by the voltage drop of semiconductor devices; Factor 2 is related to the on-state resistance of semiconductor devices and the parasitic resistance of power circuits; Factor 3 involves driving delay and dead times. Factor 4 comes from the signal sampling circuits including conditioning and A/D conversion delay. Factor 5 includes the calculation delay and PWM delay, etc.

A. Voltage Drops of Semiconductor Devices

The forward characteristic of semiconductor devices can be equivalent by a fixed voltage U_{th} and an on-state resistance r_d [22-23]. Output voltage v_{INV} of the inverter bridge will be affected by voltage drop U_{th}, as shown in Fig. 7.

Regarding the fixed voltage drop of power switching devices,

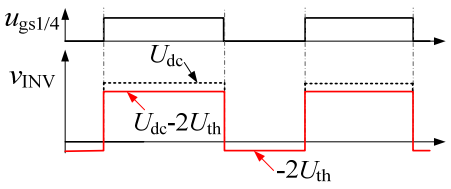


Fig. 7. Influences of U_{th} on v_{INV}.

we calculate the average value after multiple measurements at different voltage levels, and then fit the average value and voltage to obtain the mathematical expression of the fixed voltage drop.

$$U_{th} = U_0 - K_U u_{rms} \tag{13}$$

Where U_0 is an initial voltage drop, K_U is a slope rate of relationship curve obtained by data fitting, and u_{rms} is RMS value of AC voltage.

Taking a period that the inductor current is larger than zero as example, the output voltage v_{INV} of the inverter bridge is U_{dc}-$2U_{th}$ when switches S_1 and S_4 are on, where U_{dc} is the input DC voltage; the output voltage v_{INV} is $-2U_{th}$ when switches S_1 and S_4 are off, where the forward voltage drop of power diodes is assumed to be U_{th} too. Therefore, the voltage drop of semiconductor devices causes a level shift on the output voltage of the inverter bridge.

B. Parasitic Resistances

Parasitic resistances affect the output voltage amplitude of the inverter bridge in the similar manner with voltage drops of semiconductor devices. However, the parasitic resistances induced by semiconductor devices and power circuits show considerable differences at different operation conditions.

In order to face this challenge, this section proposes to find the relationship between the parasitic resistance and RMS of output current based on experimental tests with several setting operation conditions. After collecting and fitting test data, the relationship can be found as bellow,

$$r_d = R_0 - K_d I_{rms} \tag{14}$$

Where r_d is the parasitic resistance from power devices and power circuits, R_0 is an initial resistance, K_d is a slope rate of relationship curve obtained by data fitting, and I_{rms} is RMS value of output current. Similar to the voltage drop of semiconductor devices, the parasitic resistance causes a level shift on the output voltage of the inverter bridge. In summary, both of voltage drops and parasitic resistances have a negative shift on the output voltage of the inverter bridge at the positive half stage of output current, and a positive shift during the negative half period.

C. Driving Delay and Dead Time

Driving delay includes transmission delay of driving signals, turn-on and turn-off delays of semiconductor devices. Different from above two non-ideal factors, the driving delay and dead time cause influences on width of the output voltage of the inverter bridge.

Assuming that the turn-on and turn-off delays of power devices are t_{on}, and t_{off}, respectively, as well as dead time is t_d, the width reduction of output voltage v_{INV} is expressed as

$$t_{com} = t_d + t_{on} - t_{off} \tag{15}$$

The compensation signal of modulation waveform can be obtained by further transform calculation between compensation voltage and delay time with switching frequency restriction, as expressed in (16),

$$u_{com} = U_{dc} \frac{t_{com}}{T_s} \tag{16}$$

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2019.2962441, IEEE Transactions on Industrial Electronics

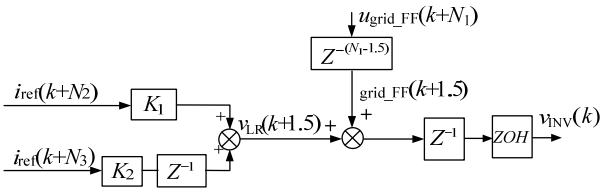


Fig. 8. Inverter control block with PPD controller.

Where, T_S is the switching period.

Taking the aforementioned factors including voltage drops, parasitic resistances and delay times into consideration, the modulation waveform compensated is expressed in (17),

$$u_{ref\_F}=\begin{cases}u_{ref}+2U_{th}+2r_dI_{rms}+u_{com} & i_{ref}>0\\ u_{ref}-2U_{th}-2r_dI_{rms}-u_{com} & i_{ref}<0\end{cases} \tag{17}$$

Where u_{ref} is the modulation voltage calculated by PPD controller and u_{ref_F} is the modulation voltage after compensating non-ideal factors.

D. Feed-Forward Delay of Grid Voltage

The main factors that affect the performance of grid-voltage feed-forward compensation include sampling, calculation, and update parts, as shown in Fig. 8.

Delay times of conditioning and sampling circuits can be set to be integer or fractional times of the switching period by adjusting hardware parameters and setting registers of the A/D module. There are delays in the calculation and update of modulation waveform based on DSP, i.e., the modulation waveform loaded into the PWM module comparator register in the k th switching period is calculated during the k-1 th switching period. The analysis of this process reveals that it behaves as a zero-order holder and can be equivalent to pure time-delay [24].

Obviously, the delays discussed above deteriorate the performance of grid-voltage feed-forward compensation. In order to eliminate this influence, a mature and simple prediction algorithm has been employed, its formula is expressed in (18)

$$\begin{aligned}u_{grid\_FF}(k+N_1)=&\,u_{grid\_FF}(k)+\\ &N_{1\_1}(u_{grid\_FF}(k)-u_{grid\_FF}(k-1))+\\ &N_{1\_2}(u_{grid\_FF}(k-1)-u_{grid\_FF}(k-2))\end{aligned} \tag{18}$$

Where N_1 is the number of total switching periods during the delay of grid-voltage feed-forward, N_{1_1} and N_{1_2} comply with the restriction of $N_1=N_{1\_1}+N_{1\_2}$, $u_{grid\_FF}(k)$ is the sampling value at sampling instant kTs, $u_{grid\_FF}(k\text{-}1)$ is the sampling value at sampling moment $(k\text{-}1)T$s, and $u_{grid\_FF}(k\text{-}2)$ is the sampling value at sampling moment $(k\text{-}2)T$s, respectively, $u_{grid\_FF}(k+N_1)$ is the predicted value of grid-voltage feed-forward with N_1 switching periods in advance.

E. Control Delay of PPD Controller

Loop delay of PPD controller is mainly caused by factors of calculation, updating and loading, and PWM Module, as shown in Fig. 8. The loop delay of the PPD controller can be eliminated by using reference signals with several switching periods ahead.

The structure of the PPD controller is shown in Fig. 4, and redrawn in Fig. 8 in discrete domain. The number of switching periods predicted by the reference current of K_1 branch is N_2. According to the structure, N_2 equals to the number of delayed switching periods caused by calculation, updating and loading, and PWM module. Therefore, the reference current can be predicted by employing the following method:

$$i_{ref}(k+N_2)=[i_{ref}(k+N_{2\_1})+i_{ref}(k+N_{2\_2})]/2 \tag{19}$$

Where $N_{2\_1}+N_{2\_2}=2N_2$, $i_{ref}(k+N_{2\_1})$ is the reference current with N_{2_1} switching periods ahead, and $i_{ref}(k+N_{2\_2})$ is the reference current with N_{2_2} switching periods in advance.

The number of switching periods used to compensate for K_2 branch is N_3. The number N_3 of delayed switching periods is calculated by accumulating calculation, updating and loading and PWM Module links, and minus the number of switching periods set for the delay part of PPD controller. Therefore, the reference current can be predicted by employing the following method:

$$i_{ref}(k+N_3)=[i_{ref}(k+N_{3\_1})+i_{ref}(k+N_{3\_2})]/2 \tag{20}$$

Where $N_3=N_2\text{-}1/2^N$, $N_{3\_1}+N_{3\_2}=2N_3$, $i_{ref}(k+N_{3\_1})$ is the reference current with N_{3_1} switching periods ahead, and $i_{ref}(k+N_{3\_2})$ is the reference current with N_{3_2} switching periods in advance.

V. Stability Analysis and Dynamic Characteristics

A. Stability analysis of PPD control

PPD control is a type of MPC and also a type of open loop control. In the actual system, there are delays in hardware conditioning circuit and digital control, as shown in Fig. 9, which should be taken into account when analyzing the stability of the system.

In Fig. 9, G_{d2} represents the delay caused by hardware sampling circuit; G_{d1} is the delay of control signal caused by calculation and update; G_Z represents the delay of control signal caused by PWM modulation. Grid-in current $I_g(s)$ can be expressed as:

$$\begin{aligned}I_g(s)=&\frac{I_{ref}(s)G_{ppd}G_{d1}G_Z}{Ls+r}+\frac{U_g(s)(G_{d2}G_{d1}G_Z-1)}{Ls+r}\\ =&I_{11}(s)+I_{12}(s)\end{aligned} \tag{21}$$

It can be seen that the grid-in current includes two parts: response current i_{11} from PPD controller applied on the filter inductor, and disturbance current i_{12} generated by grid voltage due to feedforward delay.

Here, stability of $I_{11}(s)$ is analyzed. When the delay of K_2 branch of PPD controller is 1Ts, the delay of sampling calculation, updating, loading is 1Ts, and the delay of PWM modulation is 0.5Ts, the transfer function of i_{11} for the inverter

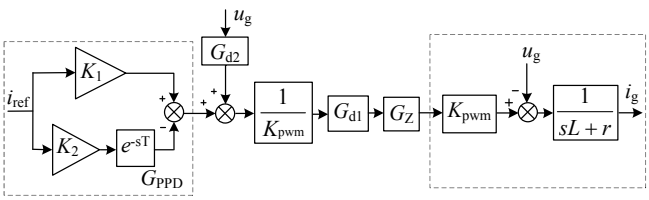


Fig. 9. Inverter system block diagram with delays.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2019.2962441, IEEE Transactions on Industrial Electronics

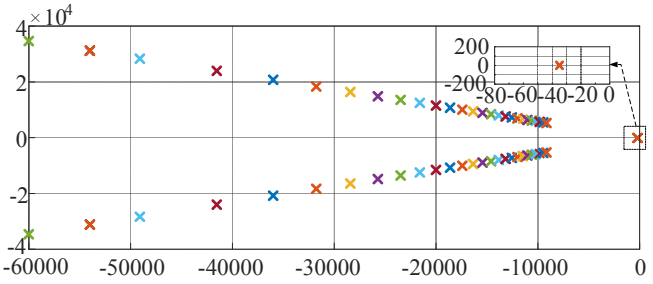


Fig. 10. Poles' traces of current transfer function with different digital control delays.

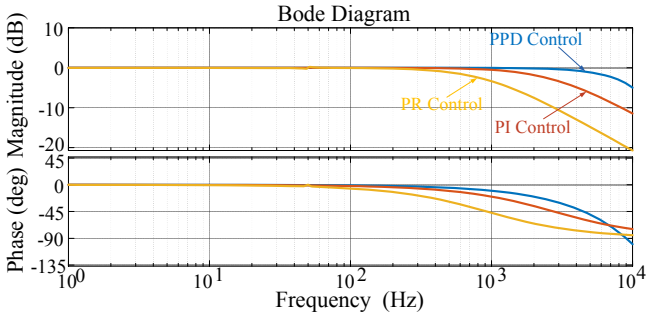


Fig. 11. Bode diagrams of grid-in current transfer functions with different controllers.

voltage u_{inv} can be obtained:

$$I_{11}(s)=\frac{(K_1-K_2e^{-sT})e^{-1.5sT}}{sL+r} \tag{22}$$

In low-frequency range, the pure delay part can be equivalent as an inertia unit. Therefore, e^{-sT} and $e^{-1.5sT}$ can be approximately replaced by the following inertia units:

$$e^{-sT}\approx\frac{1}{Ts+1} \tag{23}$$

$$e^{-1.5sT}\approx\frac{1}{1.5Ts+1} \tag{24}$$

By substituting equations (23) and (24) into equation (22), it can be obtained:

$$I_{11}(s)=\frac{K_1Ts+K_1-K_2}{(Ls+r)(1.5Ts+1)(Ts+1)} \tag{25}$$

It can be seen from equation (25) that the poles of the open-loop transfer function are all located in the left half plane of the s-plane. Fig. 10 shows poles' trace of transfer function I_{11}(s) with different digital control delays from 0 to 6 Ts, and

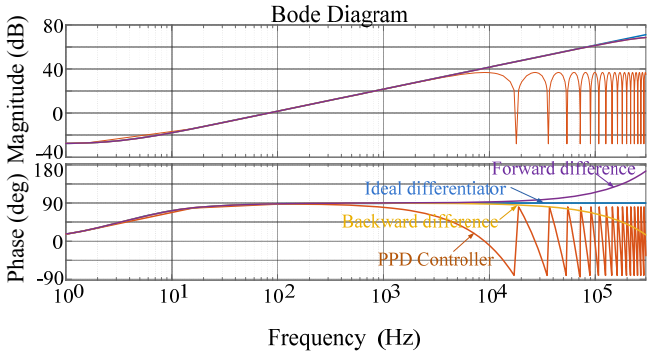


Fig. 12. Bode diagrams of ideal differential controller, PPD controller, forward differential controller and backward differential controller.

0.2Ts interval. Therefore, transfer function I_{11}(s) is stable.

Since disturbance current transfer function I_{12}(s) generated by feedforward delay of grid voltage, it is negligible. The reason is that the feedforward delay can be offset by expression (18).

B. Dynamic characteristics of PPD control

Since PPD control belongs to MPC, it has the advantages of fast dynamic performance compared with traditional PI and PR control.

Considering that the delay parts of inverter system can be compensated effectively, transfer functions of grid-in current related to the reference current with PPD controller, PI controller and PR controller are obtained, respectively.

$$G_{PPD}(s)=\frac{K_1+K_2e^{-sT}}{sL+R} \tag{26}$$

$$G_{pi}(s)=\frac{(K_p+\frac{K_i}{s})\frac{1}{sL+R}}{1+(K_p+\frac{K_i}{s})\frac{1}{sL+R}} \tag{27}$$

$$G_{PR}(s)=\frac{(K_{PR}+\frac{K_{PRi}s}{s^2+\omega^2})\frac{1}{sL+R}}{1+(K_{PR}+\frac{K_{PRi}s}{s^2+\omega^2})\frac{1}{sL+R}} \tag{28}$$

Bode diagrams of these transfer functions are shown in Fig. 11. It can be seen that PPD controller has wider bandwidth, which indicates that the dynamic characteristic of PPD controller is faster than PI controller and PR controller.

C. Control performance of PPD controller

The main purpose of proposed PPD controller is to implement the ideal differential controller in practice. Because the ideal differential controller is sensitive to high frequency noise, it is rarely used directly in practical systems. Therefore, digital differential controllers realized by forward Euler and backward Euler have been proposed in control area.

Fig. 12 shows Bode diagrams of ideal differential controller, PPD controller, forward differential controller and backward differential controller. It can be seen that in vicinity of the fundamental frequency, their amplitude gains and phase angle gains are consistent. However, as the frequency increases into higher span, the amplitude gain of PPD controller no longer increases, it is very important to suppress high frequency noise. Therefore, PPD controller is less sensitive to high frequency

Fig. 13. Experimental platform.

noise.

VI. Experiment Results and Discussion

In order to verify the effectiveness of the proposed PPD controller and compensation strategy, A 3 kW grid-connected inverter prototype has been built in our laboratory and extensively experimental tests have been performed. A DSP with model number TMS320F28035DSP from TI has been used as main controller chip, and IGBTs with model number FGA40N65SMD have been selected as the power switches for the prototype. The experimental platform is shown in Fig. 13 and the specific parameters are shown in Table 1.

TABLE I
Main Parameters of 3 kW Prototype

Parameters	Value
Rated power P_N	3 kW
DC bus voltage U_{dc}	360 V
Inductance L	1.92 mH
Resistance R	50 mΩ
Capacitance C	4.7 μF
Power grid u_g	220 V/50 Hz
Switching frequency f_S	18 kHz
K_1	34.61
K_2	-34.56
ΔT	55.56μs
Formula (13), U_0/K_U	0.6479/0.0004
Formula (14), R_0/K_d	0.3971/ 0.0192
Formula (15), $t_d/t_{on}/t_{off}$	1.52us/0.06us/ 0.24us
Formula (18), N_{1_1}/N_{1_2}	1.8/1.7.
Formula (19), N_{2_1}/N_{2_2}	2/1
Formula (20), N_{3_1}/N_{3_2}	1/0

A. Steady State Performance Verification

Fig. 14 shows the steady-state waveforms of the grid-connected inverter at unit power factor including grid voltage u_g, reference current i_{ref} and grid-in current i_g. It is worth mentioning that the figure is drawn by importing experimental data into MATLAB, in doing so, the grid-in current is easy to be compared with its given reference. It can be seen from Fig. 14 that PPD controller is able to track the reference current accurately.

Fig. 15 shows the steady-state waveforms at non-unit power factor. Fig. 15 (a) shows the condition that the reference current leads the grid voltage with 90 degrees. Fig. 15 (b) shows the condition that the reference current lags the grid voltage with 90 degrees, respectively. It can be concluded that proposed PPD controller is able to track a reference current accurately with any power factor.

B. Dynamic Performance Verification

Fig. 16 and 17 show the dynamic waveforms of the PPD controller with differently sudden changes. Fig. 16(a) shows the waveforms of the inverter when the reference current drops suddenly at the peak, and Fig. 16(b) shows the waveforms of the inverter when the reference current rises suddenly at the peak, respectively. These figures show that PPD controller is able to track reference current quickly regardless of the sudden increase or decrease. The experiment results indicate that proposed PPD controller has a good dynamic performance.

Fig. 17(a) shows the waveforms of the inverter when the grid voltage drops suddenly at the peak, and Fig. 17(b) shows the waveforms of the inverter when the grid voltage restores suddenly at the peak, respectively. These figures show that the PPD controller is able to keep stable regardless of the sudden decrease or increase of grid voltage. Therefore, the experiment results prove that PPD controller has the fault ride-through capability.

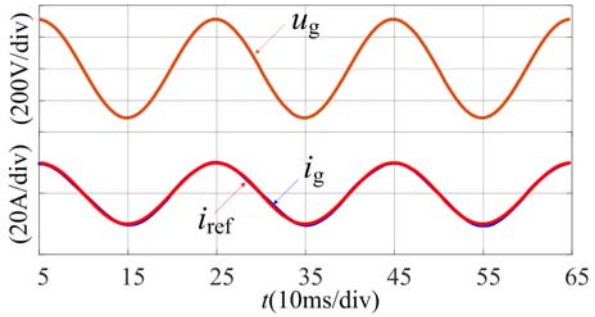
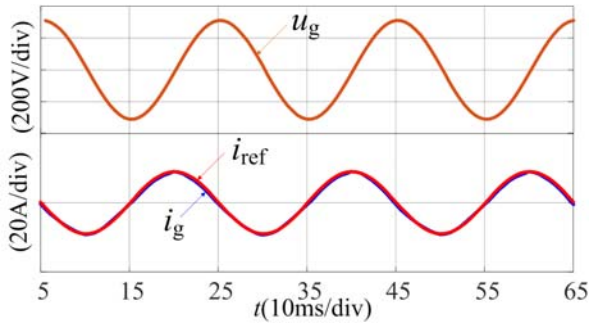
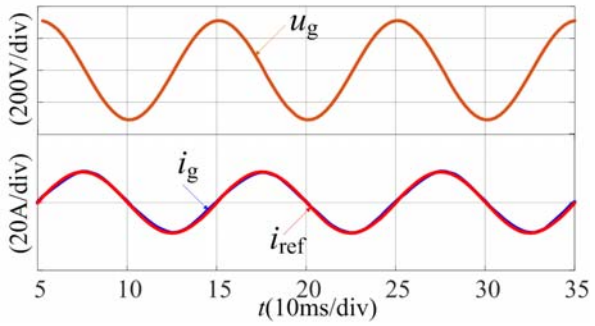


Fig. 14. Steady state waveforms with unit power factor.



(a)



(b)

Fig. 15. Steady state waveforms with non-unit power factors. (a) 90° leading. (b) 90° lagging.

Fig. 18 shows the waveforms of grid-in current PI controller, PR controller, and PPD controller when the reference current drops suddenly at the peak. It can be seen that PPD control has the faster dynamic response speed, and the results are in consistent with theoretical analysis results of Fig. 11.

C. Verification of Compensation Strategies for Non-ideal Factors

Fig. 19(a) shows the steady state waveforms of grid-in current without the compensation strategies, and Fig. 19(b) shows the waveforms of grid-in current with the compensation strategies, respectively. By comparing two groups of waveforms, it can be seen that the grid-in current distortion is significantly reduced and the steady-state error is close to zero after the proposed compensation strategies are enabled.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2019.2962441, IEEE Transactions on Industrial Electronics

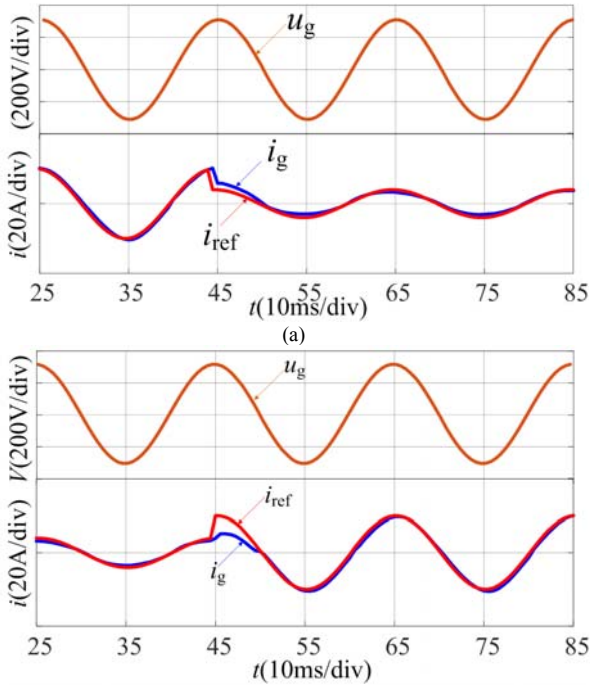


Fig. 16. Dynamic performance with current reference changes. (a) Step down. (b) Step up.

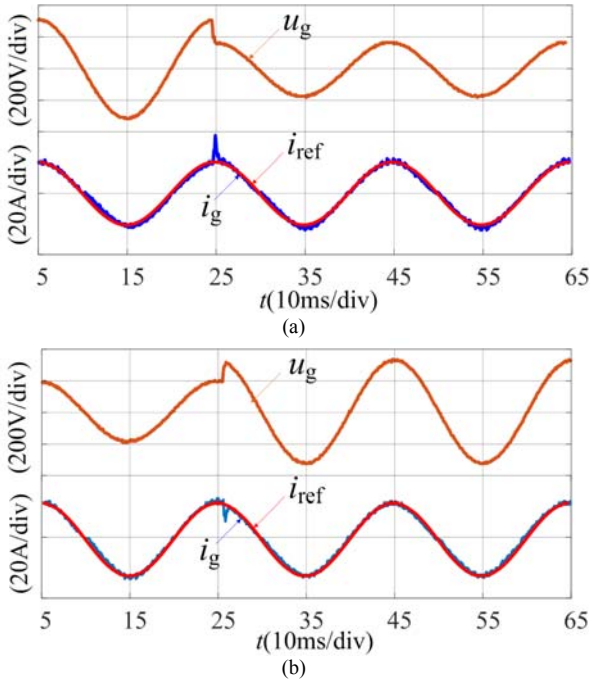


Fig. 17. Dynamic performance with grid voltage changes. (a) Step down. (b) Step up.

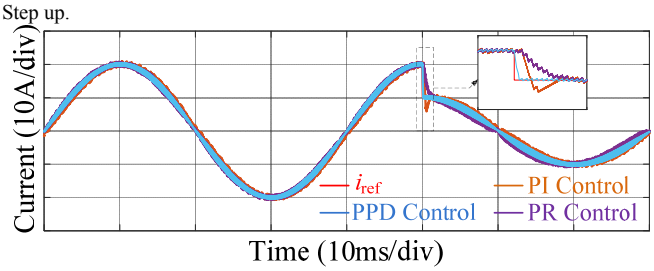


Fig. 18. Dynamic performance comparison with different controllers.

Fig. 20(a) shows the dynamic grid current response with the current reference changed suddenly when the compensation strategies are disabled, and Fig. 20(b) shows the dynamic grid current response under the same condition when the compensation strategies are enabled, respectively. It can be seen that the influence of non-ideal factors on the dynamic performance of PPD control is not obvious. However, the static performance, such as THD and tracking error, are significantly different.

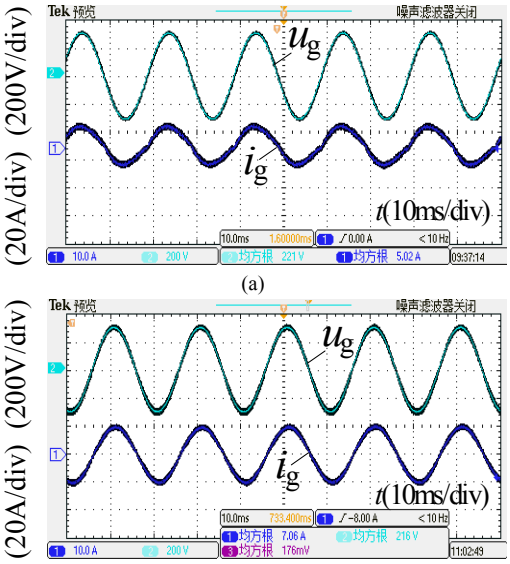


Fig. 19. Steady state performance of the compensation strategies. (a) Without compensation strategies. (b) With compensation strategies.

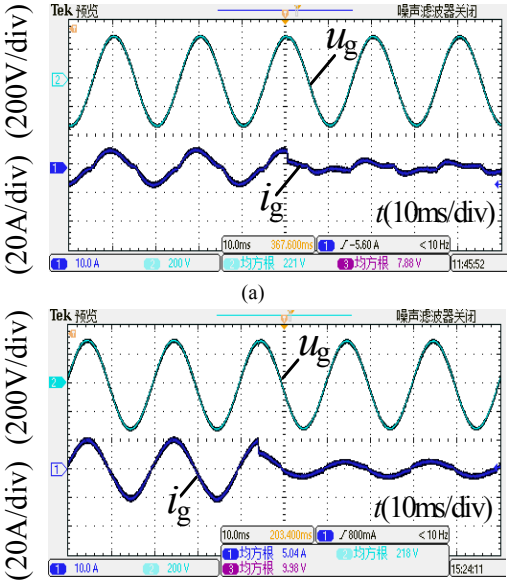


Fig. 20. Dynamic performance of the compensation strategies. (a) Without compensation strategies. (b) With compensation strategies.

Table 2 lists the current amplitude and phase angle deviations with and without the proposed compensation strategies at different current ratings. It can be seen that the static performance has been significantly improved by using the proposed compensation strategies in whole power range.

TABLE II

DEVIATIONS OF GRID CURRENT TRACKING WITH AND WITHOUT PROPOSED COMPENSATION STRATEGIES

Current	Amplitude Error		Phase Error	
Reference	Without	With	Without	With
1A	35%	12%	4.1°	0.31°
5A	16%	2.6%	4.4°	0.32°
9A	10%	1.2%	3.3°	0.30°
13A	5.8%	0.5%	2.7°	0.33°

Ⅶ CONCLUSION

This paper has proposed a new method to realize differential controller that troubled power electronics control for long time. The structure of the new controller abbreviated as PPD has been derived from step combination excitations, and parameters design method of the new controller has been discussed in detail in this paper. Non-ideal factors have been thoughtful investigated and the corresponding compensation strategies are presented. The main conclusions are summarized as below.

1) Proposed PPD controller is simple in parameters design and does not need parameter debugging process by observing response performances.

2) Switching frequency of PPD control is constant. The modulating waveform of PPD control is calculated by the proportional and delay algorithms, and gate driving signals are obtained by a conventional PWM comparator.

3) Proposed PPD controller is able to suppress high frequency noise compared with ideal differential controller, forward differential controller and backward differential controller.

4) After designing the precise compensation strategies for non-ideal factors, proposed PPD controller is able to track a current reference with full power factor and zero static error. Moreover, PPD controller has fast dynamic response and strong grid fault ride through capability.

ACKNOWLEDGEMENT

The authors would like to thank Prof. Boon-Teck Ooi, McGill University, for his help during the principle analysis of the PPD controller.

REFERENCES

[1] W. Li, Y. Gu, H. Luo, W. Cui, X. He, and C. Xia, "Topology review and derivation methodology of single-phase transformerless photovoltaic inverters for leakage current suppression," *IEEE Trans. Ind. Electron.*, vol. 62, no. 7, pp. 4537-4551, July, 2015.

[2] Jofre M, Llor A M, Silva C A. " Sensorless Low Switching Frequency Explicit Model Predictive Control of Induction Machines fed by Neutral Point Clamped Inverter, " *IEEE Trans. Ind. Electron.*, vol. 66, no. 12, pp. 9122-9128, Dec, 2019.

[3] Li G, Hu J, Li Y, et al. , "An Improved Model Predictive Direct Torque Control Strategy for Reducing Harmonic Currents and Torque Ripples of Five-Phase Permanent Magnet Synchronous Motors," *IEEE Trans. Ind. Electron.,* vol. 66, no. 8, pp. 5820-5829, Aug, 2019.

[4] Shuai Z, Huang W, Shen C, et al, " Characteristics and restraining method of fast transient inrush fault currents in synchronverters," *IEEE Trans. Ind. Electron.*, vol. 64, no. 9, pp. 7487-7497,Sep, 2017..

[5] Mohamed YARI，El-Saadany E F, "An improved deadbeat current control scheme with a novel adaptive self-tuning load model for a three-phase PWM voltage-source inverter, " *IEEE Trans. on Ind. Electron.*, vol. 54, no. 2, pp. 749-759, Feb. 2007.

[6] X. Zhang, Y. Wang, C. Yu, et al., "Hysteresis model predictive control for high-power grid-connected inverters with output LCL filter, " *IEEE Trans. on Ind. Electron.*, vol. 63, no. 1, pp. 246-256, Jan. 2016.

[7] C. Bao, X. Ruan, X. Wang, et al., "Design of grid-connected inverters with LCL filter based on PI regulator and capacitor current feedback active damping, " *Proceedings of the CSEE*, vol. 32, no. 25, pp. 133-142, July 2012.

[8] D. N. Zmood, D. G. Holmes, and G. H. Bode, "Frequency-domain analysis of three-phase linear current regulators," *IEEE Trans. on Ind. Appl.*, Vol. 37, no. 2, pp. 601-610, Mar./Apr. 2001.

[9] L. Harnefors, A G Yepes, A. Vidal, et al., "Passivity-based controller design of grid-connected VSCs for prevention of electrical resonance instability," *IEEE Trans. on Ind. Electron.*, vol. 62, no. 2, pp. 702-710, Feb. 2015

[10] D. Chen, J. Zhang, Z. Qian, "An improved repetitive control scheme for grid-connected inverter with frequency-adaptive capability," *IEEE Trans. on Ind. Electron.*, vol. 60, no. 2, pp. 814-823, Feb. 2013.

[11] X. Zhang, Y. Wang, C. Yu, et al., "Mechanism of the control coupling and suppression strategy using PI and repetitive control in grid-connected inverters," *Proceedings of the CSEE*, vol. 34, no. 30, pp. 5287-5295, Oct. 2014.

[12] Z. Zou, K. Zhou, Z, Wang, et al., "Frequency adaptive fractional-order repetitive control of shunt active power filters," *IEEE Trans. on Ind. Electron.*, vol. 62, no. 3, pp. 1659-1668, Mar. 2015

[13] X. Cao, G. Tan, C. Wang, et al., "A research on low switching frequency PWM rectifiers with satisfactory and model predictive control," *Proceedings of the CSEE*, vol. 33, no. 27, pp. 69-77, Sep. 2013.

[14] Vazquez S, Rodriguez J, Rivera M, et al, "Model predictive control for power converters and drives: Advances and trends," *IEEE Trans. Ind. Electron.*, vol. 64, no. 2 pp. 935-947, Feb. 2017.

[15] Young H A, Perez M A, Rodriguez J, "Analysis of finite-control-set model predictive current control with model parameter mismatch in a three-phase inverter," *IEEE Trans. Ind. Electron.*, vol. 63, no. 5 pp. 3100-3107, May. 2016.

[16] Kou P, Liang D, Linbo Y, et al., " Nonlinear model predictive control of wind farm for system frequency support," *IEEE Trans.on Power Systems*, vol. 34, no. 5 pp. 3547-3561, Sep. 2019.

[17] Gontijo G F, Tricarico T C, Franca B W, et al., " Robust model predictive rotor current control of a DFIG connected to a distorted and unbalanced grid driven by a direct matrix converter," *IEEE Trans. on Sustainable Energy*, vol. 10, no. 3 pp. 1380-1392, Jul. 2018.

[18] Mohapatra S R, Agarwal V, "Model predictive controller with reduced complexity for grid tied multilevel inverters, " *IEEE Trans. on Ind. Applications*, Vol. 66, no. 11, pp. 8851-8855, Nov.2018.

[19] Guzman R, de Vicuña L G, Camacho A, "Receding-horizon model-predictive control for a three-phase VSI with an LCL filter, " *IEEE Trans. on Ind. Appl.*, vol. 66, no. 9, pp. 6671-6680, Sep. 2019.

[20] Zhang X, Tan L, Xian J, "Direct grid-side current model predictive control for grid-connected inverter with LCL filter, " *IET Power Electron.*, vol. 11, no. 15, pp. 2450-2460, Dec. 2018.

[21] V. Blasko, V. Kaura, "A novel control to actively damp resonance in input LC filter of a three-phase voltage source converter," *IEEE Trans. on Ind. Appl.*, Vol. 33, no. 2, pp. 542-550, Mar./Apr. 1999.

[22] J. W. Choi, S. K. Sul, "Inverter output voltage synthesis using novel dead time compensation," *IEEE Trans. on Power Electron.*, Vol. 11, no. 2, pp. 221-227, Mar. 1996.

[23] S. Chen, Z. Xue, "The analysis and compensation of output Error for voltage source PWM inverter," *Transactions of China Electrotechnical Society*, vol. 16, no. 2, pp. 51-55, Feb. 2001.

[24] D. Yang, X. Ruan, H Wu, "A real-time computation method with dual sampling mode to improve the current control performance of the LCL-type grid-connected inverter," *IEEE Trans. on Ind. Electron.*, vol. 62, no. 7, pp. 4563-4572, Mar. 2015.

Hua F. Xiao (S'10–M'13-SM'17) was born in Hubei Province, China. He received the B.S., M. S. and Ph.D. degrees in electrical engineering from Nanjing University of Aeronautics and Astronautics (NUAA), Nanjing, China, in 2004, 2007 and 2010, respectively.

He joined the Faculty of power electronics in 2011, and is currently a Professor at the College of Electrical Engineering, Southeast University (SEU), Nanjing, China. From 2015 to 2016, he was a Postdoctoral Fellow with the Department

of Electrical and Computer Engineering, Ryerson University, Toronto, ON, Canada. From Aug. 2016 to 2017, he was a Postdoctoral Fellow with the Department of Electrical and Computer Engineering, McGill University, Montreal, QC, Canada.

Dr. Xiao's research interests include high frequency soft-switching conversions, photovoltaic power systems, and applications of power electronic technology in power system. Dr. Xiao has authored more over 80 technical papers in Journals and Conference proceedings, and held 32 china patents.

Mingming Li was born in Jiangsu, China, in 1989. He received the B.S. degree in 2013 from Hohai University, and is currently working towards the Ph.D. degree in electrical engineering in Southeast University, Nanjing, China.

His current research interest includes grid-connected inverters' control

Liliang Wu was born in JIangsu，China，in 1994. He received the B.S. degree in 2017 from Hohai University, and is currently working towards the M.S. degree in electrical engineering in Southeast University, Nanjing, China.

His current research interest includes gate driving and short-circuit protection of SiC power MOSFETs.

Ming Cheng (M'01–SM'02–F'15) received the B.Sc. and M.Sc. degrees from the Department of Electrical Engineering, Southeast University, Nanjing, China, in 1982 and 1987, respectively, and the Ph.D. degree from the Department of Electrical and Electronic Engineering, The University of Hong Kong, Hong Kong, in 2001, all in Electrical Engineering.

Since 1987, he has been with Southeast University, where he is currently a Chair Professor in the School of Electrical Engineering and the Director of the Research Center for Wind Power Generation. From January to April 2011, he was a Visiting Professor with the Wisconsin Electric Machine and Power Electronics Consortium, University of Wisconsin, Madison. His teaching and research interests include electrical machines, motor drives for electric vehicles, and renewable energy generation. He has authored or coauthored over 360 technical papers and 4 books and is the holder of 100 patents in these areas.

Prof. Cheng is a fellow of the Institution of Engineering and Technology. He has served as chair and organizing committee member for many international conferences. He is a Distinguished Lecturer of the IEEE Industry Applications Society (IAS) in 2015/2016.