Elimination of Circulating Current in a Parallel PWM Rectifier using an Interface Circuit

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***Abstract*- Parallel pulse width modulation rectifiers (PPWMR) are a good solution for high-power AC-DC applications which enhance quality and reliability. However, the main and inevitable shortcoming of parallel structures is a generation of circulating current. Various methods are proposed to reduce or eliminate circulating current, most of which tend to change or limit the switching pattern of parallel converters. This paper presents an interfacing circuit with low rating elements which eliminates the circulating current without any limitation for the switching pattern of parallel converters. Therefore, voltage and current waveforms are in high quality. Moreover, unlike previous methods that had complex control and high mathematical computations, the presented method has simple control. Therefore, Multiple modules can be implemented in a modular fashion with a fast dynamic response. Simulation and Laboratory results are presented to validate the analysis.**

***Index Terms*— Parallel PWM rectifiers, circulating current, interfacing circuit, switching pattern, modular**

I. I. INTRODUCTION

The use of parallel PWM rectifiers (PPWMR) is essential in a wide range of applications in electrical industry such as renewable energy systems and motor drives [1, 2]. High power conversion, higher reliability, enhanced power quality, improved current and voltage waveforms are among the benefits of parallel structure. The main problem with the application of such structures is the inevitable creation of circulating current, which will damage semiconductor devices, increase losses, cause distortion in current and voltage waveforms, reduce efficiency and reliability of the system [3, 4]. Circulating currents are categorized as high and low frequency components [1, 5] which are due to different switching states of parallel rectifiers and different control system of converters respectively. Also, different design components and unbalanced voltages are of concern in low frequency circulating currents.

Low frequency circulating currents are normally reduced using a droop control strategy [6] and also PI controllers which are dependent on circuit performance in different states. Among these strategies are PI controller with feed forward controller [7], deadbeat control method [8], using a PIR with feed forward term which requires information of switching vectors in each period [9], improved D-∑ digital method [10], finite-time controller and zero-vector feed forward control method [5]. [11-14] introduces a strategy based on an average model. [15] investigated elimination of circulating current due to third harmonic order.

Main solutions for high frequency circulating current reductions are mainly classified in three main categories: Filters, PWM strategies and topology reconfiguration. Each of which has its advantages and disadvantages. Coupled inductor (CI) [16-18], common mode inductor (CMI)[19], inter-phase inductor [20] and modified LCL (MLCL) [6] are the main structures in the category of filter-based techniques. Mainly, they have issues regarding size, cost and losses. However, according to [3, 6], MLCL leads to internal common mode resonance current and external zero-sequence resonance circulating current.

Among PWM-based strategies, synchronization of the switching states (or carriers) of multiple converters along with a selection of the same design parameters for each converter (inductors, power sharing and power factor) are the main solutions of circulating current elimination [21, 22]. However, in case of any delay or mismatch between converters[6], solutions have to be considered. Other PWM strategies for circulating current reduction are selective harmonic elimination PWM [23], dual-carrier space-vector PWM (SVPWM) [24], three-level space vector modulation[25], active zero state PWM [26] and hybrid PWM [27].

Interleaved PWM is also used to improve current and voltage quality and reduce common mode voltage in PPWMRs[28, 29]. This leads to a drastic increment of circulating current. Many techniques are introduced such as two-degree of freedom interleaved scheme [28] , interleaving discontinuous PWM [29] and interleaved POD scheme[30]. filters are utilized in interleaved converters which also adds cost and size [31].

Reduction of circulating current and increasing the quality at the same time are somehow contradictory and causes a lack of degree of freedom in the selection of switching states. Therefore, multilevel inverters [7, 32-34] are introduced in order to eliminate circulating currents using a high number of switching states. It gives the opportunity to work on both circulating current elimination and other performance factors of the converter at the same time. Such topologies still have complex control strategies in both module and system levels.

The main focus of this paper is on the topology reconfiguration without requiring complex control strategies.

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This technique gets rid of interfering in the switching pattern of converters. Therefore, an interface circuit is added to the circuit in order to disconnect the circulating current path without any limitations for converters' switching strategy.

Section II discusses circulating current in PPWMRs based on different conditions on switching strategies, power sharing, and inductors values of the converters. The proposed structure to eliminate the circulating current is introduced in section III. Simulation and practical results are presented in section IV to validate the performance accuracy of the proposed structure. Finally, the conclusion is brought in section V.

II. CIRCULATING CURRENT

Given the possible conditions for switching state, circulating current can be determined as follows. Note that only leg A is considered for the simplicity of the analysis. Other legs can be analyzed in the same way. Circulating current is considered for two cases of the same and different switching states for the mentioned leg. In each case, the calculation shows the important factors and their impacts on the circulating current.

A. In same switching state

Fig.1 shows two three-phase PPWMRs rectifiers. The same switching states are considered for switching of leg A (both lower switches are on). Circulating the current path is shown where there is not any DC link capacitor in the path. V_A, V_B and V_C are the phase voltages. L_{1A} and L_{2A} are the inductance of converter at phase A. C_{11} and C_{12} (C_{21}, C_{22}) are the DC link capacitors of the upper (lower) converter with the midpoint of O_1 (O_2). Note that O_1 and O_2 are considered to be the same voltage as O.

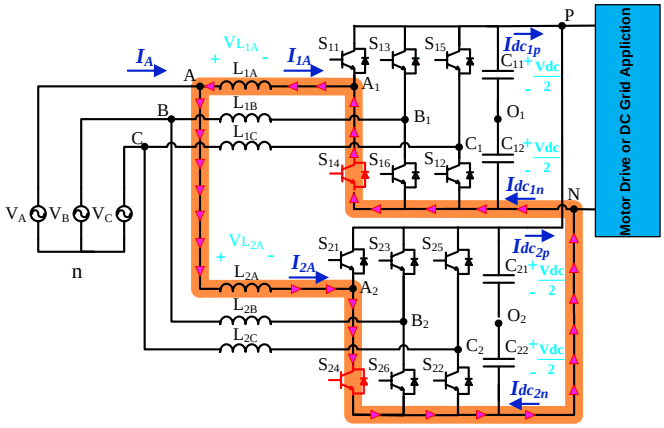


Fig. 1: Circulating current path in same switching state and of leg A

Circulating current is defined as the difference of phases' currents at AC side, which is written as:

$$I_{CC_A}=\frac{\frac{I_{2A}}{K}-I_{1A}}{2} \tag{1}$$

I_{A1} and I_{A2} are phase A currents of the upper and lower converters, respectively. K is the ratio of the power of two converters ($P_2=KP_1$). Inductors may have slight differences ($L_{2A}=hL_{1A}$). As shown in this figure, inductor voltages (when the lower switch is turned on) can be written as:

$$V_{L_{1A}}=V_{L_{2A}}=V_A+\frac{V_{dc}}{2}-V_{On} \tag{2}$$

Where V_{On} is the common mode voltage. From (2) and assuming $V_A=V_m sinwt$, one can have the following equations in a switching state interval of (t_{n-1}, t_n) as:

$$\int_{i_1(t_{n-1})}^{i_1(t_n)} di_{1A}(t)=\int_{t_{n-1}}^{t_n}\frac{1}{L_1}(V_m\sin wt+\frac{V_{dc}}{2}-V_{On})dt \tag{3}$$

$$\int_{i_2(t_{n-1})}^{i_2(t_n)} di_{2A}(t)=\int_{t_{n-1}}^{t_n}\frac{1}{L_2}(V_m\sin wt+\frac{V_{dc}}{2}-V_{On})dt \tag{4}$$

I_{1A} and I_{2A} can be calculated from (3-4) and substituted in (1) to achieve the circulating current of leg A at t_n.

$$I_{CC_A}(t_n)=(\frac{1-Kh}{2Kh})\times\left(\frac{V_m}{\omega L_{1A}}(\cos\omega t_{n-1}-\cos\omega t_n)+(\frac{V_{dc}}{2}-V_{On})\frac{t_n-t_{n-1}}{L_{1A}}\right)+\frac{I_{2A(t_{n-1})}-KI_{1A(t_{n-1})}}{2K} \tag{5}$$

B. In different switching state

As shown in Fig.2, different switching states are considered for leg A of both converters. This is a critical condition for the creation of circulating current (with depicted paths where the DC link capacitor is involved in the path). Inductors' voltages are:

$$V_{L_{1A}}(t)=L_{1A}\frac{di_{1A}(t)}{dt}=V_A-\frac{V_{dc}}{2}-V_{On} \tag{6}$$

$$V_{L_{2A}}(t)=L_{2A}\frac{di_{2A}(t)}{dt}=V_A+\frac{V_{dc}}{2}-V_{On} \tag{7}$$

With the same procedure of (3-5), the circulating current of leg A can be calculated as:

$$I_{CC_A}(t_n)=\left(\frac{V_m}{\omega L_{1A}}(\cos\omega t_{n-1}-\cos\omega t_n)+V_{On}\frac{t_n-t_{n-1}}{L_{1A}}\right)(\frac{1-Kh}{2Kh})+\frac{V_{dc}}{2}(\frac{1+Kh}{Kh})\frac{t_n-t_{n-1}}{2L_{1A}}+\frac{I_{2A(t_{n-1})}-KI_{1A(t_{n-1})}}{2K} \tag{8}$$

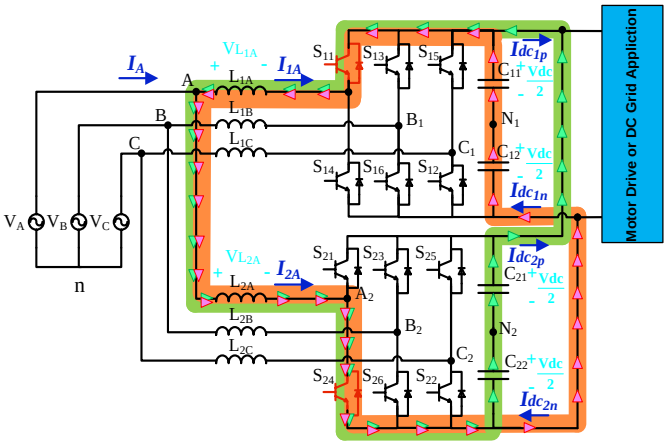


Fig. 2: Circulating current path for different switching state of Leg A

The following facts can be concluded from the calculations.

1) In the same switching states, circulating current is eliminated with considering the same power sharing and same inductance ($K=h=1$) and same initial currents ($I_{2A}(t_{n-1})=I_{1A}(t_{n-}$

$_1$)). While with different power sharing, according to (5), *Kh*=1 has to be guaranteed in order to eliminate circulating current.

2) In different switching states (with same power sharing, same inductance and same initial currents), circulating current is calculated from (8) as:

$$I_{CC_A}(t_n) = V_{dc}\frac{(t_n - t_{n-1})}{2L_{1A}} = V_{dc}\frac{\Delta t}{2L_{1A}} \quad (9)$$

According to this equation, circulating current is depending on DC link voltage, inductance and Δt which is related to the switching frequency which are the main design parameters of the converters. However, semiconductor devices have limited switching frequency and by increasing switching frequency, switching loss increases, too. Increasing inductance increases cost as well as the volume of the whole system. Furthermore, it slows down the system's dynamic response and makes it difficult to control.

Total circulating current can be achieved as the sum of circulating currents of three legs (which is calculated from (5) and (8) based on the same or different switching of the legs). On the other hand, the difference between DC link currents of the upper converter at positive and negative points ($I_{dc,1p}$, $I_{dc,1n}$) can be defined as circulating current (which is much easier for measurement purposes). For the same power sharing (K=1) and referring to (1), the following equation can be achieved for the circulating current of the first converter.

$$I_{cc} = I_{CC_A} + I_{CC_B} + I_{CC_C} = \frac{(I_{1A} + I_{1B} + I_{1C})}{2} - \frac{(I_{2A} + I_{2B} + I_{2C})}{2} \quad (10)$$
$$= I_{1A} + I_{1B} + I_{1C} = I_{dc_{1p}} - I_{dc_{1n}}$$

where $I_{dc,j1}$ and $I_{dc,j1}$ are the currents at the positive and negative sides of DC-link ofthe first converter. It is clear that the circulating current for the second converter is the same as the first one at the opposite direction (I_{CC2}=-I_{CC1}).

III. PROPOSED METHOD TO ELIMINATE CIRCULATING CURRENT

According to the mentioned analysis in the previous section, elimination of circulating current requires exact power sharing between converters as well as same design parameters for parallel converters. Also, different switching states have to be avoided in this regard and synchronized switching states have to be applied. However, in some cases such

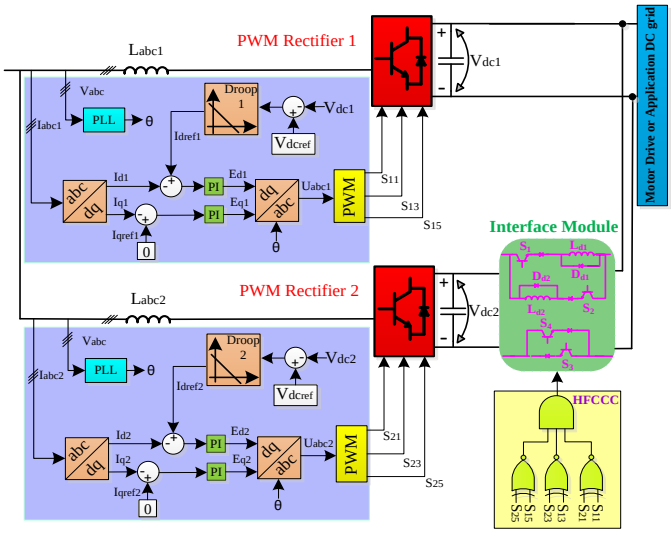
as unwanted shift between carries or any other mismatch between control system of converters, generation of circulating currents are inevitable. In addition, interleaved PWM strategy is also may be implemented in some applications which is totally against synchronized switching of converters. Worst case is V_0 switching vector (000) from one converter and V_7 (111) from another one where all three legs have different switching states. This creates three circulating current paths. Other conditions of different switching states for two legs and one leg are also possible which have fewer circulating currents.

Investigation on presented methods in literature reveals that complete elimination of circulating current with only switching vectors modifications is impossible in this context. These strategies require a precise interrelation between switching patterns of converters which imposes a high computational burden on processors. This in turn eliminates the number of modules to two and avoids the generalization of a modular system with multiple converters.

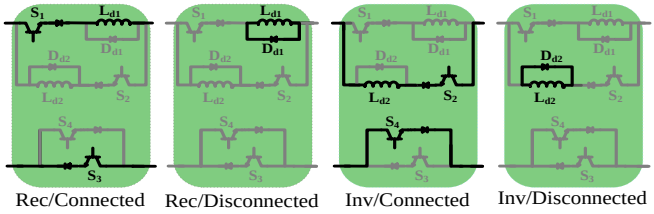
To eliminate circulating current, the path in which circulating current is created, should be cut off. Therefore, topology-based modification is a good alternative in this context. As sown in Fig.3(a), an interface circuit is added to the parallel configuration in order to disconnected the circulating current path. Fig.3(b) depicts different states of switches of the interface circuit. There are four switches which prepare bidirectional power flow (rectifier or inverter modes). As mentioned above, interface circuit connect (disconnect) the modules to DC link when the switching states of converters are same (different) in order to eliminate circulating currents. During rectifier (inverter) mode, for connection of modules switches S_1 & S_3 (S_2&S_4) are turned on. For disconnection of modules, all switches are turned off and only D_{d1} (D_{d2}) are circulating the current through L_{d1} (L_{d2}) during rectifier (inverter) mode of operation. Note that, L_{d1} and L_{d2} are tiny inductors which are used to suppress the current spikes of paralleling DC link capacitors. This inductor is defined as:

$$L_{d1} = \frac{V_{L_{d1}}}{\frac{di_{L_{d1}}}{dt}} \quad (11)$$

Where V_{Ld1} is the voltage of DC side inductor and is the difference between the DC link voltage of upper and lower converters which is the low voltage range. di_{Ld1}/dt is the acceptable tolerable current stress of the switch. Therefore, the mentioned inductor is a small amount with low volume and cost. Application of series diode with switches is due to the fact that at the event of switch disconnection, a reverse voltage may fall on the switch and damage it. Also, the parallel diode of the inductor is used to create a freewheeling path for inductor current when the series switch is disconnected.



(a)



(b)

Fig. 3: (a) Proposed structure with control strategy and interface module (b) connected or disconnected modes of parallel modules in rectifier/inverter modes of operation

The control strategy of each PWM rectifier in a two-module system is also shown in Fig.3(a) where proper reference voltage signals are defined in order to achieve precise power sharing which leads to elimination of low frequency circulating current. This method guarantees fast dynamic response and a high static performance depending on the quality of the internal current control loop.

The most crucial benefit of this method is its modularity (see Fig.4). In this case, each converter needs an interface circuit (in two-module system only one interface module would suffice). Similarity of switching states between ith and jth modules is shown in Fig.4(b) where M_{ij} of 0 (1) means different (same) switching states of two modules. Note that S_{i1}, S_{i3} and S_{i5} (S_{j1}, S_{j3} and S_{j5}) are the switching states of upper switch of legs a, b and c of the ith (jth) module. For multiple module system (with n parallel converters and i,j=1,2,…,n), similarity between all combination of modules has to be obtained. A number of similar modules with ith module is: $M_i = \sum_{j=1}^{n} M_{ij}, i \neq j$. As shown in Fig.4(c), modules selection block is based on M_i comparison such that for maximum M_i, modules with M_{ij}=1 is inserted in the parallel operation. This is to ensure the insertion of highest number of modules with similar switching states. In case of similar M_i, the module selection would be based on the modules with lower losses.

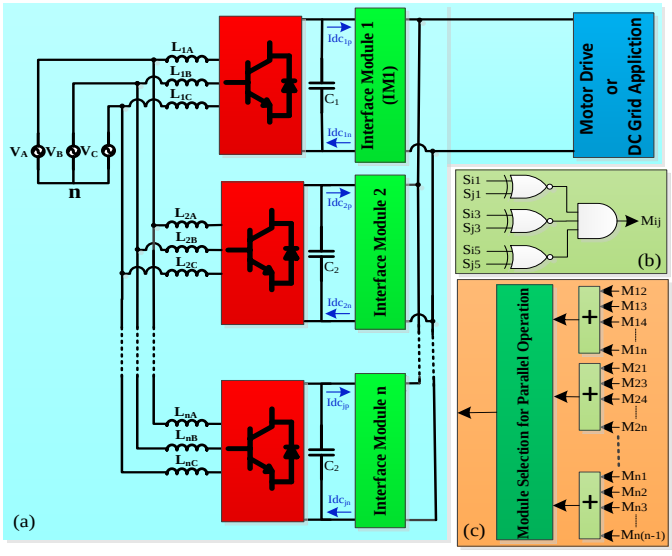
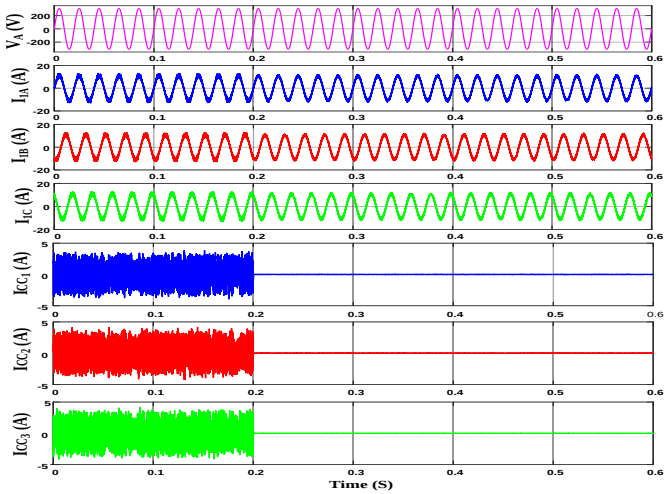


Fig. 4: (a) Proposed Modular structure (b) Similarity assessment of ith and jth modules (c) module selection for parallel operation

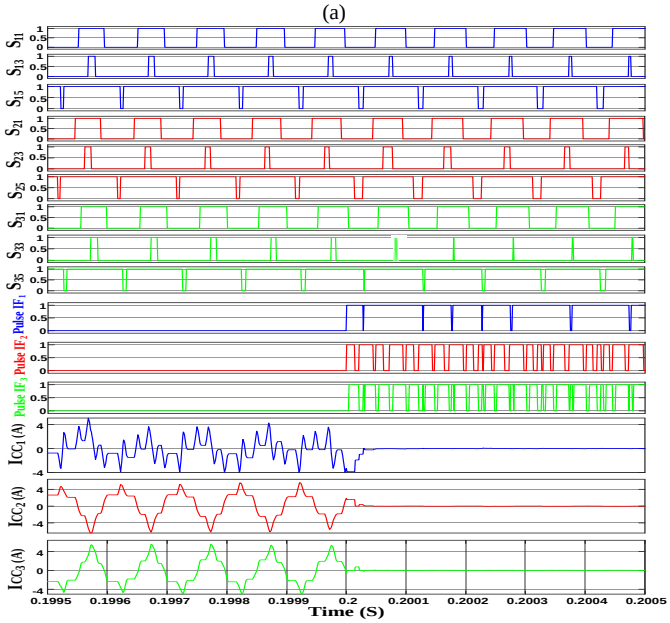
IV. SIMULATION AND EXPERIMENTAL RESULTS

A. Simulation Results

A three-module PPWMR system is considered for the simulation studies. AC side inductors (L_{jA} , L_{jB} , L_{jC} $(j=1, 2, 3)$) are 1mH and interface inductors (L_{1d} , L_{2d}) are considered 50µH. Capacitors C_o, C_1, C_2 are 500µF. peak AC voltage and output DC voltage is 300 and 600 volts respectively. A 30 Ω load is used and the switching frequency is 10 kHz. To investigate the performance of proposed system on circulating current, carrier signals of three converters shifted from each other by 5, 18 and 120 degrees to create circulating current intentionally. The Voltage of phase A, three-phase currents of the first converter and circulating current are shown in.5(a). A zoom view of switching pulses for three converters and their interface circuit alongside with circulating currents of three legs for two cases of 18 and 5 degrees shift between carrier signal of three inverter are shown in Fig.5(b) and (c) respectively.



(a)



(b)

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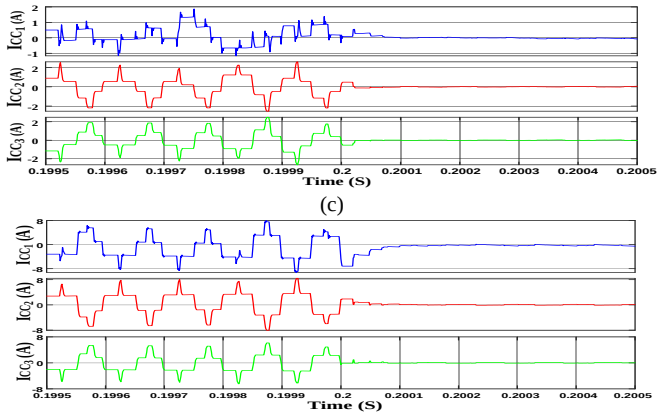


Fig.5. (a) Voltage of phase A, phase currents and difference of DC link currents for a three-module PPWMR: without proposed circuit (0-0.2S) and with proposed interface circuit (after 0.2S) for 18-degree phase difference between carrier signals (b) zoom for selected area along with switching pulses (c) circulating currents for carriers with 5-degree phase difference (d) circulating currents for carriers with 120-degree phase difference (interleaved)

Also, elimination of circulating current in interleaved PWM is somehow impossible (with only working on PWM) and reduction can be achieved (at the cost of changing switching states of parallel converters which is not the context of this paper). However, as shown in Fig.5(d), proposed interface system can suppress the circulating currents in interleaved PWM which is a great achievement. Analysis is carried out with a 120-degree phase shift between carrier signals of a three-module system. Fig.6 shows the performance of the system in removing circulating current for both rectifier (0.2S - 0.3S) and inverter (0.3S - 0.6S) modes of operation with preserving the quality of phase currents and voltages.

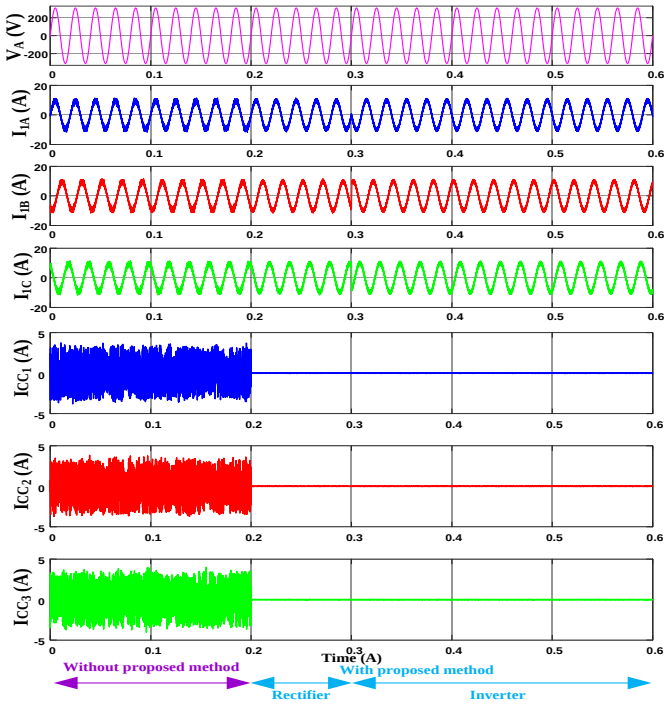


Fig.6. Voltage of phase A, phase currents and difference of DC link currents for a three-module PPWMR: without proposed circuit in rectifier mode (0-0.2S), with proposed interface circuit in rectifier mode (0.2S - 0.3S) and with proposed interface circuit in inverter mode (0.3S - 0.6S)

Proposed method is also applied to the case when the converters work in different power factors (with the same active power and with phase difference between voltage and current of 0, 45 and -45 degrees for converters 1, 2 and 3 respectively). As shown in Fig.7, Current of phase A for the first, second and third converter is shown. At 0.1S, the circulating current is eliminated and the ripple of the currents are also decreased. FFT of input current of (I_A) and each converter currents (I_{1A}, I_{2A}, I_{3A}) at PCC are shown. THD for input current is 6% which is decreased to 3.13%.

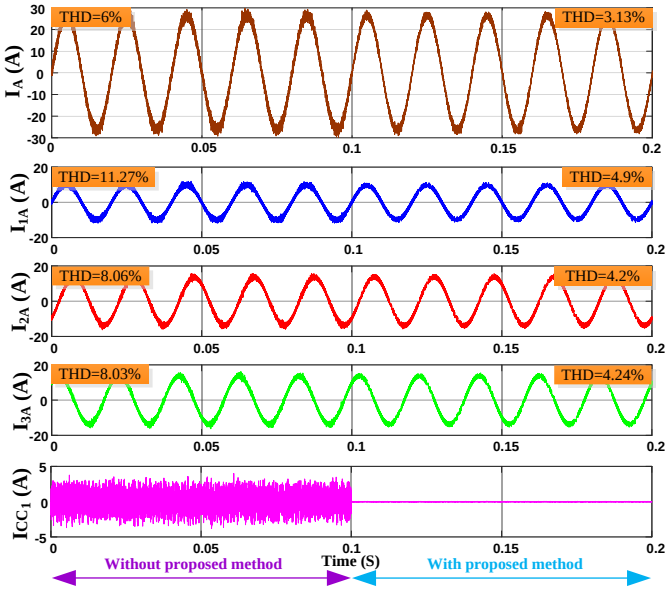


Fig.7. input current of phase A and currents of each converter at PCC.

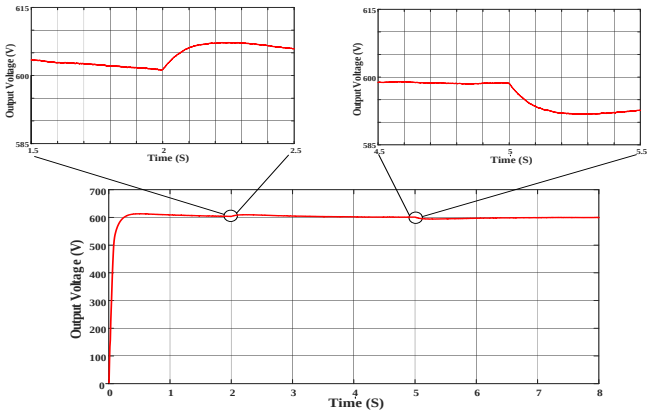


Fig.8. DC link voltage of a three-module PPWMR considering load changes from 100% to 50% (at t=2S) and vice versa (at t=5S)

Output voltage waveform is shown in Fig. 8 with changing the load from 100% to 50% of rated load at t=2S. Load reduction leads to increasing output voltage while the proposed control system maintain voltage on 600 V. Also, at t=5S, load changes from 50% to 100% of its rated value. Output voltage increases a little bit but the difference with its reference is not exceeded more than 10 volts. Therefore, system response is appropriate and DC link voltage reaches its reference value after any dynamics.

B. Experimental Results

Fig.9 shows a laboratory test setup of a two-module proposed system with the parameters of Table I.

TABLE I
EXPERIMENTAL PARAMETERS

Component	Type
PWM Rectifiers Switches	GW38IH130D
Switch gate drivers	HCPL-A 316J
Voltage Sensors	MINMAX-MAU202
Current Sensor	TAMURA-10ZB9
Interface Circuit Switches	IGW50N60T
Main Control Chip	DSP TMS320F28335
Voltage Probe 1	P 2100 100MHz
Voltage Probe 2	PINTEK DP-50
Current Probe 1,2,3	FLUKE 80i-110s AC/DC
L_{1A}, L_{1B}, L_{1C}, L_{2A}, L_{2B}, L_{2C}	Ferrite Core EE110, 5mH
L_{1d}, L_{2d}	Iron Powder Core T184-52, 60μH
C_1, C_2	450 V 470μF
V_{AC}(Peak)	100 V
V_{DC}	300 V
Load	60Ω
f_{SW}	10 kHz

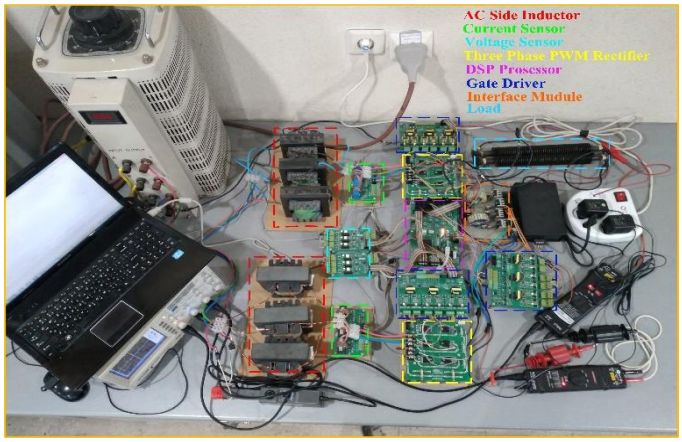


Fig.9. Laboratory test setup of two-module PPWMR

The voltage of phase A and three-phase currents of upper converter (with the peak value of 5A) is shown in Fig.10 without any circulating current control strategy. $I_{dc,1p}$ and $I_{dc,1n}$ are shown in Fig.11 and their difference are determined as circulating current. According to figure, however, as soon as activating interface circuit, circulating current is totally eliminated.

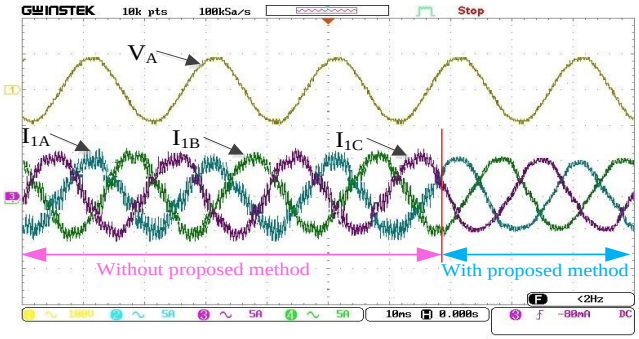


Fig. 10: Voltage of phase A and three-phase input current of three-phase rectifier without and with proposed method

Fig. 12 shows the DC link currents at positive and negative points and their difference for Unequal power sharing (K≠1). It is clear that by using proposed method, circulating current is reduced to a great extent. Note that the ripples of the phase currents of two converters are also reduced after activating interface module cancelation of circulating current.

Effects of Load change from 100% to 50% and vice versa on the converter current and DC link voltage are shown in Fig.13(a) and (b) respectively. According to this figure, current quality is high, output voltage is accurately controlled with little overshoot and undershoot. Proposed converter is also tested at standalone inverter mode of operation. A 300V DC voltage is converted to a sinusoidal AC voltage with a high-quality low ripple current. Fig.14 shows AC output voltage (upper waveform) and load current (lower waveform) of phase A with a three-phase resistive load of 20Ω. This ensures the application of such converter in both modes of operation.

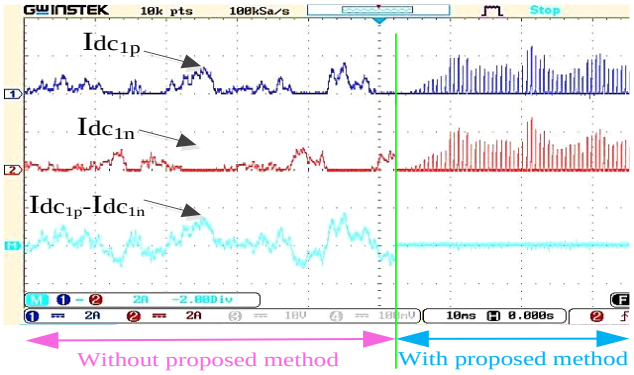


Fig. 11: DC link currents at positive and negative points ($I_{dc,1p}$, $I_{dc,1n}$) and circulating current of the upper converter

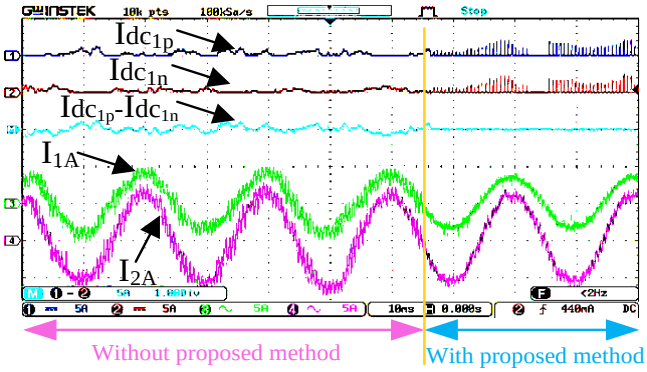
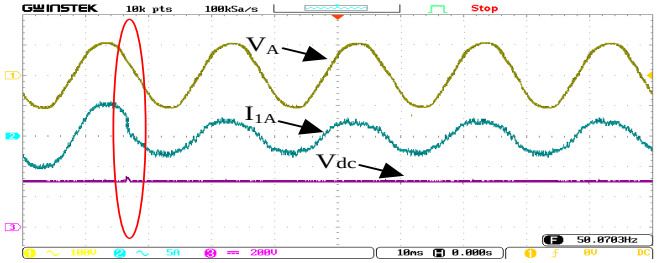
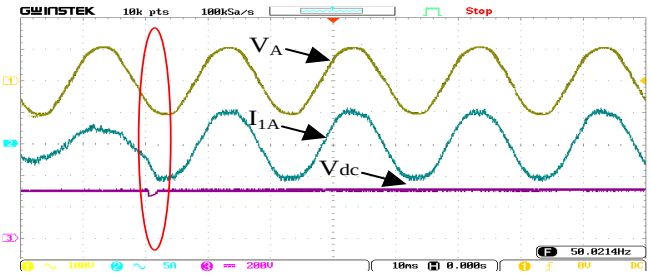


Fig. 12: DC link currents of the first converter and their difference and phase A current of both converters in case of unequal power sharing



(a)



(b)

Fig.13. Voltage and current of phase A along with DC link voltage for Load change from (a) 100% to 50% and (b) 50% to 100%

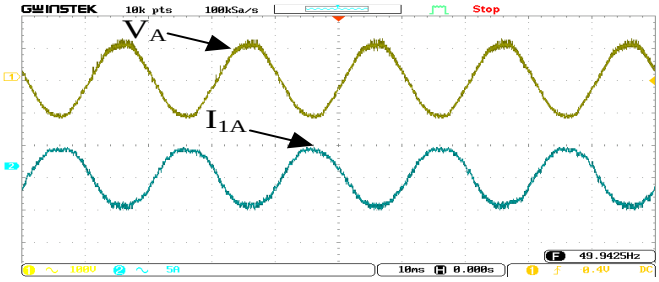


Fig.14: Voltage and current of phase A for proposed parallel converter with interface circuit in inverter mode of operation

V. DISCUSSION

A discussion as carried out regarding the operating factors of the PPWMR with and without proposed interface circuit.

A. Loss Calculations

A detailed loss analysis of the parallel converter with and without proposed interface circuit is carried out. Switches/diodes losses and six inductors' losses (considering their internal resistance) are considered in the loss calculation.

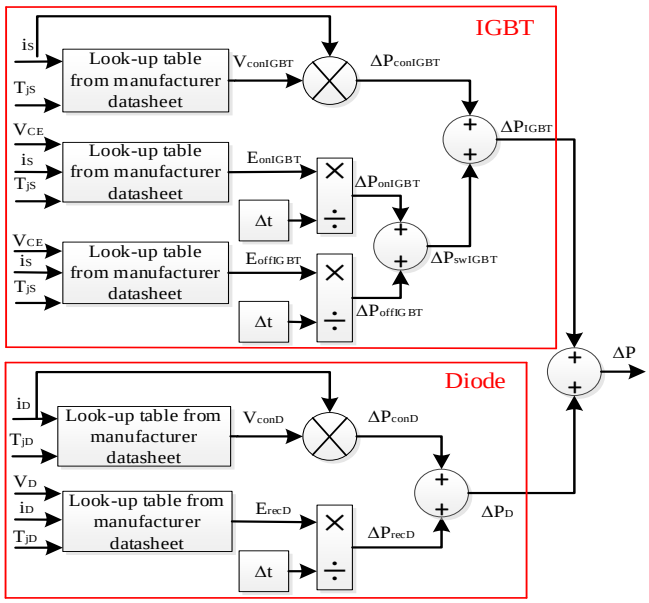


Fig. 15. Loss calculation for switches and diodes

As shown in Fig.15, Losses of switches (IGBTs) and diodes are calculated as [35]:

$$\Delta P = \Delta P_{con_{IGBT}} + \Delta P_{sw_{IGBT}} + \Delta P_{con_D} + \Delta P_{rec_D} \quad (12)$$

where $\Delta P_{con_{IGBT}}$, $\Delta P_{sw_{IGBT}}$, ΔP_{con_D} and ΔP_{rec_D} are conduction losses of IGBTs, switching losses of IGBTs, conduction losses of diodes and diodes reverse recovery losses respectively which are calculated as follows:

$$\Delta P_{con_{IGBT/D}} = V_{con_{IGBT/D}}(t) \times i_{IGBT/D}(t) \quad (13)$$

$$\Delta P_{on_{IGBT}} = \frac{E_{on_{IGBT}}}{T_S} \quad (14)$$

$$\Delta P_{off_{IGBT}} = \frac{E_{off_{IGBT}}}{T_S} \quad (15)$$

$$\Delta P_{rec_D} = \frac{E_{rec_D}}{T_S} \quad (16)$$

where $V_{con_{IGBT/D}}$ and $i_{IGBT/D}$ are conduction voltage and current of the switch/diode respectively. $E_{on_{IGBT}}$ and $E_{off_{IGBT}}$ are turn-on and turn-off energy losses of the switch which are achieved from $E_{on/off_{IGBT}} - i_S$ curves of the semiconductor. E_{rec_D} is the reverse recovery energy of diode. Also, Inductor losses at input side is considered in the analysis.Fig.16 shows the efficiency of the proposed converter in different voltage and current ranges with and without proposed interface. It is evident that during high power and high voltage applications where high circulating current passes through semiconductors, proposed topology with interface circuit has lower loss. This is due to elimination of circulating current from 12 switches and six inductors and adding two switches in conduction mode.

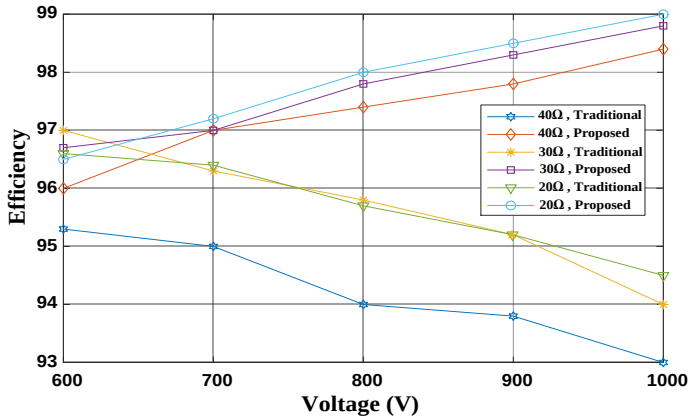


Fig. 16. Efficiency with and without proposed interface circuit at different operating conditions

B. Reliability

Reliability evaluation of the parallel converters with and without proposed interface circuit is presented using Markov approach. Note that hazard rates of power electronic components are only considered in their useful life and other phases such as de-bugging (which are related to manufacturing errors) and fatigue phases of the components are note considered in the analysis. Fig.17 shows the Markov Chain of the mentioned system which are not employing any

fault tolerant scheme. It has only two states (State1: healthy mode and State2: failure mode).

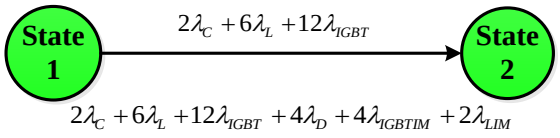


Fig.17. Markov chain of PPWMR with and without interface circuit

It is assumed that failure of at least one component leads to complete failure. For the conventional PPWMR, failure rate of the converter is calculated as:

$$\lambda_{12_{conventional}} = 2\lambda_C + 6\lambda_L + 12\lambda_{IGBT} \quad (17)$$

For the proposed PPWMR with interface circuit, failure rate of the components is calculated as:

$$\lambda_{12_{Proposed}} = 2\lambda_C + 6\lambda_L + 12\lambda_{IGBT} + 4\lambda_D + 4\lambda_{IGBT_{IM}} + 2\lambda_{L_{IM}} \quad (18)$$

Note that additional interface has for four switches, 2 diodes and 2 inductors for bidirectional power flow (rectifier or inverter mode). Therefore, only two switches, 1 diode and 1 inductor are considered in the calculation. λ_{IGBT} , λ_D , λ_C and λ_L are the failure rates of switches, diodes, capacitors and inductors respectively which are calculated as:

$$\lambda_{IGBT} = \lambda_b \pi_T \pi_A \pi_Q \pi_E \quad (19)$$

$$\lambda_D = \lambda_b \pi_T \pi_S \pi_C \pi_Q \pi_E \quad (20)$$

$$\lambda_C = \lambda_b \pi_{cv} \pi_Q \pi_E \quad (21)$$

$$\lambda_L = \lambda_b \pi_C \pi_Q \pi_E \quad (22)$$

For each component, λ_b , π_Q , π_E are basic failure rate factor, quality factor, environment factor of mentioned components respectively. π_A is the application factor of the switch (linear or switching mode). π_{cv} and π_C are capacitance factor and inductor construction factor. Also, π_S is the electrical stress factor of the diode. Mentioned parameters can be easily extracted from [36] regarding the type of the component and its application. π_T is the temperature factor for switches and diodes:

$$\pi_{T_{IGBT}} = \exp\left[-1925\left(\frac{1}{T_{j_{IGBT}} + 273} - \frac{1}{298}\right)\right] \quad (23)$$

$$\pi_{T_D} = \exp\left[-3091\left(\frac{1}{T_{j_D} + 273} - \frac{1}{298}\right)\right] \quad (24)$$

where $T_{j_{IGBT}}$ and T_{j_D} are the junction temperature of the switch and diode respectably.

$$T_{j_{IGBT}} = T_A + R_{JA_{IGBT}} \times P_{loss_{IGBT}} \quad (25)$$

$$T_{j_D} = T_A + R_{JA_D} \times P_{loss_D} \quad (26)$$

T_A is the ambient temperature. $P_{loss_{IGBT}}$ and P_{loss_D} are the losses of the switch and diode which can be achieved from Fig.15. $R_{JA_{IGBT}}$ and R_{JA_D} are the junction ambient resistance.

According to the Fig.17 and mentioned equations, the probability of each states is calculated as:

$$\frac{d}{dt}\begin{bmatrix} P_1(t) & P_2(t) \end{bmatrix} = \begin{bmatrix} P_1(t) & P_2(t) \end{bmatrix} \begin{bmatrix} \lambda_{11} & \lambda_{12} \\ \lambda_{21} & \lambda_{22} \end{bmatrix} \quad (27)$$

where P_1 and P_2 are probability of states 1 and 2 respectively. λ is the transition matrix where:

$$\lambda_{21} = \lambda_{22} = 0 \quad , \quad \lambda_{11} = -\lambda_{12} \quad (28)$$

Assuming the chain is started from state1 which is healthy state, following initial condition is occurred and the reliability is calculated as:

$$P(0) = \begin{bmatrix} 1 & 0 \end{bmatrix} \quad (29)$$

The reliability is calculated as:

$$R(t) = P_1(t) = e^{-\lambda_{12} t} \quad (30)$$

Mean Time to Failure (MTTF) is obtained as:

$$MTTF = \int_0^\infty R(t)dt \quad (31)$$

Figure 18 shows the graphs for the reliability the PPWMR with and without interface system in different application scenarios. According to analysis, reliability is even increased in some cases (high power and high voltage applications which generates high circulating currents) in comparison with the system without interface circuit. In some other case (normally lower circulating currents), the reliability is decreased but the amount of this decrement is negligible. Note that this tiny decrement leads to elimination of circulating currents at the benefit of removing control complexity.

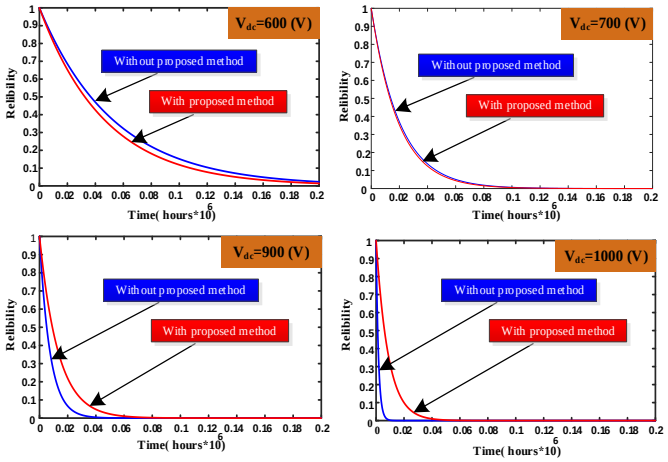


Fig.18. Reliability of the PPWMR with and without proposed interface in different DC-link voltages and power ratings

VI. CONCLUSION

In this paper, an interface circuit is proposed to eliminate circulating current of parallel converters. Converters' switching states have no limitations in this structure which leads to high quality current waveforms. Also, it has a very simple control that causes the fast dynamics of the whole system. Mentioned interface circuit avoids complex calculations of previous circulating current reduction strategies which were mainly dealt with manipulating on switch states of multiple converters. Accordingly, the

proposed structure is modular and can be implemented for any number of parallel converters. The analyses performed by simulation and laboratory samples, confirmed the performance of proposed topology in different modes of operations such as load change, bidirectional power flow and also unequal power sharing of the converters.

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