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ScienceDirect
Energy Reports 8 (2022) 813–830
www.elsevier.com/locate/egyr

2022 The 4th International Conference on Clean Energy and Electrical Systems (CEES 2022), 2–4 April, 2022, Tokyo, Japan

Model predictive control of Packed U-Cell inverter for microgrid applications

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Received 16 May 2022; accepted 19 May 2022
Available online xxxx

Abstract

In this paper, an outline of microgrid arrangements and control methods at various hierarchical levels of Packed U-Cell (PUC) converters are provided. The paper discusses the control of these topologies using various techniques. The goal of these control strategies is to maintain a small THD, superior steady-state, fast-dynamic response, and high-power factor while balancing capacitor voltages under different operating conditions. The PI current controller is modelled on five and seven-level PUC inverters. The PI voltage and current controllers have also been modelled on a seven-level PUC inverter. Thereafter, model predictive control of five, seven and fifteen level inverters are also formulated and then simulated using MATLAB/Simulink. Finally, HIL validation of different PUC inverters is performed.

Peer-review under responsibility of the scientific committee of the 4th International Conference on Clean Energy and Electrical Systems, CEES, 2022.

Keywords: Model predictive control; PI control; Packed U-Cell Inverter

1. Introduction

The electrical power generated from renewable energy resources (solar, wind and hydro, etc.) are either used for domestic purposes directly or they are supplied to the grid [1]. For example, the power generated by a solar plant is of dc nature which is first conditioned and then inverted to get an alternating output. This ac power is then synchronized with the grid according to the grid's characteristics (frequency and phase angles) [2]. In each of the steps, there are many parameters to be controlled in an accurate manner so that power quality is maintained. For this purpose, the most suitable consideration is the multi-level family converters.

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https://doi.org/10.1016/j.egyr.2022.05.188

Peer-review under responsibility of the scientific committee of the 4th International Conference on Clean Energy and Electrical Systems, CEES, 2022.

Due to improved power quality compared to their two-level counterparts in recent times, multilevel inverter (MLI) topology has become increasingly accepted in commercial applications. The reduced harmonic deformation, improved waveform like a sinusoidal waveform and enhanced use of switches due to diminished voltage stress. MLI have their uses in various fields of renewable energy sources including, HVDC, distributed generation (DG) system, application of industrial drive systems, uninterruptible power supplies, etc. [3–6]. Based on a few semiconductor devices coupled with different dc links, MLIs generate sinusoidal waveforms at their outputs through staircase waveforms. MLI has traditionally been used in three major topologies in commercial applications within the last few decades: Cascade H-Bridge (CHB) inverters, Flying Capacitor (FC) inverters and Neutral Point Clamped (NPC) inverters. Each MLI topology, however, have some drawbacks, such as the increasing count of source necessities, the balancing of capacitor voltage, and the high necessity for switches counting in the CHB, FC, and NPC network topologies, respectively [3].

To overcome the shortcomings of these inverters, new topologies are proposed with many effective results. A very capable topology is the Packed U Cell (PUC) inverter which includes the merits of cascaded H-Bridges and flying capacitor [4]. PUC inverter employs a single stand-alone DC source while the other DC buses are maintained to obtain appropriate voltage levels. Compared to conventional topologies, it utilizes fewer switches. Many control techniques have been evolved and studied on PUC converters either in inverter or rectifier operation [5]. In today's grid, both active and reactive power are distributed with the help of inverters, which allow for online control of grid parameters. Conventional control schemes are not suitable for such applications. With increasing computational capabilities of micro controllers, fast computing is not a matter of concern. Hence, predictive algorithms can be applied easily for the inverter control.

Model Predictive Control (MPC) was introduced in the late 60 s and was chiefly conned to process and chemical industries. During the 1970s, it was introduced to Power Electronics and Drives applications and it appears to be a suitable control approach [6]. In the comparison of classical control to the MPC, a significant number of computations are performed at every sampling interval before feeding the control signals to the system. It comprises estimating the future behaviour of the controlled variable, competing it with the reference, then the comparison of the predicted data with the reference data determines what the cost function should be optimized for [7,8]. MPC responds very quickly, tracks reference values more accurately, and does not require any gain tuning, etc. [9].

2. PUC inverters

2.1. Seven level PUC inverter topology

The PUC topology for seven-level inverters can be obtained from Fig. 1. This contains one DC source, 6 switches, and a capacitor. The PUC7 inverter aims to keep the capacitor voltage at one third of the DC voltage (V_1) [10]. Due to its inherent limitations, the PUC inverter can only generate voltage values up to a DC voltage value. The PUC-based inverter has the advantage of providing a multi-level distribution of DC bus voltage so that load voltage harmonics are reduced. This process diminishes the needed filter size at the output of the inverter. The switching strategy for PUC7 inverter is presented below in Table 1 [10].

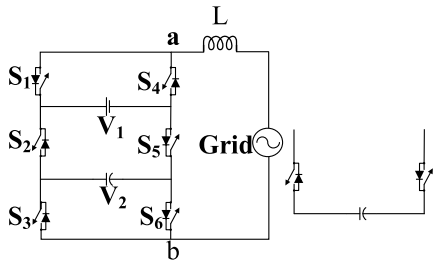

Fig. 1. Seven level Packed U-Cell topology and a single U-Cell.

Table 1. Switching states for seven-level and five-level inverters.

Switching states	S_1	S_2	S_3	V_{ab}	Capacitor voltage
1	1	0	0	V_1	No effect
2	1	0	1	$V_1 - V_2$	Charging
3	1	1	0	V_2	Discharging
4	1	1	1	0	No effect
5	0	0	0	0	No effect
6	0	0	1	$-V_2$	Discharging
7	0	1	0	$V_2 - V_1$	Charging
8	0	1	1	$-V_1$	No effect

2.2. Five level PUC inverter topology

For a five-level PUC inverter, the primary circuit diagram, Fig. 1, has one DC supply, six power electronic switches, and a capacitor. The PUC7 and PUC5 have same circuit diagram, only difference is of value at which capacitor voltage is maintained. The 5-level topology might compromise the voltage output levels to generate power of low THD and element number to avoid the unwanted rise in the expense and the inverter's dimension [11].

The switching states, presented Table 1, for a five-level PUC inverter is such that it uses only six switching states omitting two states per cycle, one in the positive cycle of the sinusoidal source wave of discharging (switching state 3) and one in the negative cycle of the sinusoidal source wave of charging (switching state 7) keeping all other switching states same as that of PUC7.

2.3. Fifteen level PUC inverter topology

Fig. 2 illustrates the topology of fifteen-level PUC inverters. It comprises four branches of switches detached by three auxiliary sources. The DC bus is linked across the source V_1, while the voltages V_2 and V_3 are maintained by the control technique around their corresponding values. These capacitor voltages are maintained to $3V_1/7$ and $V_1/7$ correspondingly to produce the 15-level output voltage. Table 2 summarizes the switching states as well as corresponding output voltage of this topology.

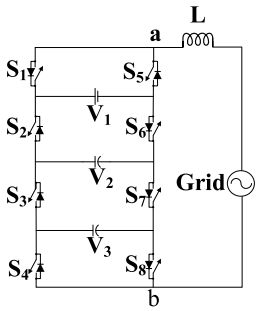

Fig. 2. Basic circuit for fifteen level PUC topology.

3. Microgrid

A microgrid, presented in Fig. 3, may be portrayed as a group of distributed generation (DG) units, loads, and energy storage systems (ESSs) operating in synchronization to dependably distribute electricity, integrated to the primary power system at the supply level at a solo point of connection, the Point of Common Coupling (PCC).

Microgrid may be stated as the alternative for dependable connection of renewable DERs, including Storage Systems and controllable loads. This microgrid is now unified with the utility grid and it is resembled as a single element. In other words, it can be called as a knot of loads, DERs, and ESSs connected to a host or primary grid at the supply level at Point of Common Coupling.

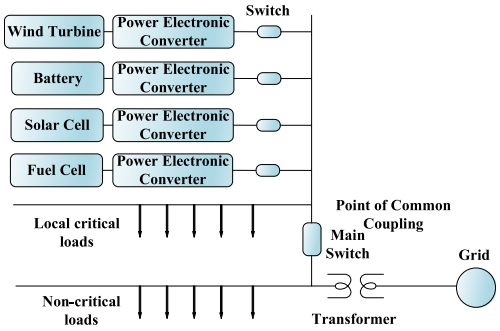

Fig. 3. Point of common coupling (PCC).

Table 2. Switching states of fifteen-level inverter.

Switching state	S_1	S_2	S_3	S_4	V_{inv}
1	0	0	0	0	0
2	0	0	0	1	$-V_3$
3	0	0	1	0	$V_3 - V_2$
4	0	0	1	1	$-V_2$
5	0	1	0	0	$V_2 - V_1$
6	0	1	0	1	$V_2 - V_1 - V_3$
7	0	1	1	0	$V_3 - V_1$
8	0	1	1	1	$-V_1$
9	1	0	0	0	V_1
10	1	0	0	1	$V_1 - V_3$
11	1	0	1	0	$V_1 - V_2 + V_3$
12	1	0	1	1	$V_1 - V_2$
13	1	1	0	0	V_2
14	1	1	0	1	$V_2 - V_3$
15	1	1	1	0	V_3
16	1	1	1	1	0

4. proportional–integral (PI) control of PUC inverters

4.1. Current control of seven-level PUC inverter

Fig. 4 shows the PI current control of PUC7 inverters. Considering the PUC7 topology, the switches S_4, S_5 and S_6 should be operating just opposite of S_1, S_2 and S_3. Thus, the individual set of switches (S_1, S_4), (S_2, S_5) and (S_3, S_6) could not be turned on at the same time.

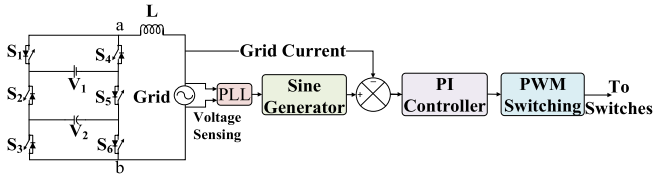

Fig. 4. Block diagram for current control of the PUC7 inverter.

In the situation of using a capacitor along with a DC voltage source, the output terminal voltage is consequently attained from the trailing seven levels (V_1, $2V_1/3$, $V_1/3$, 0, $-V_1/3$, $-2V_1/3$, $-V_1$). In sequence to achieve the mentioned levels, the auxiliary device voltage (V_2) must be controlled to $V_1/3$ [12].

4.2. Current control of five-level PUC inverter

The PI current control of PUC-based five-level inverters can be obtained from Fig. 4. The fundamental difference between both is that in the case of a seven-level inverter, the capacitor voltage (V_2) is kept at one third of the DC supply. In contrast, in the event of the PUC5 inverter, the capacitor voltage (V_2) is sustained at fifty percent of the DC voltage supply. The possible voltage level obtained in the case of five-level inverter is $-V_1$, $-V_1/2$, 0, $V_1/2$, and V_1.

4.3. Voltage control and current control of PUC7 inverter

In this control, as drawn in Fig. 5, the first PI control loop tries to sustain the auxiliary device voltage (V_2) to the reference capacitor voltage and minimize the error between the two values. Once the error minimization is achieved, another PI control loop is applied between the reference current, generated using the output of the first PI controller and the sinusoidal unity wave attained from the PLL block. The resultant of this PI controller is taken as the base sinusoidal signal given to PWM for the production of the triggering pulse for toggling the switches.

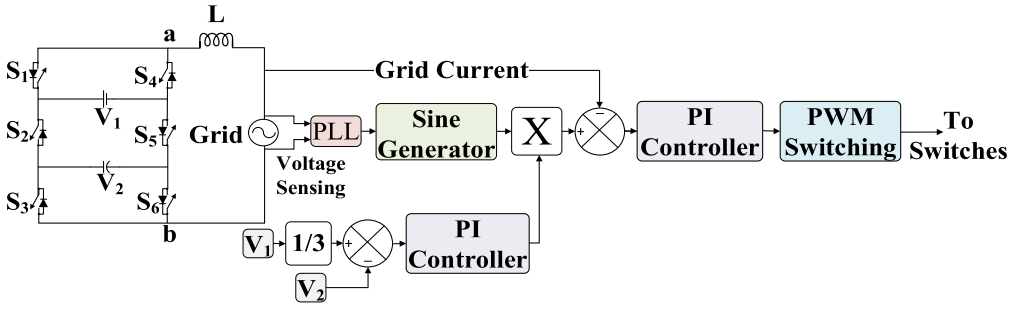

Fig. 5. Block diagram for voltage and current control of the PUC7 inverter.

5. MPC of PUC inverters

For simplicity and stability, the Proportional–Integral (PI) based linear controller is normally used to control the converter. On the other hand, this method exhibits a poor dynamic response and involves a complicated switching scheme for maintaining the capacitor voltage at DC voltage. The basic block diagram for MPC of PUC MLIs topology is given in Fig. 6.

The basic idea present in the MPC can be well illustrated from the flowchart as shown in Fig. 7 and can be summarized as [13]:

- Use of a prototype in order to forecast the forthcoming values until a limit in time.
- A cost function that characterizes the anticipated behaviour of the model.
- The ideal actuation should be determined by diminishing the cost function

5.1. MPC of seven level PUC inverters

MPC consists of measuring variables which in this circumstance are the auxiliary component voltage V_2 and the grid current i_g which are used in the algorithm to determine the future values of the controlled variable for every switching state as shown in Fig. 8.

From the previous block diagram, it can be seen that the grid current and the auxiliary component voltage are being measured for every sampling time. These data are then used by the derived model to calculate future values. The current referential values can be obtained using phase locked loop. Once future values are calculated using the deduced formula, a cost function is determined by comparing the forecasted and recommended values for each of the switching states which are seven in the case of the PUC inverter as different states are responsible for different voltage levels [12,14,15].

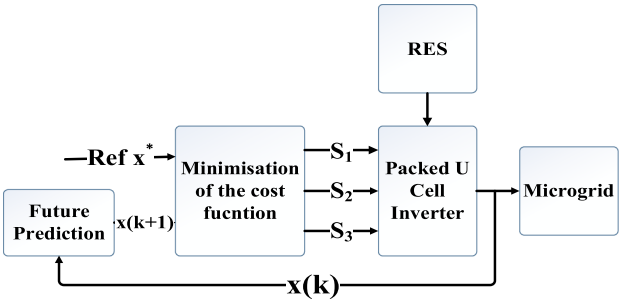

Fig. 6. Block representation of MPC scheme.

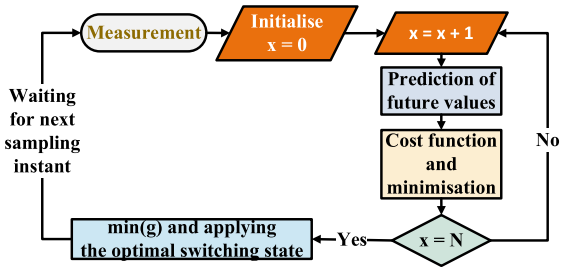

Fig. 7. Flowchart of the MPC implementation.

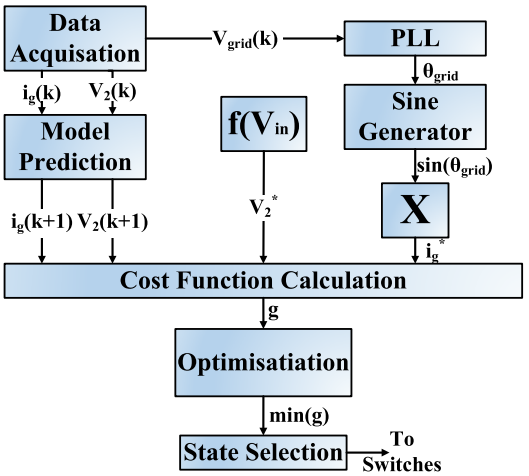

Fig. 8. Block diagram of MPC of PUC7 inverters.

The grid injected current i_g and the auxiliary component voltage V_2 are the variable which are going to be regulated. Therefore, to ease up the mathematical computation, two different variables S_a and S_b are introduced by (1) and (2). Also, the new switching state is demonstrated in Table 5.

$$S_a = S_1 - S_2 \tag{1}$$

$$S_b = S_2 - S_3 \tag{2}$$

The inverter terminal output voltage is determined using (3)

$$V_{inv} = S_a V_1 + S_b V_2 \tag{3}$$

Capacitor Voltage is given by (4)

$$i_2 = C_2 \frac{dV_2}{dt} = -S_b i_g \tag{4}$$

Using Kirchhoff's Voltage Law (KVL), the load current relation could be expressed by (7) as:

$$V_{inv} = V_g + r \times i_g + L \frac{di_g}{dt} \tag{5}$$

Similarly based on Forward Euler Approximation, the output current may be replaced as

$$\frac{di_g}{dt} = \frac{i_g\,(k+1) - i_g(k)}{T_s} \tag{6}$$

Thus, using (7) and (8), the load current could be written as

$$i_g\,(k+1) = \left(1 - \frac{r \times T_s}{L}\right) \times i_g\,(k) + \frac{T_s}{L}\left(V_{inv}\,(k) - V_g\right) \tag{7}$$

Lastly, the cost function g may be obtained as (10)

$$g\,(k) = k_1 \left(i_g\,(k) - {i_g}^*\right)^2 + k_2 \left(V_2\,(k) - {V_2}^*\right)^2 \tag{8}$$

The cost function, g, is computed for all the probable cases, however optimum states are those corresponding to the minimum cost function. Once S_a and S_b are determined, the S_1, S_2 and S_3 can be derived from (1) and (2).

5.2. MPC of five level PUC inverters

The basic block diagram of this topology is the same as that of the PUC7 inverter. The primary difference is that in the case of a PUC7 inverter, and the capacitance–voltage is kept at the 1/3rd of the DC voltage supply, while for PUC5 inverter, it is half of the DC voltage supply [16,17]. Hence, all the mathematical relationships are the same as that of seven level inverters as mentioned above except the switching states are changed as shown in Table 6.

5.3. MPC of PUC based fifteen level inverters

The circuit diagram shown in Fig. 9 is used to generate fifteen level inverter voltage by maintaining the capacitor voltages (V_2 & V_3) at $3V_1/7$ and $V_1/7$ respectively. The switches (S_1, S_5), (S_2, S_6), (S_3, S_7) and (S_4, S_8) are controlled in an alternating manner [18].

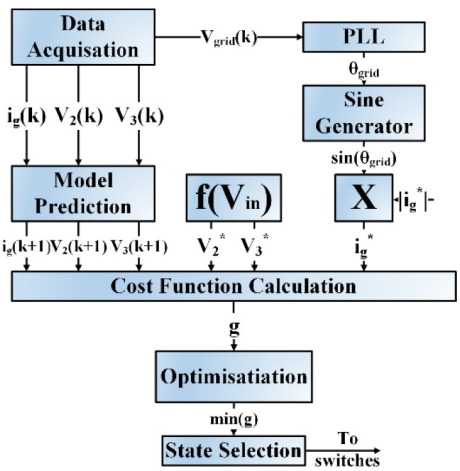

Fig. 9. Block diagram of MPC of PUC15 inverters.

Using Kirchhoff's laws, the voltages of the capacitors $V_1(t)$, $V_2(t)$ and $V_3(t)$, the grid current $i_g(t)$ and the switching states s_i (i = 1, 2, 3, 4) are related by (9)–(11)

$$C_2 \frac{dV_2(t)}{dt} = (s_3 - s_2)\, i_g(t) \tag{9}$$

$$C_3 \frac{dV_3(t)}{dt} = (s_4 - s_3)\, i_g(t) \tag{10}$$

$$L \frac{di_g(t)}{dt} = (s_1 - s_2)\, V_1(t) + (s_2 - s_3)\, V_2(t) + (s_3 - s_4)\, V_3(t) - V_g(t) \tag{11}$$

Applying the Forward Euler Approximation approach

$$\frac{df(t)}{dt} = \frac{f(k+1) - f(k)}{T_s} \tag{12}$$

$$V_2(k+1) = V_2(k) + \frac{T_s}{C_2}(s_3 - s_2)\, i_g(k) \tag{13}$$

$$V_3(k+1) = V_3(k) + \frac{T_s}{C_3}(s_4 - s_3)\, i_g(k) \tag{14}$$

$$i_g(k+1) = i_g(k) + \frac{T_s}{L}\left[(s_1 - s_2)\, V_1(k) + (s_2 - s_3)\, V_2(k) + (s_3 - s_4)\, V_3(k) - V_g(k)\right] \tag{15}$$

In this work, the state variables are normalized by calculating their maximal variations ΔV_{2max}, ΔV_{3max}, and Δi_{gmax} of the state variables (16)–(18) and cost function is formulated in (19)

$$\Delta V_{2max} = \frac{2i_g}{C_2} T_s \tag{16}$$

$$\Delta V_{3max} = \frac{2i_g}{C_3} T_s \tag{17}$$

$$\Delta i_{gmax} = \frac{2V_1}{L} T_s \tag{18}$$

$$g = \lambda_v \left| \frac{V_2^* - V_2(k+1)}{\Delta V_{2max}} \right| + \lambda_v \left| \frac{V_3^* - V_3(k+1)}{\Delta V_{3max}} \right| + \lambda_i \left| \frac{i_g^* - i_g(k+1)}{\Delta i_{gmax}} \right| \tag{19}$$

where λ_v and λ_i are scaling values, that could be modified as per required working criteria. These scaling values are primary adjusted to accomplish the constancy and required working criteria of the PUC inverter. The adjustment can be done such that the current distortion and the deviation of auxiliary device voltage from the reference is reduced.

6. Simulation results

The simulation parameters for PI control are tabulated in Table 3 and for MPC in Table 4. Firstly, the simulation results for PI control are presented in Figs. 10–18. Then, the results using MPC are demonstrated in Figs. 19–27.

Table 3. Simulation parameters for PI control.

Parameters	Values
DC voltage (V_1)	315 V
DC capacitor (C_1)	9800 μF, 9500 μF
Line inductor (L)	5 mH, 4mH
Grid voltage (RMS)	220 V
Line frequency	50 Hz
Modulating frequency	16 kHz
Proportional gain (K_p)	0.018, 1.2, 0.001
Integral gain (K_i)	50, 0.1, 70

Fig. 10 shows the output voltage of PUC7 inverter when applying only current PI control. This voltage can be improved by applying cascaded voltage–current PI control loops as shown in Fig. 16. Consequently, the grid injected current, using the cascaded PI control loops, has better reference signal tracking compared with that of a single PI control loop as presented in Figs. 11 and 12 respectively.

Table 4. Simulation parameters for MPC.

Parameters	Values
DC bus voltage (V_1)	315 V
DC capacitor (C_2)	9800 μF
Line inductor (L)	5 mH
Parasitic resistance (r)	0.2 Ω
AC Grid voltage (V_g) (RMS)	220 V
Line frequency (f)	50 Hz
Sampling time (T_s)	10 μs

Table 5. Modified switching state based on MPC for PUC7 inverter.

States	S_a	S_b	V_{inv}
1	1	0	V_1
2	1	−1	$V_1 - V_2$
3	0	1	V_2
4	0	0	0
5	0	−1	$-V_2$
6	−1	1	$V_2 - V_1$
7	−1	0	$-V_1$

Table 6. Modified switching states for PUC5 inverter.

States	S_a	S_b	V_{inv}
1	1	0	V_1
2	1	−1	$V_1 - V_2$
4	0	0	0-
5	0	−1	$-V_2$
7	−1	0	$-V_1$

Also, in regard to the capacitor voltage, the single PI control loop has higher error as shown in Fig. 12 while in the case of the cascaded PI control loops, the capacitor ripple is considerably diminished as drawn in Fig. 18. The PI control of the PUC5 based inverter output is plotted in Fig. 13. PUC5 is simulated just to show the simplicity of control applied but at the same compromising the voltage and current THD. The grid injected current is shown in Fig. 14. The auxiliary device voltage is plotted in Fig. 15. The inverter output voltage and grid injected current in case of cascaded PI control loop is shown in Figs. 16 and 17 respectively.

The MPC of five, seven and fifteen level PUC topologies are simulated, and their respective graphs are plotted. From Figs. 19 and 16, it could be evidently observed that the output voltage profile of PUC7 based inverter is better in case of the PI than that of the MPC control. Fig. 19 shows the output voltage of PUC7 inverter using MPC while the grid injected current is presented in Fig. 20. The capacitor voltage when applying MPC on PUC 7 is demonstrated in Fig. 21. Similarly, the inverter output voltage, grid current and the capacitor voltage when applying MPC on PUC5 topology are presented in Figs. 22–24, respectively.

For the PUC15 inverter, the grid injected current is plotted in Fig. 25 which is very closely following the reference current. The reference and actual capacitor voltages (VC2 and VC3) are plotted in Figs. 26 and 27 respectively. From these figures, one can see that the voltages of these two capacitors are closely following their respective reference values.

Using the conventional control techniques, it can be seen that the current THD in case of PUC5 and PUC7 inverters, considering only the current control loop, are 6.58% and 4.66% respectively, while the current THD can be further reduced to 2.63% using two PI control loops (voltage and current control) as presented in Figs. 29–32.

In case of MPC, the current THD of PUC5 inverter is 2.62% as shown in Fig. 36 compared to the conventional PI control THD which is 6.58%. Similarly, the current THD of PUC7 inverter is 2.34% in Fig. 34 and that of PUC15 inverter is 0.59% in Fig. 38 which is systematically shown in Table 7 (see Figs. 28, 33, 35, 37 and 39).

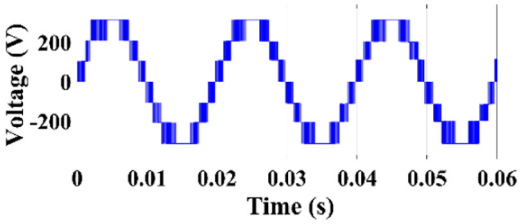

Fig. 10. PUC7 inverter voltage using a single PI control loop.

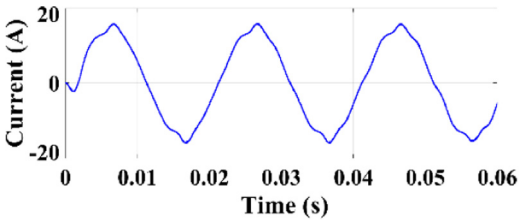

Fig. 11. Grid injected current of PUC7 inverter using a single PI control loop.

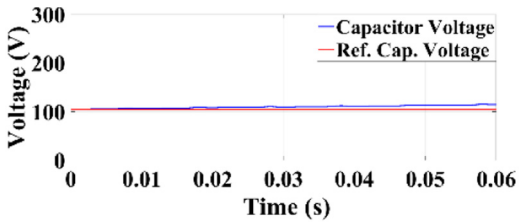

Fig. 12. Capacitor voltage of PUC7 inverter using a single PI control loop.

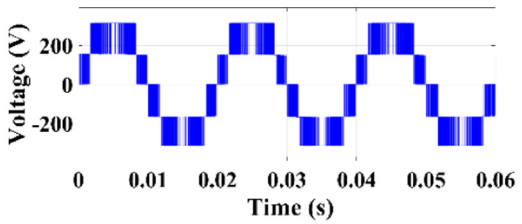

Fig. 13. PI control of PUC5 inverter voltage.

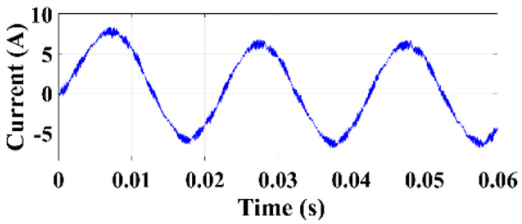

Fig. 14. PI control of grid injected current.

7. Hardware-in-loop (HIL) validations

To validate the MPC strategy on the PUC inverters, hardware in the loop (HIL) testing was performed using Typhoon HIL 402 hardware emulators. The MPC control was designed in Typhoon real-time simulator, which

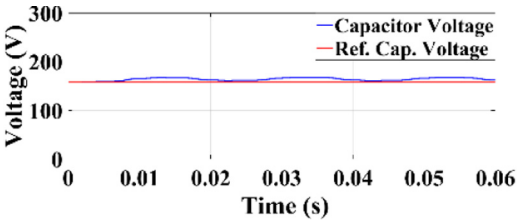

Fig. 15. PI control of measured Cap. voltage.

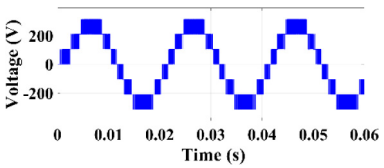

Fig. 16. PUC7 inverter voltage using cascaded PI control loops.

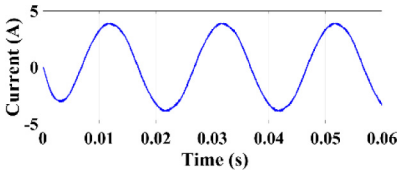

Fig. 17. Grid injected current of PUC7 using cascaded PI control loops.

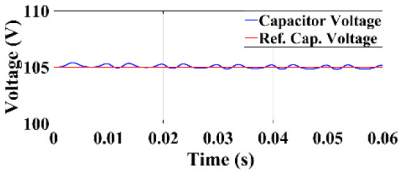

Fig. 18. Capacitor voltage of PUC7 inverter using cascaded PI control loops.

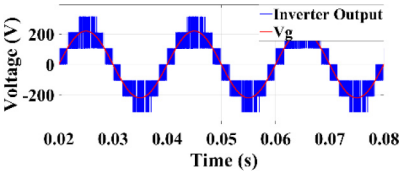

Fig. 19. PUC7 inverter voltage using MPC.

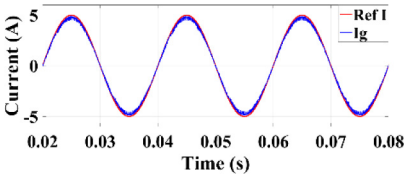

Fig. 20. Grid injected current of PUC7 inverter using MPC.

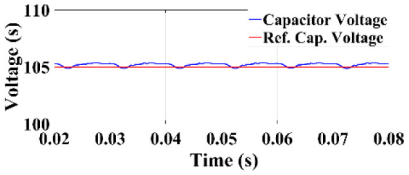

Fig. 21. Capacitor voltage of PUC7 using MPC.

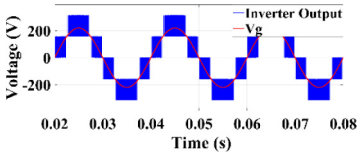

Fig. 22. PUC5 inverter voltage using MPC.

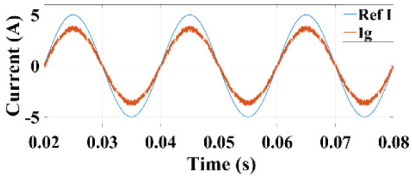

Fig. 23. Grid injected current of PUC5 inverter using MPC.

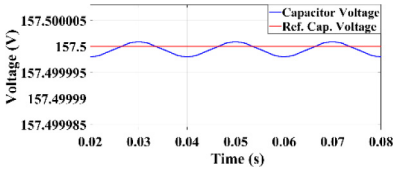

Fig. 24. Capacitor voltage of PUC5 using MPC.

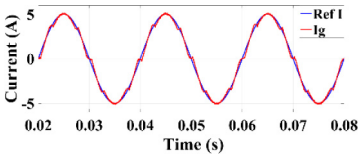

Fig. 25. Grid injected current of PUC15 inverter using MPC.

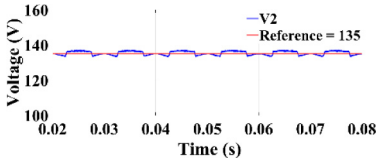

Fig. 26. Capacitor C_2 voltage of PUC15 using MPC.

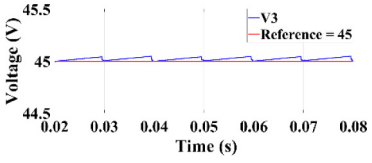

Fig. 27. Capacitor C_3 voltage of PUC15 using MPC.

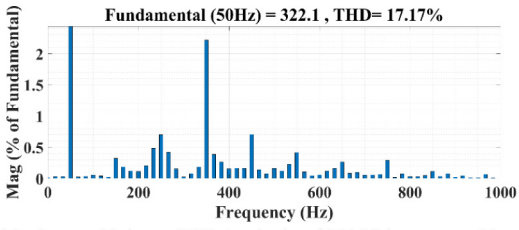

Fig. 28. Output voltage FFT analysis of PUC7 inverter — PI control.

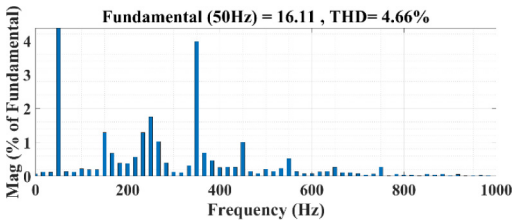

Fig. 29. Grid current FFT analysis of PUC7 inverter — PI control.

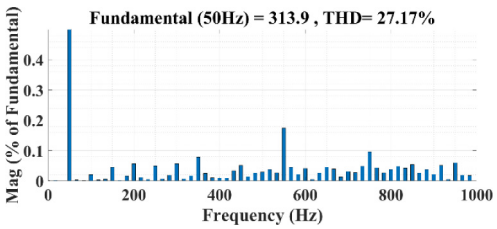

Fig. 30. Output voltage FFT analysis of PUC5 inverter — PI control.

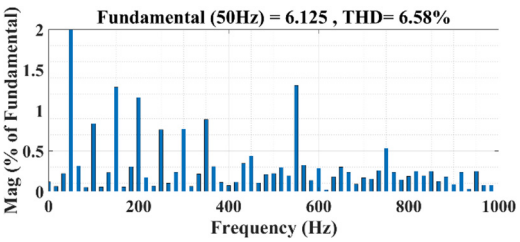

Fig. 31. Grid current FFT analysis of PUC5 inverter — PI control.

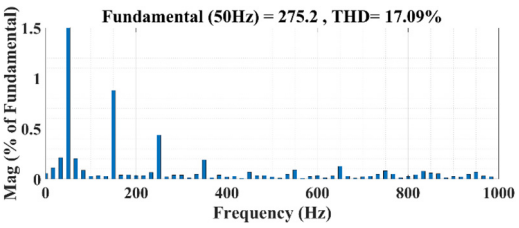

Fig. 32. Output Voltage FFT Analysis of PUC7 inverter (two loop control).

serves as an external physical controller in a HIL setup. PUC5 and PUC7 inverters were tested in HIL mode. the results of PUC5 are shown in Figs. 40–42. While the inverter output voltage of PUC5 inverter is demonstrated in

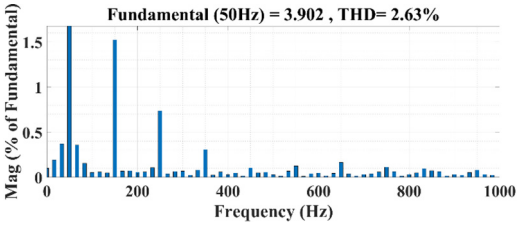

Fig. 33. Grid current FFT analysis of PUC7 inverter (two loop control).

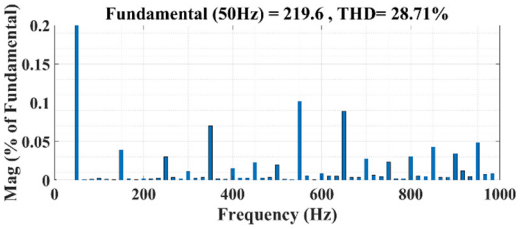

Fig. 34. Output voltage FFT analysis of PUC7 inverter — MPC.

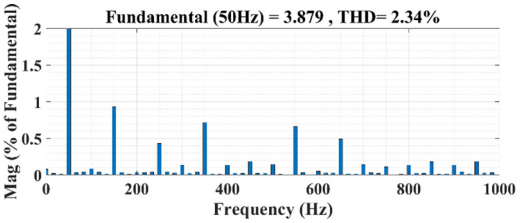

Fig. 35. Grid current FFT analysis of PUC7 inverter — MPC.

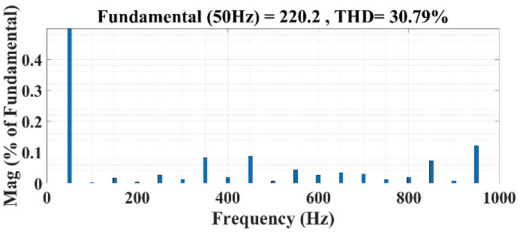

Fig. 36. Output voltage FFT analysis of PUC5 inverter — MPC.

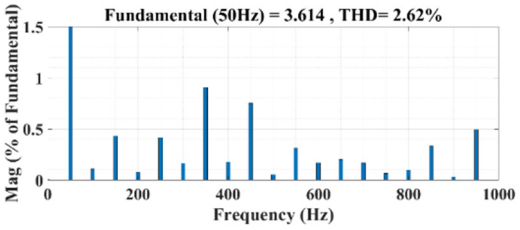

Fig. 37. Grid current FFT analysis of PUC5 inverter — MPC.

Fig. 40, the grid injected current of the same topology is shown in Fig. 41. These results agree with the simulation performed previously. Also, the capacitor voltage tracking is achieved by setting the reference voltage to 157.5

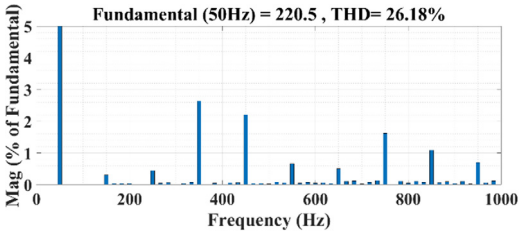

Fig. 38. Output voltage FFT analysis of PUC15 inverter — MPC.

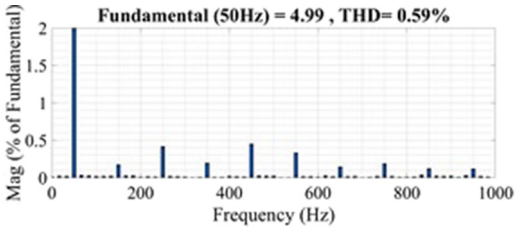

Fig. 39. Grid current FFT analysis of PUC15 inverter — MPC.

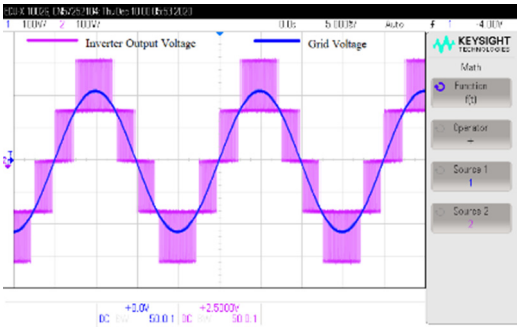

Fig. 40. PUC5 inverter and grid voltages using MPC.

Table 7. Comparison of different control techniques.

Control strategy	PUC levels	Voltage THD (%)	Current THD (%)
PI control	Five level	27.17	6.58
	Seven level	17.17	4.66
	Seven levels (Two control loop)	17.09	2.63
Model predictive control	Five level	30.79	2.62
	Seven level	28.71	2.34
	Fifteen level	26.18	0.59

V as presented in Fig. 42. Similarly, the results of PUC7 are drawn in Figs. 43–45. In these figures, the voltage and current waveforms are shown in agreement with previous simulation studies of this paper. Also, the capacitor voltage reference tracking is achieved by setting the reference voltage to 105 V as explained in Fig. 45.

8. Conclusions

The main purpose of this work is to present that MPC can be a better alternative to the classical PI control when applying such control techniques on different PUC topologies. Although MPC is known for its limitations in terms

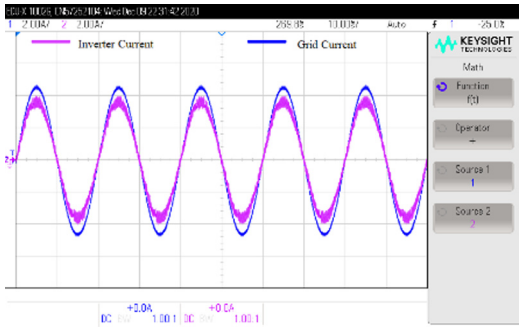

Fig. 41. Grid current and the inverter current of PUC5 inverter.

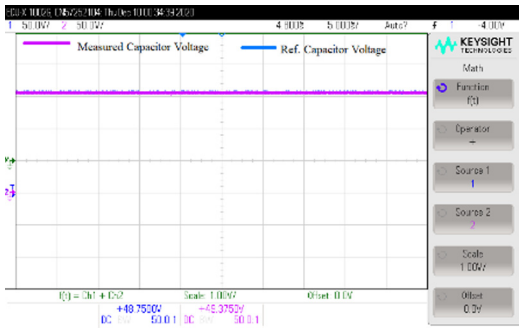

Fig. 42. Measured and reference capacitor voltage of PUC5 inverter.

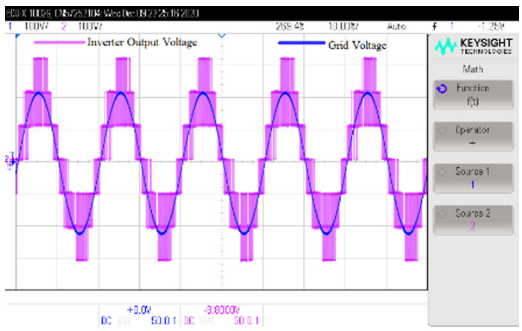

Fig. 43. PUC7 inverter and grid voltages using MPC.

of the steady-state error, MPC can be one of the greatest alternatives to the classical PI due to the simplicity of designing this control, the ability to achieve multiple objectives, and the high accuracy in transient conditions.

In this paper, MPC was successfully applied on five, seven and fifteen level PUC inverters and compared with PI control when applied on the same topologies. Although the converters' voltages usually have higher THD when MPC is applied, the easy implementation of MPC and the capability to control more than one control variables are the some of the advantages which increase the chances of using MPC in such applications.

In this work, using MPC, the capacitor voltages of the different PUC inverters were well regulated to follow their reference values using a single controller. However, in order to achieve similar performance using the classical PI control, two control loops, voltage and current control loops, were required to be designed which significantly increase the complexity of this control.

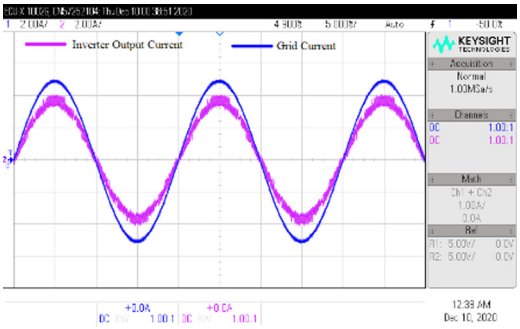

Fig. 44. Grid current and the inverter current of PUC7 inverter.

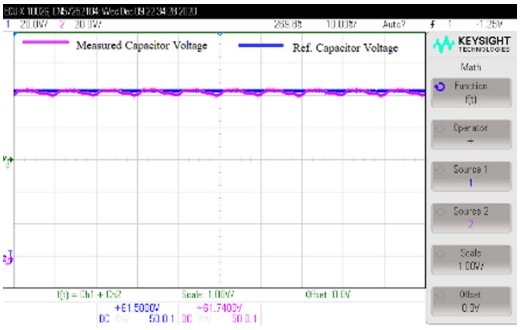

Fig. 45. Measured and reference capacitor voltage of PUC7 inverter.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Funding

This work was funded by the Deanship of Scientific Research at Jouf University under grant No (DSR-2021-02-0394)

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