Improved NPC Inverters Without Short-Circuit and Dead-Time Issues

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***Abstract*—The traditional neutral point clamped (NPC) inverter has short-circuit problem. The risk of short-circuit can be decreased by using dead-time in the switching signals. However, the dead-time decreases the achievable output voltage and causes distortion in the waveforms. To overcome the short-circuit problem, dual-buck NPC (DB-NPC) and split-inductor NPC (SI-NPC) inverters have been researched. However, the voltage stress of the two external diodes in the DB-NPC inverter is higher. On the other hand, the SI-NPC inverter has a problem of generating huge voltage spikes in the dead-time, which can destroy the semiconductor devices. In addition, the SI-NPC inverter cannot provide reactive power. This article presents a family of NPC inverters consisting of single-phase, three-phase, and cascaded inverters. The proposed inverters have no short-circuit and dead-time issues, therefore no high voltage and current spikes are caused. Also, the dead-time in the switching signals can be minimized. As a result, the magnitude of the output waveforms can be increased, and quality can be improved. Unlike the DB-NPC inverter, the voltage stress of all the semiconductor in the proposed inverter is lower, and unlike the SI-NPC inverter the proposed inverter provides reactive power. In this article, the proposed three-level NPC inverter is analyzed, designed, and tested. The voltage stress of the semiconductor devices in the proposed inverter is half of the source voltage, whereas in the conventional DB-NPC inverter the voltage stress of the two external diodes is the source voltage. In addition to the aforementioned benefits, the proposed cascaded inverter reduces the total number of inductors. To verify the analysis, detailed simulation, and experimental results of the proposed three-level inverter with input voltage 640 V, output power 1.2 kW, and output voltage 220 Vrms are provided.**

***Index Terms*—Current spikes, diode voltage stress, inverter, magnetic volume, multilevel, voltage spikes.**

I. Introduction

THE traditional H-bridge inverter is shown in Fig. 1. The voltage stress on its switches is the input voltage $V_{\rm dc}$. Therefore, the H-bridge inverter is well suitable for low-voltage applications. In high-voltage applications [1] such as HVdc transmission [2], large motor drive [3], locomotive [4], solid-state transformers [5], and reactive power compensation [6], the multilevel inverters are preferred. Flying capacitor [7], neutral point clamped (NPC) [8], and cascaded inverters [9], [10] are the famous multilevel inverter topologies.

The flying capacitor inverters synthesize output voltage by adding voltages of the flying and dc-link capacitors. The NPC inverters synthesize output voltage by adding voltages of the dc-link capacitors. The cascaded inverters synthesize output voltage by adding voltages of the series-connected H-bridge cells. The cascaded inverters are highly modular and can reach a higher output voltage [11]. Also, they can bypass faulty cells [12]. The multilevel inverters have the advantages of lower switch voltage stress, lower switching losses, smaller output filter, better output waveforms, and lower electromagnetic interference (EMI) noise issues.

The multilevel inverters are also getting popular in low-voltage and low-power applications due to the possibility of obtaining lower common-mode voltage and higher efficiency over the H-bridge inverter. In [13], multilevel inverters have been discussed for the photovoltaic (PV) systems. In [14], a half-bridge three-level NPC inverter is compared with a half-bridge two-level inverter for PV applications. It is found in [14] that a lower leakage current and higher efficiency can be realized with the NPC inverter.

II. Three-Level Neutral Point Clamped Inverters

A. Traditional NPC Inverter

The traditional NPC inverter is shown in Fig. 2(a). The voltage stress on its every switch and diode is $V_{\rm dc}/2$. During the positive half-cycle of the output voltage ($v_o > 0$), S_2 is ON, S_4 is OFF, and S_1 and S_3 work in complementary fashion. When S_1 is ON then S_3 is OFF, and when S_1 is OFF then S_3 is ON. However, overlap between S_1 and S_3 can occur due to miss triggering, delays in electronics, and EMI noise. The overleap between S_1 and S_3 causes short-circuit through C_1 as shown in Fig. 3(a). For $v_o < 0$, S_3 is ON, S_1 is OFF, and S_2 and S_4 work in complementary fashion. The overlap between S_2 and

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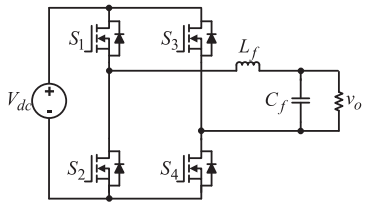

Fig. 1. H-bridge inverter.

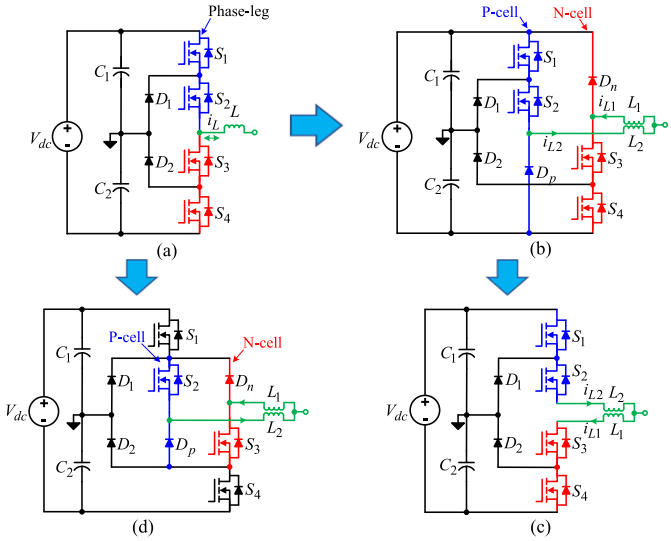

Fig. 2. Three-level NPC inverters. (a) Traditional NPC [8]. (b) DB-NPC [25], [27], [28]. (c) SI-NPC [30]. (d) Proposed.

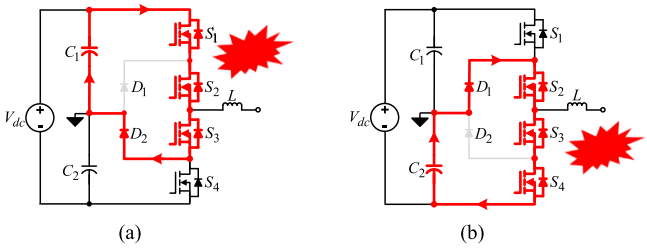

Fig. 3. Short-circuit in the NPC inverter. (a) $S_1 - S_3$ ON. (b) $S_2 - S_4$ ON.

S_4 causes short-circuit through C_2 as shown in Fig. 3(b). The short-circuit current destroys the semiconductor devices and is the main reliability killer [15]. To decrease the risk of short-circuit, dead-time in the switching signals is used. The dead-time guarantees safe operation. Although dead-time in a switching cycle is small but its effect is significant when accumulated for a complete line-frequency cycle. The output voltage magnitude and quality decrease with dead-time. It results in a momentary loss of control, and the output voltage deviates from the reference voltage [16].

The total harmonic distortion in the output waveforms increases with dead-time [17]. To overcome the dead-time issues, expensive hardwares and complicated compensators are used in industry [18]–[22]. The other approach to address the short-circuit problem in the voltage source inverters is to use the switching cell structure [23], [24]. There are two types of the switching cell, P-cell and N-cell as shown in Fig. 4. In each cell, a diode and a switch are connected in series. The center node of the P- and N-cells is connected to an inductor or current source. The phase-leg implementation with the switching cell structure is shown in Fig. 5.

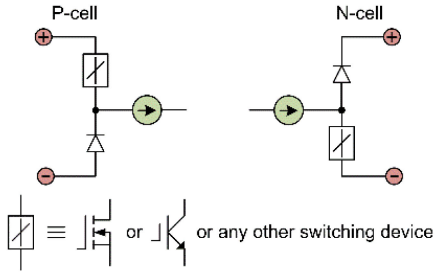

Fig. 4. Switching cells.

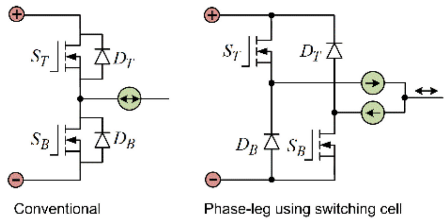

Fig. 5. Implementation of phase leg with switching cells.

To prevent short-circuit in the conventional inverters and converters, switching cells have been used in NPC inverters [25]–[30], flying capacitor inverters [31], cascaded inverters [32]–[35], cascaded ac–ac converters [36], H-bridge inverters [37]–[39], three-phase inverter [40], [41], buck–boost inverter [42], [43], and two-level ac–ac converters [44], [45].

B. Dual-Buck NPC Inverter

In [27]–[29], a systematic procedure for generating dual-buck topologies is presented. Fig. 2(b) shows the dual-buck NPC (DB-NPC) inverter [25], [27], [28]. It has been derived from the traditional NPC inverter by replacing its phase leg with the P- and N-cells. The DB-NPC inverter has no short-circuit risk, therefore dead-time in the switching signals can be eliminated. However, it requires two external diodes (D_p, D_n) of high-voltage stress. Its switch voltage stress same as the traditional NPC inverter is $V_{\rm dc}/2$, but the voltage stress on its external diodes (D_p, D_n) is $V_{\rm dc}$. The voltage stress of D_p and D_n remains $V_{\rm dc}$ irrespective of the number of levels of the inverter.

Thus, due to the high-voltage stress of its external diodes, the DB-NPC inverter losses the main benefit of the multilevel inverters which is the low-voltage stress on the semiconductor devices.

C. Split-Inductor NPC Inverter

Fig. 2(c) shows the split-inductor NPC (SI-NPC) inverter [30]. It is derived from the DB-NPC inverter by eliminating

D_p and D_n. In the SI-NPC inverter, switch S_2 and inductor L_2, and switch S_3 and inductor L_1 are connected in series. Due to the series connection of the switches and inductors, and its switching strategy, this inverter is suitable only for unity power factor operation. The SI-NPC inverter has dead-time problem. During the positive half cycle of the output current when S_2 is turned OFF, the inductor current (i_{L2}) drops instantly to zero. Similarly, during the negative half cycle of the output current when S_3 is turned OFF, the inductor current (i_{L1}) drops instantly to zero. As a result, huge voltage spikes are caused that destroy the semiconductor devices.

To address the issues of the conventional NPC inverters such as dead-time problem, short-circuit problem, high-voltage stress on diodes, and reactive power capability, this article presents a family of NPC inverters. Unlike the traditional NPC and SI-NPC inverters, the proposed NPC inverters have no short-circuit and dead-time problems. The proposed inverters can eliminate or minimize dead-time in the switching signals, as a result, the maximum available output voltage can be reached and distortion in the output waveforms can be decreased. Unlike the traditional DB-NPC inverters, the voltage stress on all semiconductor devices (diodes and switches) of the proposed inverters is lower. Therefore, low-voltage rating devices can be used in the proposed inverters. As a result, the cost can be reduced, and the proposed inverters can be operated with a high input voltage. Detailed theoretical analysis, operation principle, and comparative simulation results of the proposed three-level NPC inverter are provided. Finally, experimental results for 1.2-kW output power are reported.

III. Proposed Neutral Point Clamped Inverters

Fig. 2(d) shows the proposed three-level NPC inverter. The inner two switches S_2 and S_3 are replaced by the P and N switching cells.

The proposed inverter has no short-circuit and dead-time issues. The components count in the proposed and DB-NPC inverters is the same. However, the voltage stress on D_p and D_n of the proposed inverter is much lower. Fig. 6 shows the proposed m-level NPC inverter. Fig. 7 shows the proposed three-phase NPC inverter.

In the proposed inverters shown in Figs. 2(d) and 6, the voltage stress of D_p and D_n is $V_{\rm dc}/(m-1)$, where m is the number of levels of the inverter. In the DB-NPC inverter, the voltage stress of D_p and D_n is $V_{\rm dc}$. Fig. 8 compares the diode voltage stress of the proposed NPC and DB-NPC inverters. As shown, the voltage for the proposed inverter is much lower. For example, for a three-level inverter, the voltage stress of the proposed inverter is half of the conventional inverter, and for a 12-level inverter, the voltage stress of the proposed inverter is 11 times lower than of the conventional DB-NPC inverter.

Fig. 9 shows the proposed cascaded inverter. It connects the proposed single-phase NPC inverters in series. It inherits all the benefits of the proposed three-level inverter such as no short-circuit and dead-time issues in any cell and low-voltage stress on the semiconductor devices. In addition, it reduces the total number of inductors. An n-unit cascaded inverter based on

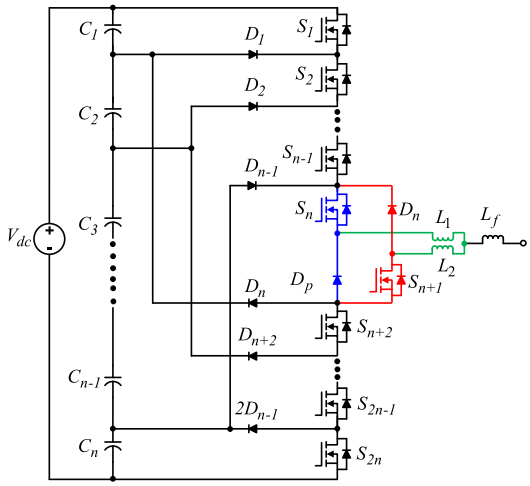

Fig. 6. Proposed m-level NPC inverter.

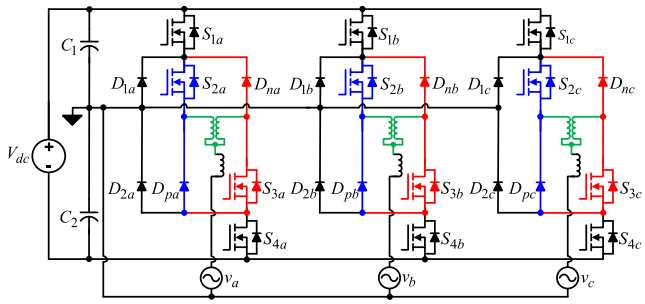

Fig. 7. Proposed three-phase NPC inverter.

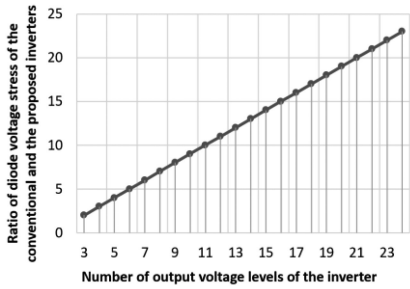

Fig. 8. Comparison of the diode voltage stress.

the DB-NPC inverter requires 4n current limiting inductors and an output filter inductor. The proposed n-unit cascaded inverter requires 2n+2 current limiting inductors and an output filter inductor. Therefore, the proposed cascaded inverter requires 2n−2 fewer inductors than the cascaded DB-NPC inverter. As a result, the soldering connections, footprints, magnetic cores, copper wires, and related losses can be decreased.

For example, a 2-unit cascaded DB-NPC inverter requires eight current limiting inductors, whereas the proposed inverter requires six inductors. A 6-unit cascaded DB-NPC inverter requires 24 inductors, whereas the proposed inverter requires 14 inductors.

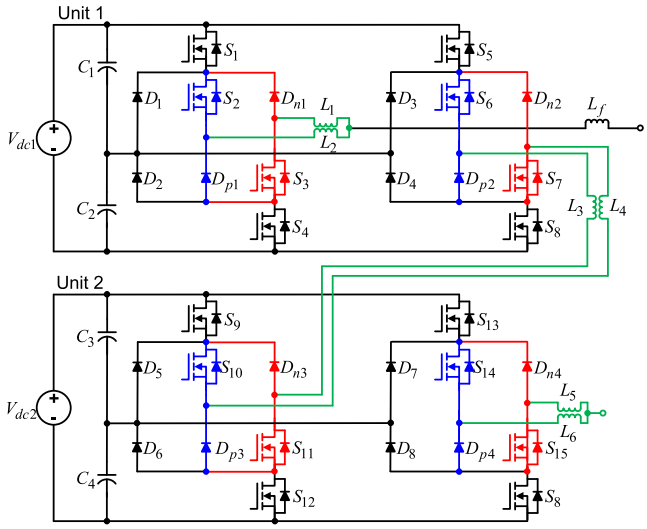

Fig. 9. Proposed cascaded NPC inverter with fewer inductors.

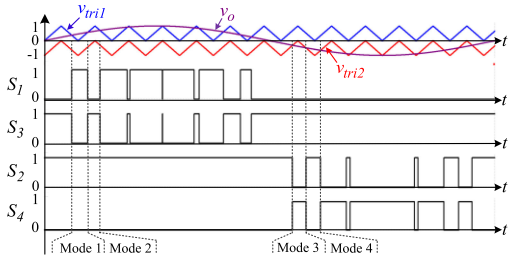

Fig. 10. Switching signals of the proposed three-level NPC inverter.

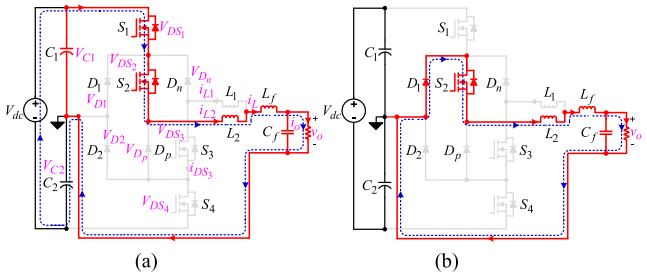

Fig. 11. Switching modes of the proposed NPC inverter for $v_o > 0,\ i_o > 0$. (a) Mode 1. (b) Mode 2.

IV. Operation of the Proposed Three-Level NPC Inverter

A. Normal Operation Modes When v_o and i_o are In-Phase

The switching signals of the proposed three-level NPC inverter are shown in Fig. 10. In a switching cycle, there are two switching modes. Mode 1 and 2 are for $v_o > 0$, and mode 3 and 4 are for $v_o < 0$.

Mode 1: In this mode, as shown in Fig. 11(a), switch $\boldsymbol{S}_1$ and $\boldsymbol{S}_2$ are ON and $\boldsymbol{S}_3$ and $\boldsymbol{S}_4$ are OFF. The inductor current increases

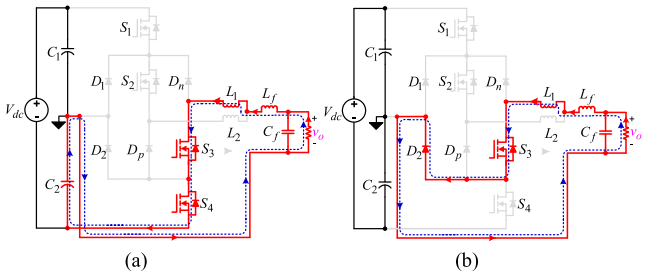

Fig. 12. Switching modes of the proposed NPC inverter for $v_o < 0,\ i_o < 0$. (a) Mode 3. (b) Mode 4.

with the slope given as

$$\frac{di_L}{dt} = \frac{0.5V_{\rm dc} - v_o}{L} \tag{1}$$

where $L = L_1 + L_f = L_2 + L_f$.

Mode 2: In this mode, as shown in Fig. 11(b), switch S_1 and S_4 are OFF and S_2 and S_3 are ON. The inductor current decreases with the slope given as

$$\frac{di_L}{dt} = \frac{-v_o}{L}. \tag{2}$$

Mode 3: In this mode, as shown in Fig. 12(a), switch S_3 and S_4 are ON, and S_1 and S_2 are OFF. The inductor current increases in the opposite direction with the slope obtained as

$$\frac{di_L}{dt} = -\frac{0.5V_{\rm dc} + v_o}{L}. \tag{3}$$

Mode 4: In this mode, as shown in Fig. 12(b), switch S_1 and S_4 are OFF, and S_2 and S_3 are ON. The inductor current decreases with the slope obtained as

$$\frac{di_L}{dt} = \frac{v_o}{L}. \tag{4}$$

B. Operation During the Overlap-Time

In the proposed inverter, the inductors L_1 and L_2 protect the short-circuit when $S_1 - S_3$ or $S_2 - S_4$ or $S_1 - S_4$ are turned-ON simultaneously as shown in Fig. 13. The slope of the current $i_{\rm sc}$ when $S_1 - S_3$ or $S_2 - S_4$ are turned-ON can be obtained from Fig. 13(a) and (b) as

$$\frac{di_{\rm sc}}{dt} = \frac{0.5V_{\rm dc}}{L_1 + L_2}. \tag{5}$$

The slope of the current $i_{\rm sc}$ when $S_1 - S_4$ are turned-ON simultaneously can be obtained from Fig. 13(c) as

$$\frac{di_{\rm sc}}{dt} = \frac{V_{\rm dc}}{L_1 + L_2}. \tag{6}$$

C. Operation During the Dead-Time

In the proposed inverter, even when all the switches are turned-OFF, the inductor currents flow smoothly. Therefore, no voltage spikes are caused. Fig. 14 shows the operation of the proposed inverter when $S_1 - S_4$ are OFF. For $i_o > 0$, diode D_p

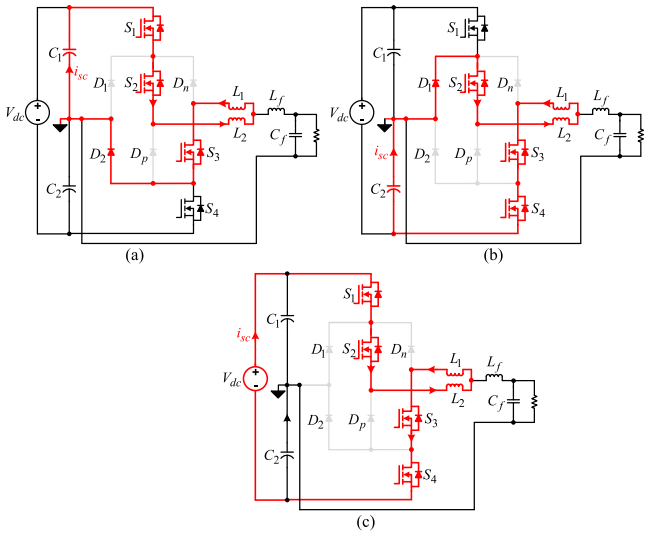

Fig. 13. Short-circuit protection in the proposed inverter. (a) $S_1 - S_3$ ON. (b) $S_2 - S_4$ ON. (c) $S_1 - S_4$ ON.

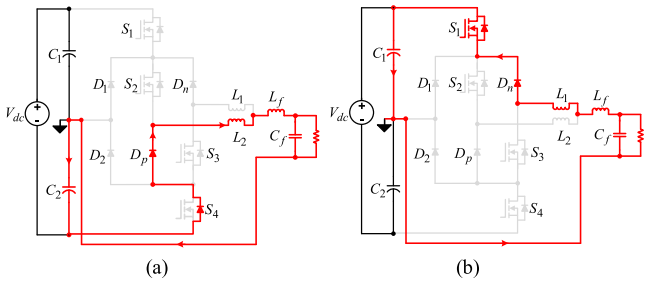

Fig. 14. Open-circuit protection in the proposed NPC inverter when all the switches are OFF. (a) $v_o > 0,\ i_o > 0$. (b) $v_o < 0,\ i_o < 0$.

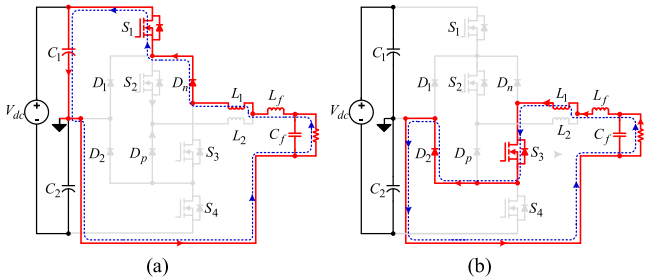

Fig. 15. Operation of the proposed NPC inverter when $v_o > 0,\ i_o < 0$. (a) Mode 1. (b) Mode 2.

ensures continuous inductor current flow, and for $i_o < 0$, diode D_n ensures continuous inductor current flow.

D. Nonunity Power Factor Operation

The operation modes of the proposed inverter when $v_o > 0$, and $i_o < 0$ are shown in Fig. 15. In mode 1, when S_1 is ON and S_3 is OFF, the inductor current freewheels through D_n and S_1 as shown in Fig. 15(a). In mode 2 when S_1 is OFF and S_3 is ON, the inductor current freewheels through S_3 and D_2 as shown in Fig. 15(b).

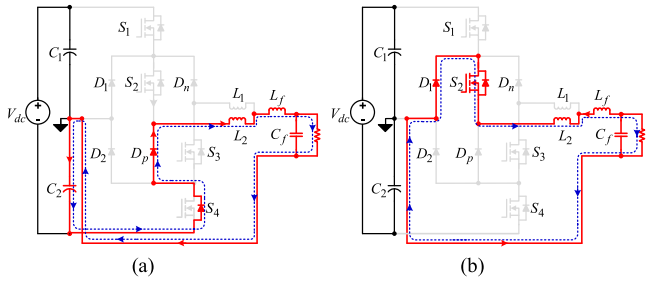

Fig. 16. Operation of the proposed NPC inverter when $\boldsymbol{v_o}\langle 0,\ \boldsymbol{i_o}\rangle 0$. (a) Mode 3. (b) Mode 4.

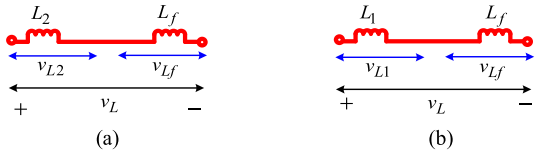

Fig. 17. Voltages across the inductors. (a) For $i_o > 0$. (b) For $i_o < 0$.

The operation modes of the proposed inverter when $v_o < 0$, and $i_o > 0$ are shown in Fig. 16. In mode 3, when S_2 is OFF and S_4 is ON, the inductor current freewheels through D_P and S_4 as shown in Fig. 16(a). In mode 4, when S_2 is ON and S_4 is OFF, the inductor current freewheels through S_2 and D_1 as shown in Fig. 16(b).

E. Selection of the Inductors

As shown in Fig. 17(a), for $i_o > 0$, the inductors L_2 and L_f are seen in series by i_o. The total voltage across L_2 and L_f is v_L. A part of v_L appears across L_2, and the rest of v_L appears across L_f. The voltage across the inductor L_2 is v_{L2} and the voltage across L_f is v_{Lf} as given by the following:

$$v_{L2} = v_L \frac{L_2}{L_2 + L_f} \tag{7}$$

$$v_{Lf} = v_L \frac{L_f}{L_2 + L_f}. \tag{8}$$

For $i_o < 0$, the inductors L_1 and L_f are seen in series by i_o as shown in Fig. 17(b). The total voltage across L_1 and L_f is v_L. A part of v_L appears across L_1 and the rest of v_L appears across L_f. The voltage across the inductor L_1 is v_{L1} and the voltage across L_f is v_{Lf} as given by the following:

$$v_{L1} = v_L \frac{L_1}{L_1 + L_f} \tag{9}$$

$$v_{Lf} = v_L \frac{L_f}{L_1 + L_f}. \tag{10}$$

As given by (7)–(10), the voltage across the inductors depends on their inductances. Note that the short-circuit protection depends on L_1 and L_2 as given by (5) and (6). The smaller L_1 and L_2 can decrease the overall magnetic volume but short-circuit may not be well protected. For example, if $L_1 = L_2 = 0$ and

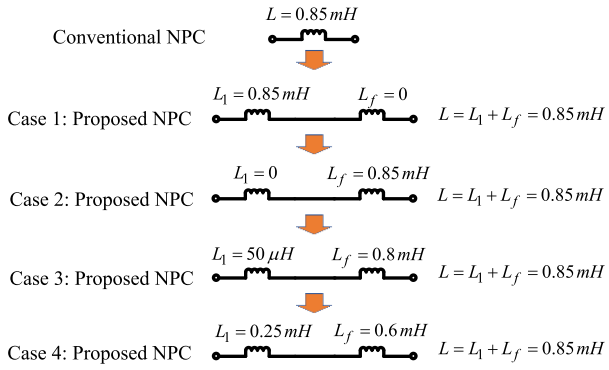

Fig. 18. Inductance values of the limiting inductors.

$L = L_f$, then the opposition to short-circuit is minimum. On the other hand, the larger L_1 and L_2 provide better protection against the short-circuit but results in increased overall magnetic volume. For example, if $L_1 = L_2 = L$ and $L_f = 0$, then the opposition to short-circuit is maximum. In this article, for a given slope of the short-circuit current in (6), L_1 and L_2 are obtained of 50 μH. Similarly, for a given slope of the output current in (1), L is found to be 0.85 mH. As $L = L_1 + L_f = L_2 + L_f$, therefore $L_f = 0.8$ mH. For $L_1 = L_2 = 50$ μH, and $L_f = 800$ μH, the voltage across the inductors L_1 and L_2 is $v_{L1} = v_{L2} = \frac{v_L}{17}$, and the voltage across the output inductor L_f is $v_{Lf} = \frac{16 v_L}{17}$.

As a result, the inductors L_1 and L_2 can be designed 17 times smaller than the main output filter inductor L_f.

The losses are not increased by the extra inductors in the proposed inverter because the overall inductance seen by the output current in the proposed inverter is same as in the conventional inverter. Assume that the inductance of the inductor (L) in the traditional NPC inverter is 0.85 mH, which has been split into smaller inductors in the proposed inverter as shown in Fig. 18. For example, in case 1, $L_f = 0$ and $L_1 = L_2 = L = 0.85$ mH. In case 2, $L_f = L = 0.85$ and $L_1 = L_2 = 0$. For all the cases, the inductance and therefore the conduction resistance seen by the output current is same as in the conventional NPC inverter.

V. Comparison of the Proposed and Conventional Inverters

A. Simulation Results With Dead-Time

A dead-time of 1 μs is set in the switching signals of all switches as shown in Fig. 19 to test the proposed and conventional inverters.

1) Traditional NPC Inverter: Fig. 19(a) shows the gate signals of $S_1 - S_4$, output inductor current i_L, and drain-source voltage (v_{DS_2}) of S_2 for the traditional NPC inverter. As shown the traditional NPC inverter works well with dead-time because in the dead-time the inductor current flows through the body diodes of switches.

2) Proposed NPC Inverter: Fig. 19(b) shows the simulation results of the proposed NPC inverter with 1 μs dead-time in the switching signals. The proposed inverter works well with dead-time because in the proposed inverter, the diodes D_p and D_n provide paths to inductor currents.

3) Traditional SI-NPC Inverter: Fig. 19(c) shows the simulation results of the SI-NPC inverter with 1 μs dead-time in the switching signals. In the SI-NPC inverter, the inductor current i_{L2} drops instantly to zero when S_2 is OFF during the positive half-cycle of the output current. Similarly, i_{L1} drops to zero instantly when S_3 is OFF during the negative half-cycle of the output current.

Therefore, the SI-NPC inverter suffers from the dead-time problem which causes huge voltage spikes that can damage the semiconductor devices.

B) Simulation Results With Overlap-Time

An overlap-time of 1 μs is set in the switching signals of all switches as shown in Fig. 20 to test the proposed and conventional inverters with a short-circuit fault.

1) Traditional NPC Inverter: Fig. 20(a) shows the gate signals of $S_1 - S_4$, output inductor current i_L, and drain-source current (i_{DS_3}) of S_3. In the traditional NPC inverter, during the overlap-time, the input voltage source gets short-circuited, therefore huge current spikes are caused, which can destroy the semiconductor devices. The overlap-time (short-circuit) is the main reliability killer in the traditional inverters.

2) Proposed NPC Inverter: Fig. 20(b) shows the simulation results of the proposed NPC inverter with a 1 μs overlap-time in the switching signals. As shown, the proposed inverter works well with overlap-time because in the proposed inverter, the inductors L_1 and L_2 protect short-circuit. Therefore, during the overlap-time, no switch current spikes are produced.

3) Traditional SI-NPC Inverter: Fig. 20(c) shows the simulation results of the SI-NPC inverter with 1 μs overlap-time in the switching signals. Like the proposed NPC inverter, the SI-NPC inverter has no short-circuit problem.

A detail comparison of the proposed and conventional three-level inverters is given in Table I. The DB-NPC inverter has high-voltage stress on D_p and D_n. The traditional NPC inverter requires dead-time in the switching signals to decrease the risk of short-circuit. The dead-time decreases the magnitude of the output waveforms and causes distortion. The dead-time limits the switching frequencies, and to achieve the same output voltage as the proposed inverter, the input voltage of the traditional NPC inverter should be increased, which increases the voltage and current stresses. Compared to the SI-NPC inverter, the proposed inverter can provide reactive power and does not generate any voltage spikes during the dead-time.

Table II shows the main advantages of the proposed cascaded inverter over the cascaded DB-NPC inverter, where *n* is the number of cascaded units.

The power loss of the proposed inverter is calculated for the unity power factor in the thermal module of PSIM as given in Fig. 21. The parameters for power loss distribution are given in Tables III and IV. The data is extracted from the datasheets and experiments to model the components in the thermal module. For unity power factor operation, the diodes D_p and D_n do not conduct, therefore their losses are negligible. The diodes D_p and

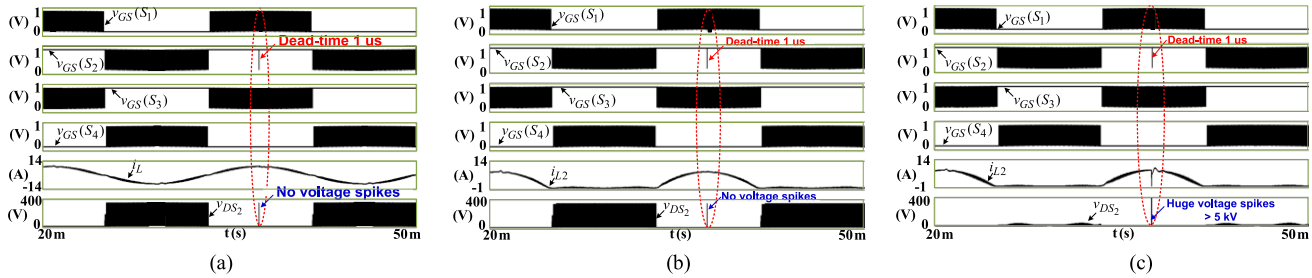

Fig. 19. Simulation results with a dead-time in the switching signals. (a) Traditional NPC inverter. (b) Proposed NPC inverter. (c) SI-NPC inverter in [30].

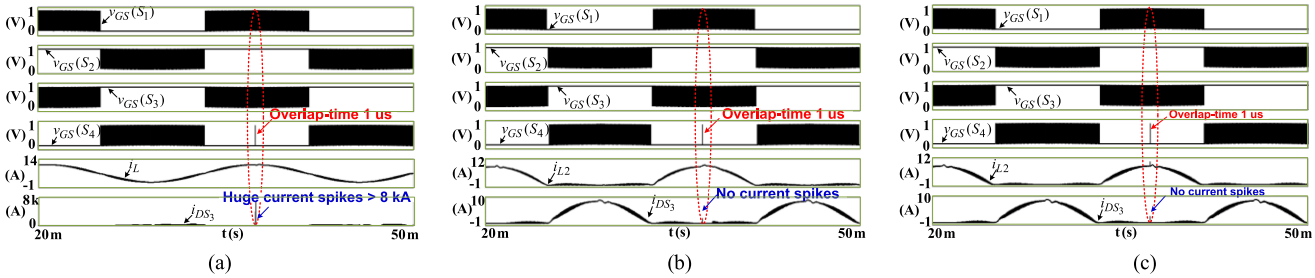

Fig. 20. Simulation results with an overlap-time in the switching signals. (a) Traditional NPC inverter. (b) Proposed NPC inverter. (c) SI-NPC inverter in [30].

TABLE I
COMPARISON OF THE PROPOSED AND CONVENTIONAL THREE-LEVEL NPC INVERTERS

	Traditional	DB-NPC	SI-NPC	Proposed
Generate high voltage spikes during overlap-time?	Yes	No	No	No
Generate high voltage spikes during dead-time?	No	No	Yes	No
Reactive power flow operation?	Yes	Yes	No	Yes
No of inductors	1	2 or 3	2	2 or 3
No of diodes	2	4	2	4
No of switches	4	4	4	4
Voltage stress of D_p and D_n	-	V_{dc}	-	$V_{dc}/2$
Voltage stress of D_1 and D_2	$V_{dc}/2$	$V_{dc}/2$	$V_{dc}/2$	$V_{dc}/2$
Voltage stress of switches	$V_{dc}/2$	$V_{dc}/2$	$V_{dc}/2$	$V_{dc}/2$
Current stress	I_o	I_o	I_o	I_o
Generation of high leakage current?	No	No	No	No
High voltage operation?	Yes	No	Yes	Yes

TABLE II
ADVANTAGES OF THE PROPOSED CASCADED INVERTER OVER THE DUAL-BUCK CASCADED INVERTER

	Proposed	Dual-Buck
No of current limiting inductors	2n+2	4n
Diode voltage stress	$V_{dc}/2$	V_{dc}

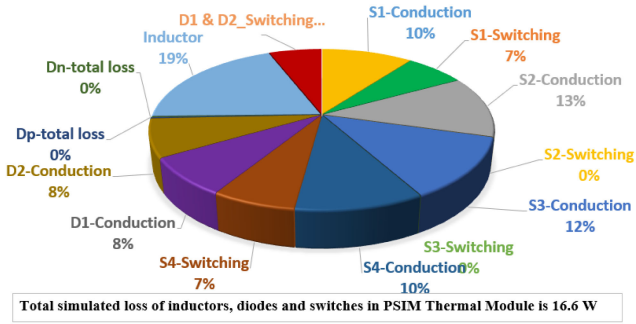

Fig. 21. Simulated power loss in thermal module of PSIM for $P_o = 1.2$ kW, $V_{\text{in}} = 640$ V, and $v_o = 220$ V_{rms}.

D_n conduct for the nonunity power factor operation and during the dead-time. The switching loss of S_2 and S_3 are negligible because they conduct the line-frequency current as shown in Fig. 20(b).

Although the proposed inverter requires two extra freewheeling diodes and two smaller inductors, the freewheeling diodes are cheap. The cost of RHRG3060 could be as low as \$0.86. The proposed inverter reduces the dead-time in the switching signals. As a result, for the same input voltage and duty ratio, the proposed inverter generates a higher output voltage than the conventional NPC inverter. Thus, to achieve the same output voltage as the proposed inverter, the input dc voltage for the conventional inverter must be increased which elevates the voltage and current stresses. As a result, high-voltage and current rating capacitors, switches, diodes, inductors, connecting wires, and PCB layout are required, which add extra cost and size. In addition, the overall power losses increase which could put extra burden on the

TABLE III
PARAMETERS FOR POWER LOSS DISTRIBUTION

Power MOSFET S1-S4	47N60CFD
Power Diode D1-D4	RHRG3060
Conduction resistance of inductors seen by current at a time (L1+Lf=L2+Lf)	56 $m\Omega$

TABLE IV
PARAMETERS OF THE EXPERIMENTAL PROTOTYPE

Parameter	Symbol	Value
DC-bus voltage	V_{dc}	640 V
Current limiting inductors	L_1, L_2	50 μH
Output main inductor	L_f	0.8 mH
Switching frequency	f_{sw}	30 kHz
Line-frequency	f	60 Hz
Rated output voltage	v_o	220 Vrms
MOSFETs	S_1-S_4	47N60CFD
Output capacitor	C_f	6.8 μF
Diodes	D_1, D_2, D_3, D_4	RHRG3060
Rated output power	P_o	1.2 kW

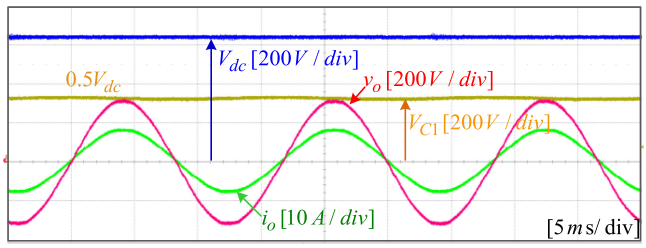

Fig. 22. Experimental waveforms of the input and output voltages and output current.

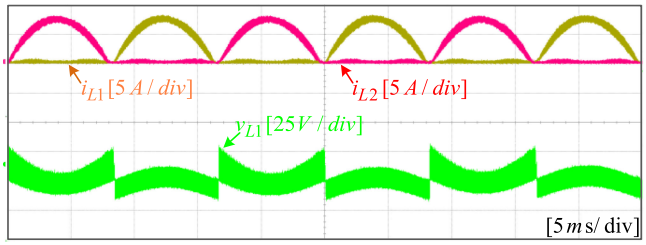

Fig. 23. Experimental waveforms of the inductor currents and voltage.

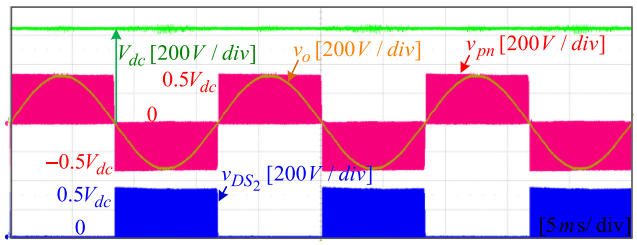

Fig. 24. Experimental results of the input voltage ($\boldsymbol{V_{dc}}$), output voltage ($\boldsymbol{v_o}$), drain-source voltage ($\boldsymbol{v_{DS_3}}$) of switch $\boldsymbol{S_3}$, and voltage ($\boldsymbol{v_{pn}}$).

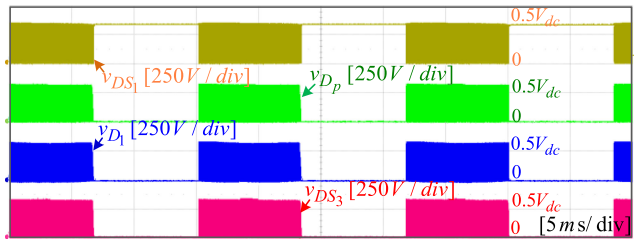

Fig. 25. Experimental waveforms of the drain-source voltage ($\boldsymbol{v_{DS_1}}$) of switch $\boldsymbol{S_1}$, drain-source voltage ($\boldsymbol{v_{DS_3}}$) of switch $\boldsymbol{S_3}$, voltage $\boldsymbol{v_{D_p}}$ across diode $\boldsymbol{D_p}$ and voltage $\boldsymbol{v_{D_1}}$ across diode $\boldsymbol{D_1}$.

heatsinking requirements. As the proposed inverter eliminates the dead-time, therefore better output waveforms can be generated. On the other hand, the traditional NPC inverter requires dead-time in the switching signals which causes high distortion in the output waveforms. As a result, the size of the output filter in the traditional NPC inverter could be larger. The dead-time limits the switching frequencies. The proposed inverter does not require dead-time; therefore, it could be operated at higher switching frequencies for the reduction of passive components size.

VI. EXPERIMENTAL RESULTS

To verify the operation of the proposed three-level inverter, a 1.2-kW hardware prototype was fabricated and tested successfully. Table IV shows the parameters of the prototype. The inductance of L_1 and L_2 is 50 μH, and L_f is 0.8 mH. For L_1 and L_2, the toroidal core (CM400173) available in the authors laboratory is used.

Fig. 22 shows the experimental waveforms of the input voltage ($V_{\rm dc}$), output voltage (v_o), dc-link capacitor voltage (V_{C1}), and output current (i_o). As shown, the output sinusoidal waveforms are generated with less distortion because the proposed inverter does not require dead-time in the switching signals. Fig. 23 shows the experimental waveforms of the currents i_{L1} and i_{L2} through the inductors L_1 and L_2, and voltage v_{L1} across L_1. The inductor currents are unidirectional positive, therefore no current flows through the antiparallel diodes of S_2 and S_3. The current freewheels through the external diodes D_p and D_n, which can decrease the reverse recovery loss.

Fig. 24 shows the waveforms of $V_{\rm dc}$, v_o, drain-source voltage of switch S_2 ($v_{\rm DS_2}$), and voltage v_{pn}, where v_{pn} is the voltage between the drain of S_2 and neutral point. The voltage v_{pn} has three levels $-V_{\rm dc}/2$, 0 and $V_{\rm dc}/2$. The output ac voltage is obtained by filtering v_{pn} through the inductors and the output filtering capacitor C_f.

Fig. 25 shows the drain-source voltage $v_{\rm DS_1}$ and $v_{\rm DS_3}$ of switch S_1 and S_3, and voltage v_{D_p} and v_{D_1} across the diode D_p and D_1, respectively. As shown, the voltage stresses of all the semiconductor devices are half of input dc voltage. Fig. 26 compares the voltage stress of the diode D_p in the proposed and conventional DB-NPC inverters. As shown, the voltage stress of the diode D_p in the proposed inverter is half of that in the conventional inverter.

Fig. 27 shows the gate-source voltage switching signals ($v_{\rm GS_1} - v_{\rm GS_4}$) of switch $S_1 - S_4$, respectively, and the inductor current i_{L1}. An overlap-time of 1 μs is inserted in the switching signals to observe the performance of the proposed inverter.

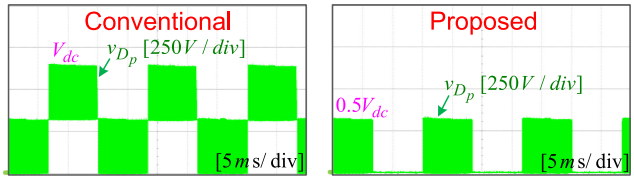

Fig. 26. Experimental waveforms of the diode voltages of the proposed NPCI and conventional DB-NPCI.

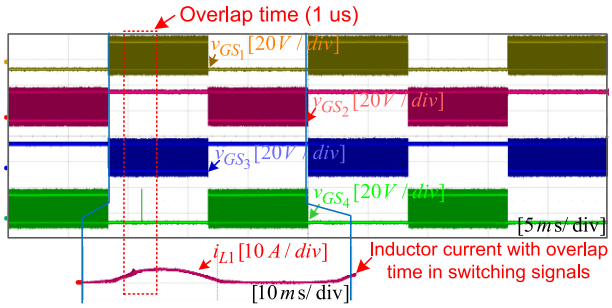

Fig. 27. Experimental waveforms of the switching signals and inductor current with overlap-time of 1 μs in the switching signals.

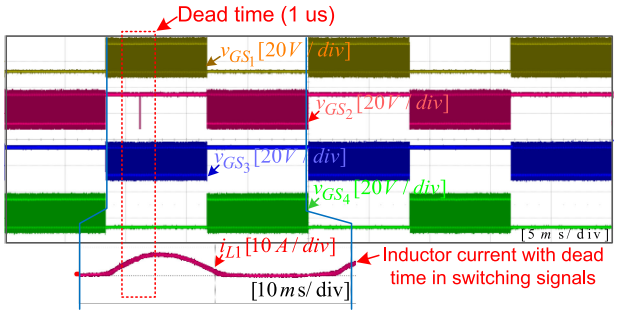

Fig. 28. Experimental waveforms of the switching signals and inductor current with dead-time of 1 μs in the switching signals.

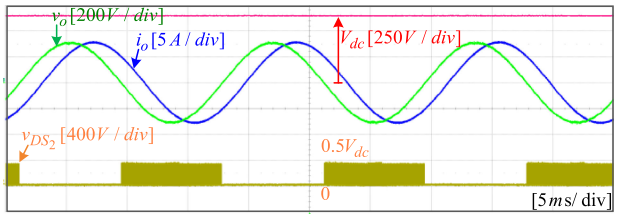

Fig. 29. Experimental waveforms with a partially inductive load.

The inverter works well with the overlap-time without short-circuiting or shoot-through current. Fig. 28 shows $v_{\mathrm{GS}_1} - v_{\mathrm{GS}_4}$ and the inductor current i_{L1}. A dead-time of 1 μs is inserted in the switching signals to observe the performance of the proposed inverter. The inverter works well with the dead-time without generating voltage spikes.

Fig. 29 shows the experimental waveforms of the proposed inverter with a partially inductive load consisting of load resistance $R_L = 40\,\Omega$, and load inductance $R_L = 100$ mH. Fig. 30

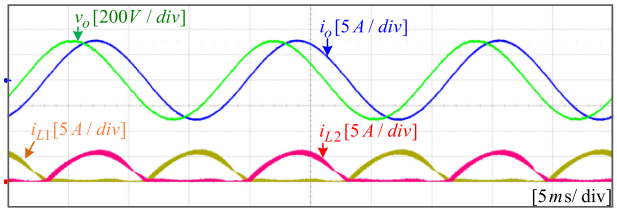

Fig. 30. Experimental waveforms of the inductor currents with a partially inductive load.

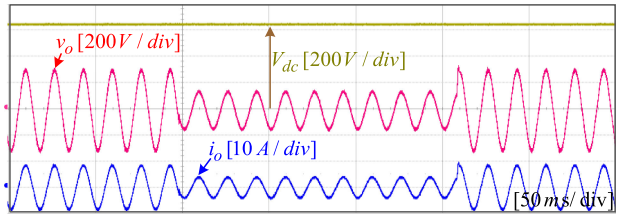

Fig. 31. Dynamic experimental waveforms for a step change in output voltage.

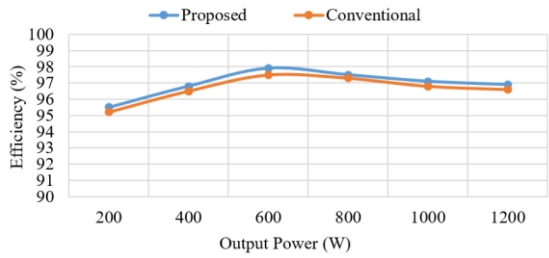

Fig. 32. Power efficiency of the proposed and conventional inverters at, $v_o = 220\ \mathrm{V_{rms}}$, and $f_{\mathrm{sw}} = 30$ kHz.

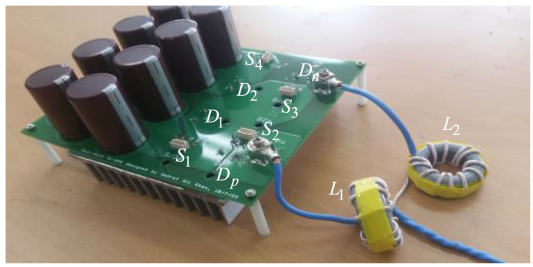

Fig. 33. Photograph of the hardware prototype.

shows the experimental waveforms of the inductor currents and output current and voltage with a partially inductive load. Fig. 31 shows the dynamic results when the output voltage is step changed from 220 to 110 $\mathrm{V_{rms}}$ and back from 110 to 220 $\mathrm{V_{rms}}$. The efficiencies of the proposed and conventional inverters are compared in Fig. 32. The efficiency of the conventional is lower because smaller dead-time is used in the switching signals of the proposed inverter, whereas 1 μs dead-time is used in the switching signals of the conventional inverter to avoid short-circuit. The dead-time decreases the output voltage of the conventional inverter. To achieve the same output voltage as the proposed inverter, the input dc voltage of the conventional

inverter is increased, which increases the power loss. A photograph of the hardware prototype of the proposed inverter is shown in Fig. 33.

VII. Conclusion

This article presented new types of single-phase, three-phase, and cascaded NPC inverters. The proposed inverters have no short-circuit risk. The dead-time in the switching signals can be reduced. As a result, the distortion in the output waveforms can be decreased, higher switching frequencies can be used for the passive components size reduction and maximum available output voltage gain can be reached. Unlike the conventional SI-NPC inverters, the proposed inverters do not generate high-voltage spikes in the dead-time and provide reactive power. Unlike the DB-NPC inverters, the voltage stress of all the external diodes in the proposed inverter is lower. The proposed cascaded inverter inherits all the features of the proposed three-level inverter. In addition, it reduces the number of inductors by sharing the inductors between the cascaded units.

A 1.2-kW hardware prototype was fabricated and tested with various loads at the input voltage 640 V, output voltage 110/220 V_{rms}, output power 1.2 kW, line-frequency 60 Hz, and switching frequency 30 kHz. The experimental results verified that the proposed inverter could generate good output waveforms, provide reactive power, works with dead and overlap-times, and obtains higher efficiency.

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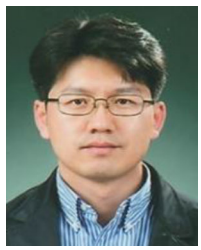

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