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# Performance Analysis of Reliability-Based Decoding Algorithm for Short Block Length Turbo Codes

P. Salija<sup>1</sup>, B. Yamuna<sup>1</sup>, T. R. Padmanabhan<sup>1</sup> and Deepak Mishra<sup>2</sup>

<sup>1</sup>Department of Electronics and Communication Engineering, Amrita School of Engineering, Coimbatore, Amrita Vishwa Vidyapeetham, India;

<sup>2</sup>Digital Communication Division (DCD), Optical and Digital Communication Group (ODCG), Satcom & Navigation Payload Area (SNPA) Space Application Centre (SAC), ISRO, Ahmedabad, India

## ABSTRACT

Demand for transmission using short block length messages has been increased recently in applications including satellite communication, mobile communication, wireless sensor networks, and machine type communications. Unacceptable performance degradation associated with the short block length Turbo codes restricted its use for applications requiring communication with short block length codewords. A novel performance improved reliability-based decoding algorithm for short block length Turbo codes has been formulated and proposed by the authors. The proposed algorithm has a coding gain of 2.45 dB at a BER of  $10^{-3}$  over AWGN channel with BPSK modulation for a code rate of  $\frac{1}{4}$ . The algorithm has a channel adaptive complexity and has shown nearly 82% reduction in the decoding time complexity for the rate  $\frac{1}{4}$  Turbo code at 3 dB SNR. As an extension of this earlier work, a detailed performance analysis of the algorithm on different Turbo codes has been carried out. A four-state Turbo encoder has been used to bring out the key aspects of the level based algorithm which is driven by reliability as the key parameter. The formulated algorithm has been applied to different Turbo encoder structures namely 3GPP LTE and CCSDS Turbo codes and a detailed analysis has been carried out in this paper. Simulation results show a significant improvement in the error correction performance of short block length Turbo codes. The algorithm also leads to a marked improvement in time complexity at high SNRs. The algorithm is an attractive solution for applications requiring communication with short block lengths.

## KEYWORDS

Bit error rate; Check equation (CE); Decoding; Performance analysis; Reliability; Turbo codes

## 1. INTRODUCTION

Achieving optimal error correction capability and computational complexity is one of the major challenges in wireless communication. Turbo codes have shown near Shannon capacity approaching performance for longer codeword lengths [1,2]. Iterative Turbo decoder which uses MAP or its variants like Log-MAP or Max-Log-MAP as the constituent decoder performs a fixed number of iterations irrespective of the channel conditions and information block size [3]. The BER performance of Turbo codes flattens in moderate to high SNR regions and the same does not improve even with a large number of iterations. This phenomenon is called as “error floor” [4]. Applications like satellite uplink, real-time communication, machine to machine communication, and mobile communication require transmission with short block length Turbo codes [5,6]. The capacity approaching Turbo codes fail to offer acceptable performance when dealing with short block length codewords due to the high error floor and unacceptable coding gain degradation [7,8]. Dynamic channel conditions introduce varying levels of errors during the transmission.

The number of errors introduced also varies according to the channel conditions and hence it is necessary to vary the error correction level accordingly, rather than providing a constant level of error correction at all channel conditions.

Emergent applications requiring communication of data with short units have increased the interest in short to medium block length Turbo codes [9–13]. Transmission over the telecommand links for satellite communication requires data typically in the range of 100 bits [14]. Ultra-low latency and ultra-reliability are the two stringent requirements of future cellular communications. Low latency requirements necessitate the use of short block length codes in wireless communication. Capacity approaching channel codes are designed to meet the requirement of longer information frame size [15]. Iterative Turbo decoders are not suitable in such scenarios and the design of short block length decoding algorithm with optimum performance in terms of error correction and computational complexity is still an open problem.

Efforts to improve the performance of short block length Turbo codes have been reported in literature. Reliability-based soft-decision decoding methods reported in literature have shown coding gain improvement for short to moderate length codewords [16]. Reliability value of a received bit indicates its certainty and hence decoding with reliability information gives improved error correction performance. Most of the reliability-based Turbo decoders take advantage of ordered statistics decoding (OSD) algorithm along with the iterative process [6,7,17,18]. The methods reported in literature have considered LLR values of each bit as reliability information. Once the iterative process is completed, reliability-based decoder performs OSD or flip and check, or CRC check [4,6,19,20]. This results in additional computational complexity and decoding delay. None of the reported methods guarantee the complete elimination of error floor at high SNRs. Thus iterative reliability-based Turbo decoder is not suitable for applications involving short block length Turbo codes.

A novel performance-enhanced reliability-based decoding algorithm for short block length Turbo codes has been proposed recently [21]. The method shows significant performance enhancement in terms of error correction and channel adaptive complexity for short block length Turbo codes. The performance-enhanced algorithm makes use of the encoder structure and the reliability information available at the output of the demodulator. An equation called ‘‘Check Equation (CE)’’ – derived from the encoder structure forms the heart of the decoding algorithm. The decoding algorithm is a level based algorithm; starting with the hard decoded sequence, the algorithm progressively forms the most likely erroneous branches. At every level, it retains only the most probable error combinations from the set of all possible error combinations.

Turbo encoder with 3GPP LTE and CCSDS specifications have been considered for most of the wireless communication applications. The efficiency of the performance-enhanced reliability-based decoding algorithm has been brought out using 3GPP LTE and CCSDS Turbo encoder configurations. To facilitate the performance analysis – in terms of error correction and decoding complexity – of the algorithm with different Turbo codes, a unique CE corresponding to each Turbo encoder is derived in this paper. Simulation results have shown significant improvement in error correction performance with an acceptable decoding complexity. The paper is organized as follows: Section 2 gives the brief outline of the novel performance-enhanced reliability-based decoding algorithm. Section 3 deals

with the formulation of CE and level based decoding with 3GPP LTE and CCSDS Turbo codes. Results are presented in Section 4, followed by conclusions in Section 5.

## 2. PERFORMANCE ENHANCED RELIABILITY BASED DECODING ALGORITHM FOR SHORT BLOCK LENGTH TURBO CODES

The concept of novel performance-enhanced reliability-based decoding algorithm for short block length Turbo codes has been proposed recently [21]. The basic algorithmic formulation that has been established can be applied on different Turbo codes. The decoder selects the most probable solution candidate from the set of all possible solution candidates. The decoding process is driven by the unique CE associated with each Turbo code and the corresponding reliability values. Reliability value of each received bit is computed as cumulative distribution function (CDF) of normal distribution by making use of the received amplitude and noise variance noise variance ( $\sigma^2$ ) [22]. Once the reliability information is calculated, the updation process for received systematic bits is performed. The reduced reliability value – called Reliability Reduction Factor (RRF) as given by Equation (1) – is used in the decoding process.

$$RRF = \frac{1 - \text{Reliability value}}{\text{Reliability value}} \quad (1)$$

The CE – of Turbo codes – derived from the encoder structure uses a set of systematic and parity bits and forms the crux of the algorithm. CE formulation, for a specific – four state Turbo encoder with generator matrix  $G(D) = \left[ 1, \frac{1+D^2}{1+D+D^2} \right]$  as shown Figure 1, has been brought out in this section and the same procedure can be extended to derive CE associated with 3GPP LTE and CCSDS Turbo codes; the detailed description for the 3GPP LTE and CCSDS Turbo codes is presented in subsequent sections.

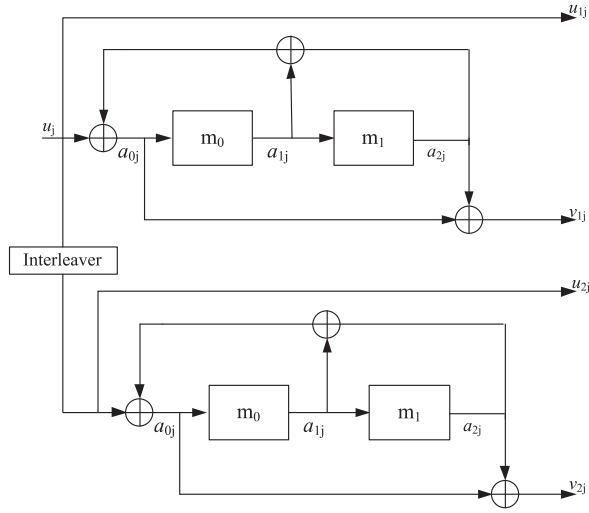
At  $j$ th time instant, the systematic output and parity output, of the constituent encoder as shown in Figure 1 are characterized by Equations (2) and (3),

$$u_j = a_{0j} + a_{1j} + a_{2j} \quad (2)$$

$$v_j = a_{0j} + a_{2j} \quad (3)$$

Combining Equations (2) and (3),

$$u_j + v_j = a_{1j} \quad (4)$$



**Figure 1:** Four-state Turbo encoder [14]

At  $(j-1)$ th instant Equation (4) can be written as

$$\begin{aligned} u_{j-1} + v_{j-1} &= a_{1j-1} \\ &= a_{2j} \end{aligned} \quad (5)$$

Since,  $a_{1j-1} = a_{2j}$

Similarly, at  $(j+1)$ th instant Equation (4) can be written as

$$\begin{aligned} u_{j+1} + v_{j+1} &= a_{1j+1} \\ &= a_{0j} \end{aligned} \quad (6)$$

Combining Equations (4), (5) and (6),

$$u_{j+1} + v_{j+1} + u_j + v_j + u_{j-1} + v_{j-1} = a_{0j} + a_{2j} + a_{1j}$$

and hence,

$$a_{1j} = u_{j+1} + v_{j+1} + u_j + u_{j-1} + v_{j-1} \quad (7)$$

From  $a_{1j}$  the rest of the state information can be derived as follows,

$$a_{0j} = u_{j+2} + v_{j+2} + u_{j+1} + u_j + v_j \quad (8)$$

$$a_{2j} = u_j + v_j + u_{j-1} + u_{j-2} + v_{j-2} \quad (9)$$

Equation (3) can be rewritten as

$$v_j + a_{0j} + a_{2j} = 0 \quad (10)$$

Substituting  $a_{0j}$  and  $a_{2j}$  in Equation (10) yields,

$$u_{j-2} + v_{j-2} + u_{j-1} + v_j + u_{j+1} + v_{j+2} + u_{j+2} = 0 \quad (11)$$

Equation (11) represents the CE corresponding to the Turbo encoder shown in Figure 1. It is clear from

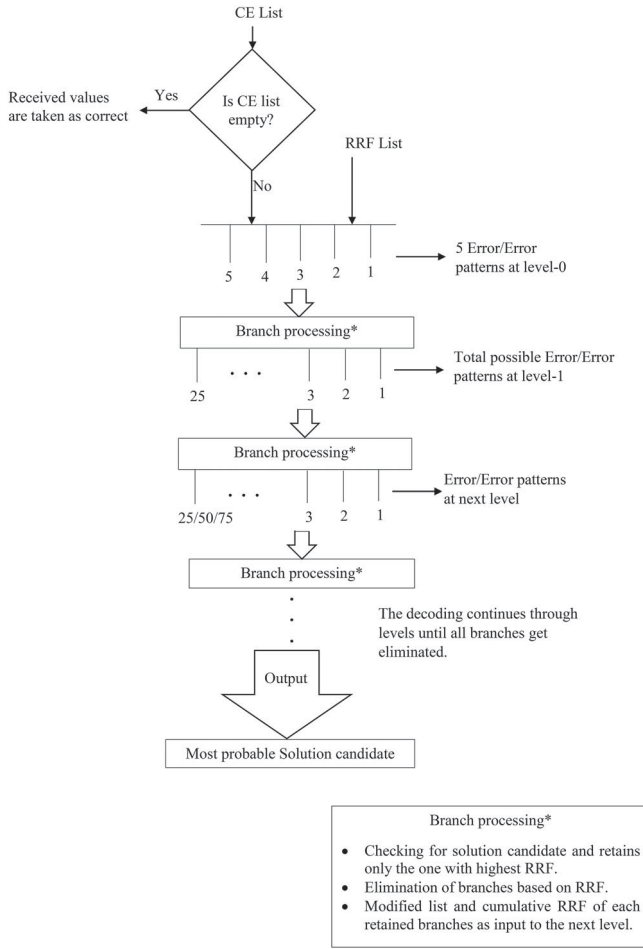
Equation (11) that the  $CE[j]$  depends on  $(u, v)$  values from the  $(j-2)$ nd time instant to  $(j+2)$ nd time instant. CE is defined for any  $(u, v)$  values in the range  $\{2, j-2\}$ .  $(N-4)$  CEs –  $CE[2]$  to  $CE[N-3]$  are possible for an  $N$  bit information sequence. CE at any  $j$ th instant is associated with a set of error/error patterns and the corresponding affected CE list. The reduced error/error patterns – consisting of single, double and triple error/error patterns – that totals to 5, and the associated affected CEs for the four-state Turbo encoder is shown in Figure 2. Each branch represents the error/error patterns and the corresponding affected CEs of  $CE[j-2]$ .

Equation (11) shows that the  $CE[j]$  depends on a sequence of  $(u, v)$  values for  $(j-2)$ nd to  $(j+2)$ nd time instant. In order to cover and correct all  $(u, v)$  values at the receiver side, it is necessary to prepend and append 4 zeros to the information message bits. The addition of zeros makes the total length as “ $N+8$ ” bits for an information bit sequence of length “ $N$ ”. In short “ $N+4$ ” CEs – ( $CE[2]$  to  $CE[N+5]$ ) – are possible with “ $N+8$ ” bits; this is necessary to correct all errors in the received codeword. The modified list becoming empty or the leading CE entry in the modified list becoming greater than  $(N+5)$  are the conditions for the solution candidate. The 12 bits (initial 4  $(u, v)$  bits and final 4  $u$  bits) are known at the receiver side and that results in fixing the corresponding RRF values as zero.

Once the updation process is completed, CEs for the entire sequence is formulated from the hard decision bits of received values. The indices of CEs with non-zero value lead to the formation of initial CE list. Once the initial list of CEs is formed, the leading entry formulates the entire error/error patterns. The modified list corresponding to each branch forms the input to the next level with associated cumulative RRF. At level-0, 5 branches are formulated and the leading entry of each retained modified list formulates error/error patterns in the next level. A maximum of  $5 \times 5$  branches are possible at level-1. The schematic diagram of the level based decoding process is shown in Figure 3. In a level, the empty modified

	Error patterns	Affected CEs
	$U_j$	$[j-2, j-1, j+1, j+2]$
	$V_j$	$[j-2, j, j+2]$
$CE[j-2]$	$U_{j-1}, V_{j-1}$	$[j-2, j-1, j]$
	$U_{j-3}, V_{j-3}, U_{j-2}$	$[j-2, j-1, j]$
	$U_{j-2}, V_{j-2}, V_{j-1}$	$[j-2, j+1]$

**Figure 2:** Error combination and affected CEs details for four state Turbo encoder



**Figure 3:** Outline of level-based decoding process

lists or primary entry in the modified list greater than the extreme CE index possible with the received data will be considered as a candidate solution. If any solution candidate occurs in further levels with RRF greater than the previous solution candidate, the previous entry is replaced with the new one, else the previous entry is retained as such. At each level, the algorithm processes all the generated error patterns and only the most probable ones are retained at each level by eliminating the branches as follows:

- Eliminate all branches with RRF value less than solution candidate's RRF if any.
- Eliminate all branches with RRF value as zero.
- If more than one branch with the same modified list occurs in any level, retain the one with highest RRF value.
- At each level, based on the RRF value, arrange error/error patterns in descending order and retain only first 25/50/75/100 branches as input to the next level.

Processing and elimination of branches, checking for the solution candidate are performed at each level. The

decoding process continues to the next level with the retained branches or stops if all the branches get eliminated. The path through the levels of the solution candidate give the indices of the erroneous bits. The decoding process is completed by inverting the bits in the positions indicated by the solution candidate.

Performance of the level based decoding algorithm has been analyzed for rate  $\frac{1}{4}$  Turbo codes. The level-based decoding algorithm opens up different alternatives with judicious use of the two encoders resulting in different possibilities of continuing the algorithm. Specifically the sequences  $\{u_1, v_1\}$  and  $\{u_2, v_2\}$  can be selectively retained/removed and the retained ones used in suitable combinations. These combinations are each characterized by its own code rate.

Further, a low complex approach to decoding, that incorporates puncturing to enhance the code rate has also been addressed in [21]. The punctured low complex method helps to converge the decoding process quickly by processing the first half of both received  $\{u_1, v_1\}$  and  $\{u_2, v_2\}$  values separately and results in the reduction of the total number of branches generated. In order to split the received information properly and decode separately, reverse ordering of input information is used at the encoder. The first constituent encoder processes the information in the original order and the second constituent encoder processes the information in the reverse order. At the receiver side, received word is decoded separately for the first half of both  $\{u_1, v_1\}$  and  $\{u_2, v_2\}$  data after updation. The solution candidate obtained from the  $\{u_2, v_2\}$  pair is deinterleaved and appended with the solution candidate from the  $\{u_1, v_1\}$  pair to form the complete solution candidate. Here, only the first halves of both  $\{u, v\}$  pair are used for decoding purpose; only the first halves of the parity bit sets are required to be transmitted. This process helps to increase the overall code rate of the Turbo codes.

The efficiency of the level based decoding algorithm with different code rates and punctured low complex method by decoding a rate  $\frac{1}{3}$  punctured Turbo code has been brought out through simulation analysis [21].

The mathematical derivations to formulate the unique CE associated with different Turbo encoder structures and level based decoding using the unique CE forms the central idea of this paper. This has been carried out with 3GPP LTE and CCSDS Turbo encoders and extensive performance analysis has been done; the details are presented in the forthcoming sections.

### 3. FORMULATION OF CE AND LEVEL BASED DECODING WITH 3GPP LTE AND CCSDS TURBO CODES

With the CE being derived based on the generator polynomial, it varies with the encoder structure. Hence the level based decoding algorithm necessitates the formulation of CEs corresponding to the encoder structure. The CE influences the error patterns and it effectively defines the performance in terms of error correction and computational complexity of the Turbo codes.

#### 3.1 3GPP LTE Turbo Codes

The generator polynomial for the 3GPP LTE Turbo codes is  $\left[1, \frac{1+D+D^3}{1+D^2+D^3}\right]$  and the Turbo encoder for the same is shown in Figure 4.

Figure 4 represents the 8 state LTE Turbo code; at  $j$ th instant the systematic output –  $u_j$  and parity output –  $v_j$  of the constituent encoder are characterized by Equations (12) and (13),

$$u_j = a_{0j} + a_{2j} + a_{3j} \quad (12)$$

$$v_j = a_{0j} + a_{1j} + a_{3j} \quad (13)$$

Combining Equations (12) and (13),

$$u_j + v_j = a_{1j} + a_{2j} \quad (14)$$

At  $(j-1)$ th instant, Equation (14) can be written as

$$\begin{aligned} u_{j-1} + v_{j-1} &= a_{1j-1} + a_{2j-1} \\ &= a_{2j} + a_{3j} \end{aligned} \quad (15)$$

since,  $a_{1j-1} = a_{2j}$ ,  $a_{2j-1} = a_{3j}$ .

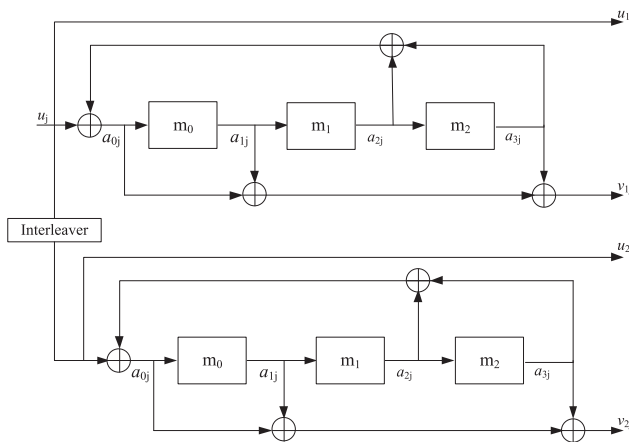


Figure 4: LTE Turbo code [20]

Similarly at  $(j+1)$ th instant, Equation (14) can be written as

$$u_{j+1} + v_{j+1} = a_{0j} + a_{1j} \quad (16)$$

Combining Equations (14), (15) and (16):

$$\begin{aligned} u_{j+1} + v_{j+1} + u_j + v_j + u_{j-1} + v_{j-1} &= a_{0j} + a_{3j} \\ &= a_{1j} + v_j \end{aligned}$$

and hence,

$$a_{1j} = u_{j+1} + v_{j+1} + u_j + u_{j-1} + v_{j-1} \quad (17)$$

From  $a_{1j}$  the rest of the state information can be derived as follows,

$$a_{0j} = u_{j+2} + v_{j+2} + u_{j+1} + u_j + v_j \quad (18)$$

$$a_{2j} = u_j + v_j + u_{j-1} + u_{j-2} + v_{j-2} \quad (19)$$

$$a_{3j} = u_{j-1} + v_{j-1} + u_{j-2} + u_{j-3} + v_{j-3} \quad (20)$$

Equation (13) can be rewritten as

$$v_j + a_{0j} + a_{1j} + a_{3j} = 0 \quad (21)$$

substituting  $a_{0j}$ ,  $a_{1j}$  and  $a_{3j}$  in Equation (21),

$$u_{j-3} + v_{j-3} + u_{j-2} + v_{j+1} + v_{j+2} + u_{j+2} = 0 \quad (22)$$

Equation (22) is the CE corresponding to the LTE Turbo code.

It represents the constituent encoder in Figure 4 and has to satisfy for all  $j$  values. It is clear from Equation (22) that the  $CE[j]$  depends on  $(u, v)$  values from the  $(j-3)$ rd time instant to  $(j+2)$ nd time instant. An  $N$  bit information sequence will have  $(N-5)$  CEs –  $CE[3]$  to  $CE[(N-1)-2]$ . If a bit  $u_j$  is in error, it will affect the CEs,  $\{CE[j-2], CE[j+2], CE[j+3]\}$ . If a bit  $v_j$  is in error, it will affect CEs,  $\{CE[j-2], CE[j-1], CE[j+3]\}$ . Similarly the erroneous bits  $u_{j-1}$  and  $v_{j-1}$  affects the CEs,  $\{CE[j-2], CE[j+1]\}$ . In this way, a total of 17 correctable error/error patterns and corresponding affected CEs are possible. The decoding process makes use of only single, double and triple error/error patterns. The details of the reduced error/error patterns that total to 5, and the affected CEs, each initiated at  $CE[j-2]$ , are given in Figure 5. Each branch represents the error/error patterns and the corresponding affected CEs.

Equation (22) shows that  $CE[j]$  depends on a series of  $(u, v)$  values. In order to cover and correct all  $(u, v)$  values at the receiver side, it is necessary to prepend and append

Error patterns	Affected CEs
$U_j$	$[j-2, j+2, j+3]$
$V_j$	$[j-2, j-1, j+3]$
$U_{j-1}, V_{j-1}$	$[j-2, j+1]$
$U_{j-4}, V_{j-4}, U_{j-3}$	$[j-2, j-1, j]$
$U_{j-2}, V_{j-2}, V_{j-1}$	$[j-2, j, j+2]$

Figure 5: Error combination and affected CEs for LTE Turbo codes

5 zeros with the message bits. This results in a total length of “ $N + 10$ ” bits for an information sequence of length “ $N$ ”. In short, “ $N + 5$ ” CEs – (CE[3] to CE[ $N + 7$ ]) – are possible with “ $N + 10$ ” bits. It is possible to correct all errors with “ $N + 5$ ” CEs. The modified list becoming empty or the leading CE entry in the modified list becoming greater than ( $N + 7$ ) are the conditions for identifying the solution candidate. The 15 bits (initial five ( $u, v$ ) bits and final five  $u$  bits) are known at the receiver side and that results in fixing the corresponding RRF values as zeros. Cumulative RRF value is calculated at each level for facilitating the selection of the solution candidate. Error patterns corresponding to zero RRF will never contribute to the solution candidate.

Once the initial list of CEs is obtained, formulation of all the 5 error/error patterns at level-0 is performed with the leading entry. The modified list with the associated cumulative RRF corresponding to each branch forms the input to the next level. At level-1, there are a total of  $5 \times 5$  branches possible and, each retained branch with the modified list and cumulative RRF at level-1 forms the input to the next level. The process of branch elimination and checking for the solution candidate are executed in each level. The decoding process continues with the retained branches until the most probable solution candidate is obtained.

### 3.2 Consultative Committee for Space Data Systems (CCSDS) Turbo Codes

The generator polynomial for the CCSDS standard Turbo code is,  $G(D) = \left[ 1, \frac{1+D+D^3+D^4}{1+D^3+D^4} \right]$  and the Turbo encoder for the same is shown in Figure 6. Figure 6 represents 16 state CCSDS Turbo code; at  $j$ th instant the systematic output and parity output of the constituent encoder are characterized by Equations (23) and (24),

$$u_j = a_{0j} + a_{3j} + a_{4j} \quad (23)$$

$$v_j = a_{0j} + a_{1j} + a_{3j} + a_{4j} \quad (24)$$

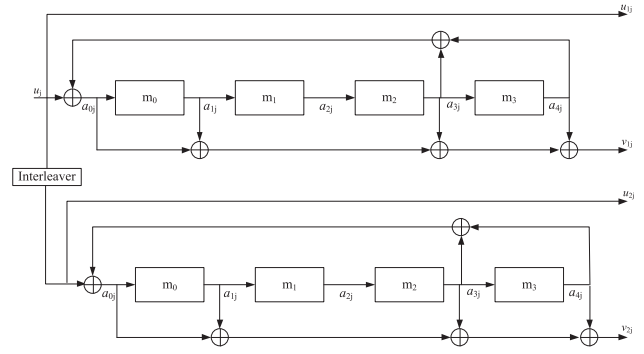


Figure 6: CCSDS Turbo code

Proceeding in the same lines as for the 3GPP LTE case above yields the CE in Equation (25);

$$u_{j-2} + v_{j-2} + u_{j-1} + v_{j-1} + u_j + v_j + u_{j+1} + u_{j+3} + v_{j+4} + u_{j+5} + v_{j+5} = 0 \quad (25)$$

Equation (25) represents the CE of the CCSDS Turbo codes. The CE depends on ( $u, v$ ) values from the ( $j-2$ )nd time instant to ( $j+5$ )th time instant. The CE is applicable for any ( $u, v$ ) values in the range  $\{2, j-5\}$ . ( $N-7$ ) CEs – CE[2] to CE[ $N-6$ ] – are possible for an information sequence of  $N$  bits. The erroneous reception of single bit “ $u_j$ ” affects the CEs,  $\{(CE[j-5], CE[j-3], CE[j-1], CE[j], CE[j+1], CE[j+2])\}$ . Similarly if  $v_j$  is in error, it will reflect in CEs,  $\{CE[j-5], CE[j-4], CE[j], CE[j+1], CE[j+2]\}$ . The erroneous reception of double errors (bits)  $u_{j-1}$  and  $v_{j-1}$  affects the CEs,  $\{CE[j-5], CE[j-4], CE[j-2]\}$ . Following in the same manner, we will get a total of 30 correctable error combinations and the corresponding affected CEs all starting with CE[ $j-5$ ]. These include error patterns varying from single error to five error combinations. The reduced set consisting of single, double and triple error/error patterns totaling to five error combinations and the affected CEs starting with CE[ $j-5$ ] are given in Figure 7. Each branch represents the error/error patterns and the corresponding affected CEs.

Error patterns	Affected CEs
$U_j$	$[j-5, j-3, j-1, j, j+1, j+2]$
$V_j$	$[j-5, j-4, j, j+1, j+2]$
$U_{j-1}, V_{j-1}$	$[j-5, j-4, j-2]$
$U_{j-4}, V_{j-4}, V_{j-3}$	$[j-5, j-3, j-2, j-1]$
$U_{j-2}, V_{j-2}, U_{j-1}$	$[j-5, j-4, j-3, j-2, j-1, j, j+1]$

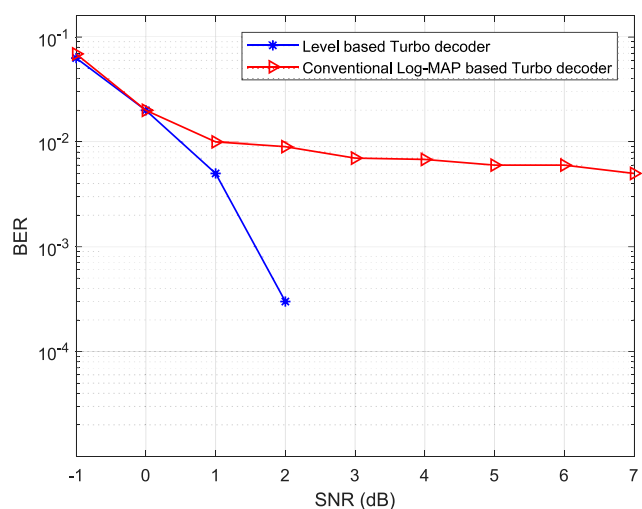
Figure 7: Error combination and affected CEs details for CCSDS Turbo codes

The CE in Equation (25) clearly shows that  $CE[j]$  depends on a series of  $(u, v)$  values. To cover and correct all information bits, it is necessary to prepend and append 7 zeros to the original information bits since  $CE[j]$  depends on the  $(u, v)$  values from the  $(j-2)$ nd time instant to  $(j+5)$ th time instant. This process results in a total length of “ $N+14$ ” bits for an information sequence of length “ $N$ ” bits. In short “ $N+7$ ” CEs – ( $CE[2]$  to  $CE[N+8]$ ) – can correct all errors in the information bits; hence the modified list becoming empty or the leading CE entry in the modified list becoming greater than  $(N+8)$  are the conditions for the solution candidate. The 21 bits (initial 14  $(u, v)$  bits and final 7  $u$  bits) are known at the receiver side and that results in fixing the respective RRF values as zero. Cumulative RRF value is calculated at each level for facilitating the selection the solution candidate. The RRF patterns corresponding to the zero RRF will never contribute to the error patterns in the received data.

Once the initial list of CEs is formed with the leading entry, all the 5 error/error patterns at level 0 are formulated. The modified list corresponding to each branch forms the input to the next level with associated cumulative RRF at level-1. The leading entry of each modified list from level-0 generates the corresponding 5-error/error patterns and results in a total of  $5 \times 5$  branches at level-1. Modified list and cumulative RRF corresponding to the retained branches at level-1 form input to the next level. Elimination of branches and checking for the solution candidate is performed at each level. The decoding process at each level continues until the solution candidate is obtained.

#### 4. RESULTS

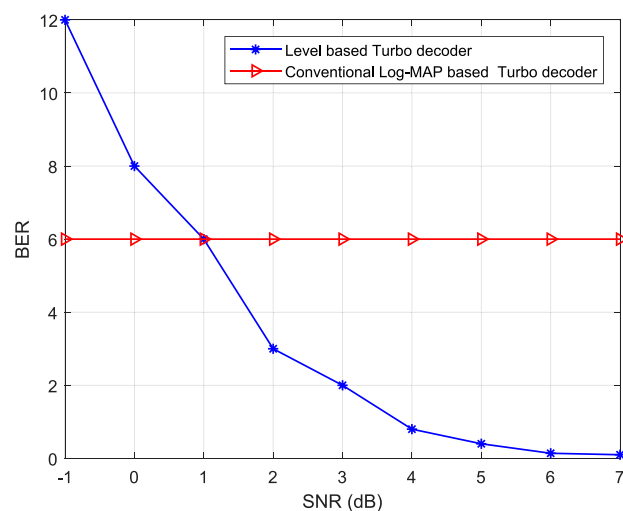
Performance analysis of the algorithm with a four-state Turbo encoder as shown in Figure 2 has been done and the same analysis is extended to applications including 3GPP LTE and CCSDS specifications to establish the efficiency of the algorithm. Initially, simulations were carried out using a message length of 100 bits along with the corresponding prepended and appended zeros; the message sequence is encoded with a rate  $\frac{1}{4}$  four state Turbo encoder as shown in Figure 2. The resulting codeword comprises of systematic and parity outputs  $u_1, u_2$  and  $v_1, v_2$  respectively. Codewords are subjected to the process of transmission through AWGN channel with BPSK modulation. The received noisy codeword is decoded using the level based algorithm for short block length Turbo codes. Performance of the algorithm is compared with the conventional iterative Turbo decoder using Log-MAP algorithm for a message length of 100 bits and for a maximum iteration number of 15.



**Figure 8:** BER performance of the conventional Log-MAP based Turbo decoder and the performance enhanced reliability-based Turbo decoding algorithm with four state Turbo encoder specifications (message block length,  $k = 100$  bits, random interleaver, 100 frames)

Figure 8 shows the BER performance of the conventional Log-MAP-based Turbo decoder and the level based Turbo decoding algorithm with four state Turbo encoder. The number of branches retained at each level and given as input to the next level is restricted to 50.

It is evident from the figure that the level based decoding algorithm for short block length Turbo codes achieves significant improvement in error correction performance as compared to the conventional Log-MAP based Turbo



**Figure 9:** Decoding time complexity comparison of the conventional Log-MAP based Turbo decoder and the performance enhanced reliability-based Turbo decoding algorithm with four state Turbo encoder specifications (message block length,  $k = 100$  bits, random interleaver, 100 frames)



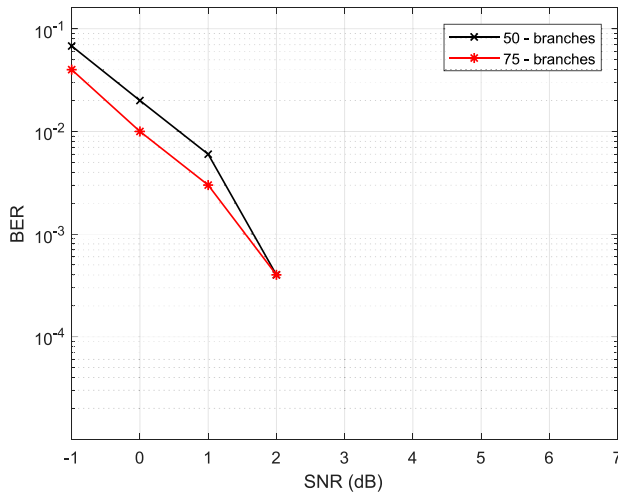
decoder. It can be seen that for SNR values greater than 2 dB, the BER remains at zero.

Figure 9 shows the decoding time comparison of the Turbo decoder using the level based algorithm and the conventional Log-MAP based Turbo decoding algorithm. It is clear from the figure that the decoding time of the conventional Log-MAP based Turbo decoder is constant at all channel conditions. As SNR increases, the time complexity of the performance-enhanced reliability-based Turbo decoder decreases. As the channel conditions become good, the received data is

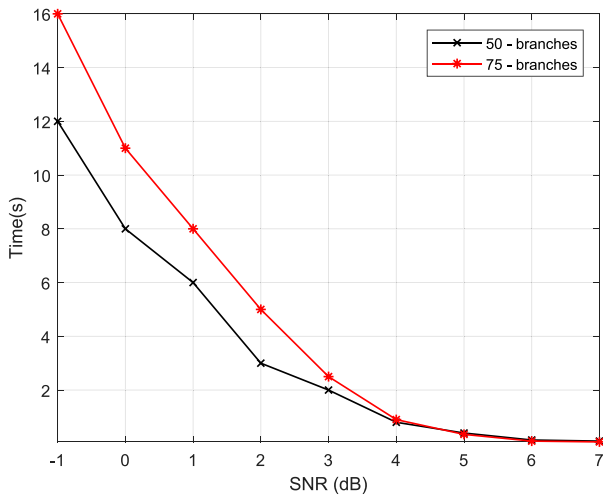
prone to less number of errors and hence fewer levels are required to identify the error positions.

Further improvement in the BER performance can be achieved by increasing the number of branches at each level. The improvement achieved with 75 branches is shown in Figure 10. This improvement in BER is achieved at the cost of increased computational complexity as shown in Figure 11.

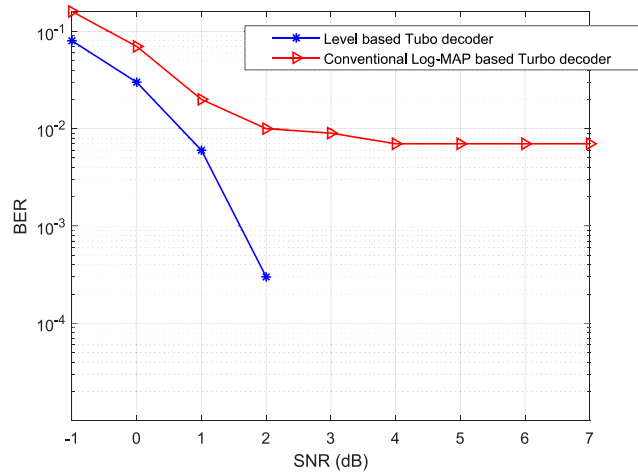
Secondly, simulations were carried out using a message length of 100 bits along with the corresponding



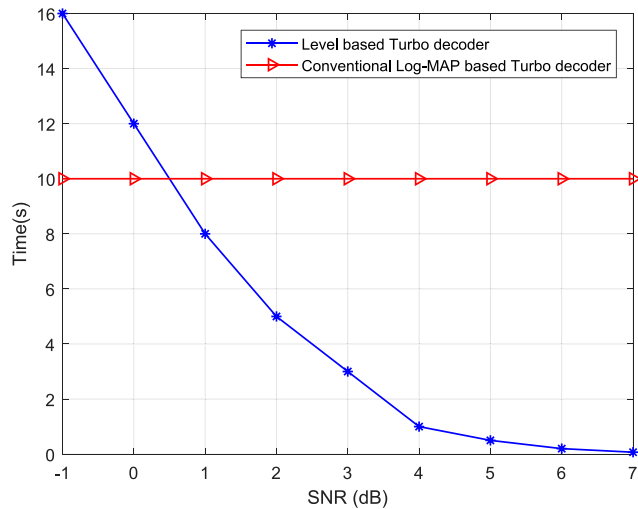
**Figure 10:** Decoding time complexity of the performance-enhanced reliability-based algorithm with 50 branches and 75 branches for four state Turbo encoder (message block length,  $k = 100$  bits, random interleaver, 100 frames)



**Figure 11:** Decoding time complexity of the performance-enhanced reliability-based algorithm with 50 branches and 75 branches for four state Turbo encoder (message block length,  $k = 100$  bits, random interleaver, 100 frames)



**Figure 12:** BER performance of the conventional Log-MAP based Turbo decoder and the performance enhanced reliability-based Turbo decoding algorithm with LTE specifications (message block length,  $k = 100$  bits, random interleaver, 100 frames)



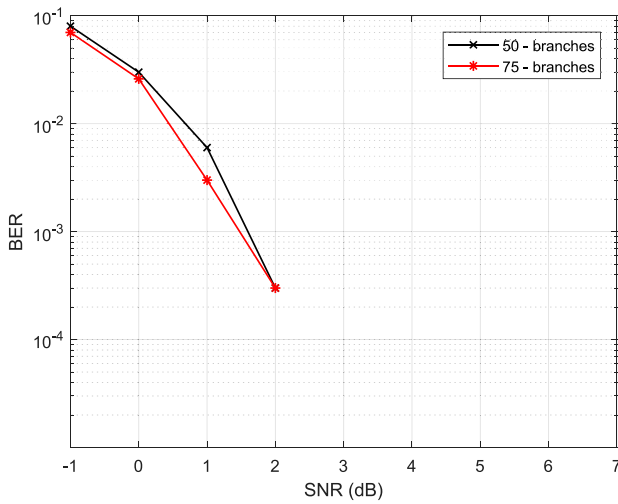
**Figure 13:** Decoding time complexity comparison of the conventional Log-MAP based Turbo decoder and performance enhanced reliability-based Turbo decoding algorithm with LTE specifications (message block length,  $k = 100$  bits, random interleaver, 100 frames)

prepended and appended zeros. The message sequence is encoded with a rate  $\frac{1}{4}$  3GPP LTE Turbo encoder as shown in Figure 4. Error correction performance and decoding time complexity of the algorithm with 3GPP LTE specifications are shown in Figures 12 and 13.

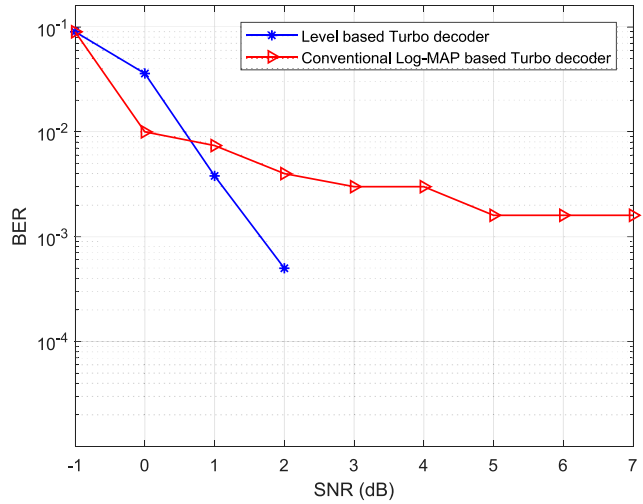
Application of the decoding algorithm in 3GPP LTE Turbo codes have shown significant error correction performance improvement as compared to the conventional iterative 3GPP LTE Turbo decoder. The performance of the decoding algorithm can be further improved by increasing the number of retained branches to 75 at each

level as shown in Figure 14. The associated complexity increases correspondingly as shown in Figure 15.

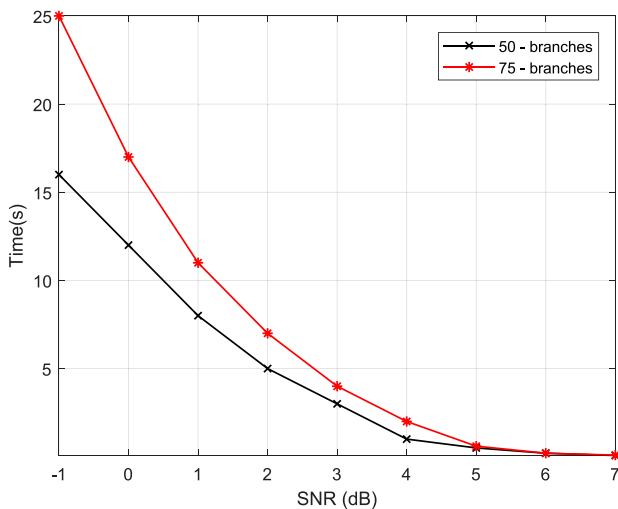
Further, to establish the efficiency of the algorithm, the performance analysis is extended to CCSDS specifications. BER performance and decoding time complexity of the conventional Log-MAP based Turbo codes and the performance enhanced level based Turbo decoding algorithm with CCSDS specification are shown in Figures 16 and 17. The level-based Turbo decoding algorithm achieves significant performance as in the case of 3GPP LTE Turbo codes. Increasing the number of retained



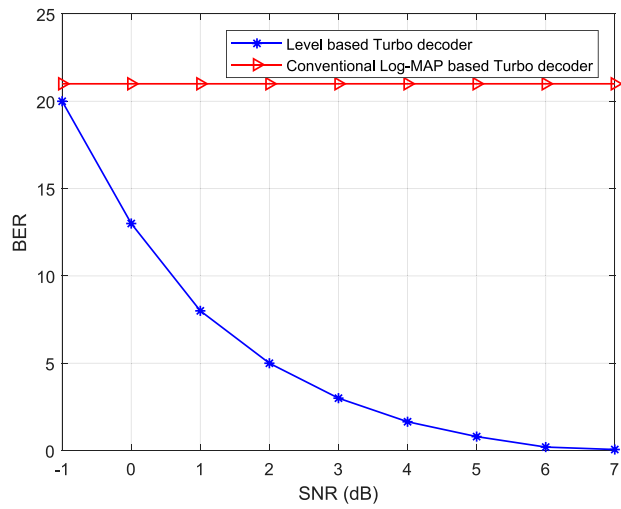
**Figure 14:** BER performance of the performance-enhanced reliability-based algorithm with 50 branches and 75 branches for LTE specifications (message block length,  $k = 100$  bits, random interleaver, 100 frames)



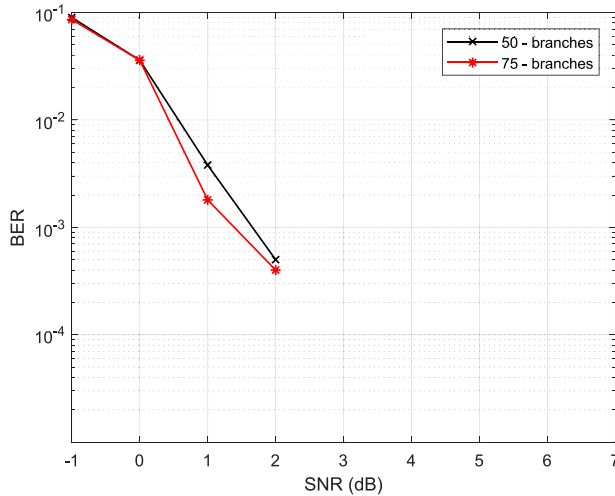
**Figure 16:** BER performance of the conventional Log-MAP based Turbo decoder and the performance enhanced reliability-based Turbo decoding algorithm with CCSDS specifications (message block length,  $k = 100$  bits, random interleaver, 100 frames)



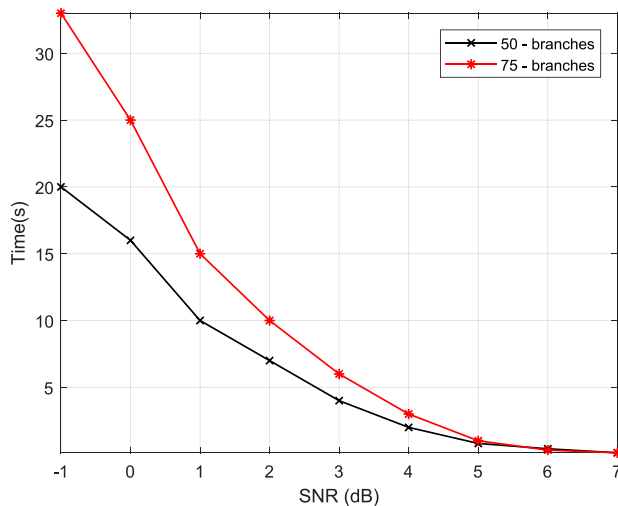
**Figure 15:** Decoding time complexity of the performance-enhanced reliability-based algorithm with 50 branches and 75 branches for LTE specifications (message block length,  $k = 100$  bits, random interleaver, 100 frames)



**Figure 17:** Decoding time complexity comparison of the conventional Log-MAP based Turbo decoder and the performance enhanced reliability-based Turbo decoding algorithm with CCSDS specifications (message block length,  $k = 100$  bits, random interleaver, 100 frames)



**Figure 18:** BER performance of the performance-enhanced reliability-based algorithm with 50 branches and 75 branches for CCSDS specifications (message block length,  $k = 100$  bits, random interleaver, 100 frames).



**Figure 19:** Decoding time complexity of the performance-enhanced reliability-based algorithm with 50 branches and 75 branches for CCSDS specifications (message block length,  $k = 100$  bits, random interleaver, 100 frames)

branches to 75 in the algorithm leads to improvement in performance as shown in Figure 18. This improvement in BER performance is achieved at the cost of increased time complexity as shown in Figure 19.

## 5. CONCLUSIONS

The demand for communication with short data blocks is increasing in recent years. Real-time communication and low latency applications require communication with short block length codewords. Strong channel codes are required to ensure reliable transmission over dynamic channel conditions. The demand for communication

with short block Turbo codes is increasing in applications like mobile communication, wireless sensor networks, and satellite communication. In this paper, the performance of the novel reliability-based algorithm has been analyzed for 3GPP LTE, and CCSDS Turbo codes. Simulation results show that the algorithm outperforms the conventional iterative Turbo decoder in terms of BER performance. The time complexity of the performance-enhanced reliability-based Turbo decoder shows a clear advantage as SNR increases. The performance flattening at high SNR region is completely eliminated with the proposed decoding algorithm. This is a clear advantage for applications requiring communications with short block length Turbo codes. The algorithm is an attractive solution to achieve reliable and timely transmission of short block length Turbo codes in mobile and satellite communication applications. The proposed algorithm has a coding gain of 2.45 dB at a BER of  $10^{-3}$  over AWGN channel with BPSK modulation for a code rate of  $\frac{1}{4}$ . The algorithm has a channel adaptive complexity and has shown nearly 82% reduction in the decoding time complexity for the rate  $\frac{1}{4}$  Turbo code at 3 dB SNR. The performance analysis of the level based Turbo decoding algorithm gives an insight into an alternate decoding approach for Turbo codes.

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## REFERENCES

1. S. Tong, D. Lin, A. Kavcic, B. Bai, and L. Ping. "On short forward error-correcting codes for wireless communication systems," in Proceedings of 16th IEEE International Conference on Computer Communications and Networks, Honolulu, 2007, pp. 391–6.
2. S. N. Vaniya, N. Kumar, and C. Sacchi. "Performance of iterative turbo coding with nonlinearly distorted OFDM signal," in Proceedings of IEEE Annual India Conference (INDICON), Bangalore, 2016, pp. 1–5.
3. L. Shu, and D. J. Costello. *Error Control Coding*. Noida, UP: Pearson Education, 2011. ch. 16.
4. T. Tonnellier, C. Leroux, B. L. Gal, B. Gadat, C. Jegou, and N. V. Wambeke, "Lowering the error floor of turbo codes with CRC verification," *IEEE Wireless Commun. Lett.*, Vol. 5, pp. 404–7, Aug. 2016. DOI: 10.1109/LWC.2016.2571283
5. M. Hernaez, P. M. Crespo, and J. D. Ser, "Flexible channel coding approach for short-length codewords," *IEEE Commun. Lett.*, Vol. 16, pp. 1508–11, Sep. 2012. DOI: 10.1109/LCOMM.2012.073112.121295

6. T. Jerkovits, and B. Matuz. "Turbo code design for short blocks," in Proceedings of Advanced Satellite Multimedia Systems Conference and the 14th Signal Processing for Space Communications Workshop, Palma de Mallorca, 2016, pp. 1–6.
7. N. Wiberg, H. A. Loeliger, and R. Kotter, "Codes and iterative decoding on general graphs," *Eur. Trans. Telecommun.*, Vol. 6, pp. 513–25, Sep./Oct. 1995. DOI: [10.1002/ett.4460060507](https://doi.org/10.1002/ett.4460060507)
8. G. Liva, E. Paolini, B. Matuz, S. Scalise, and M. Chiani, "Short turbo codes over high order fields," *IEEE Trans. Commun.*, Vol. 61, pp. 2201–11, Jun. 2013. DOI: [10.1109/TCOMM.2013.041113.120539](https://doi.org/10.1109/TCOMM.2013.041113.120539)
9. G. Liva, L. Gaudio, T. Ninacs, and T. Jerkovits. "Code design for short blocks: a survey," Available: arXiv:1610.00873 [cs.IT].
10. N. Abughalieh, K. Steenhaut, A. Now, and A. Anpalagan, "Turbo codes for multi-hop wireless sensor networks with decode-and-forward mechanism," *EURASIP J. Wirel. Commun. Netw.*, Vol. 2014, pp. 1–13, Dec. 2014. DOI: [10.1186/1687-1499-2014-204](https://doi.org/10.1186/1687-1499-2014-204)
11. J. V. Wonterghem, A. Alloum, and J. J. Boutros. "On performance and complexity of OSD for short error correcting codes in 5G-NR," in First International Balkan Conference on Communications and Networking, Tirana, 2017, pp. 1–5.
12. J. Oestman, G. Durisi, and E. Stroem. "Low-latency ultra-reliable 5G communications: Finite block length bounds and coding schemes," in Proceedings of IEEE Conference on Systems, Communications and Coding, Accepted for publication, 2017, Available: (or arXiv:1611.08714v1 [cs.IT]).
13. M. Shirvanimoghaddam, *et al.*, "Short block-length codes for ultra-reliable low latency communications," *IEEE Commun. Mag.*, Vol. 57, pp. 130–7, Feb. 2019. DOI: [10.1109/MCOM.2018.1800181](https://doi.org/10.1109/MCOM.2018.1800181)
14. "Next generation uplink," Consultative Committee for Space Data Systems (CCSDS) Report Concerning Space Data System Standards. Green Book, Issue 1, 230.2-G-1, 2014.
15. C. Al Bechlawi, and F. Guilloud. "Frame length reduction for massive-machine communications," in Proceedings of IEEE 81st Vehicular Technology Conference, United Kingdom, pp. 1–5, 2015.
16. I. Motohiko, M. P. C. Fossorier, and I. Hideki, "On the sub-optimality of iterative decoding for turbo-like and LDPC codes with cycles in their graph representation," *IEEE Trans. Commun.*, Vol. 52, pp. 845–54, May 2004. DOI: [10.1109/TCOMM.2004.826236](https://doi.org/10.1109/TCOMM.2004.826236)
17. Z. Chi, Z. Wang, and K. K. Parhi. "A study on the performance, power consumption tradeoffs of short frame turbo decoder design," in Proceedings of IEEE International Conference on Acoustics, Speech, and Signal Processing, Salt Lake City, UT, USA, 2001, pp. 2637–40.
18. G. Durisi, T. Koch, and P. Popovski. "Towards massive, ultra reliable, and low-latency wireless: the art of sending short packets," 2016, Available: arXiv:1504.06526 [cs.IT].
19. S. Weithoer, and N. Wehn. "Enhanced decoding for high-rate LTE turbo-codes with short block lengths," in Proceedings of IEEE International Conference on Communications Workshops, Paris, 2017, pp. 967–72.
20. T. P. Fowdur, Y. Beeharry, and S. K. M. Soyjaudah. "Performance of modified asymmetric LTE turbo codes with reliability-based hybrid ARQ," in 9th International Symposium on Communication Systems, Networks & Digital Sign, Manchester, 2014, pp. 928–33.
21. P. Salija, B. Yamuna, T. R. Padmanabhan, and D. Mishra. "A novel reliability based high performance decoding algorithm for short block length Turbo codes," *Int. J. Ad Hoc Ubiquitous Comput.*, (in Press), accepted for publication.
22. B. Yamuna. "Some investigations on a class of reliability based soft decision decoding algorithms for block codes," Ph.D. dissertation, Dept. of ECE, Amrita Vishwa Vidyapeetham, India, 2013.

## Authors



**P. Salija** obtained her B.Tech. degree in 2011 and M.Tech. Degree in 2013. She is currently a senior research fellow and is pursuing doctorate in the department of ECE at Amrita School of Engineering. Her current research interest is error control coding.

**Corresponding author. Email:** p\_salija@cb.amrita.edu



**B. Yamuna** received her M.E., in VLSI design in 2004, and Ph.D. in Error Control Coding in 2013 from Amrita School of Engineering, Amrita Vishwa Vidyapeetham. She is working as Associate Professor in the Dept. of ECE at Amrita School of Engineering. She has published and presented papers in International journals and conferences. She has reviewed papers for international and national conferences, and chaired sessions. Her current research interests include coding for reliable communication, VLSI architectures for communication systems, and cryptosystems based on error control codes. She is a member of ISTE and IETE.

**Email:** b\_yamuna@cb.amrita.edu



**T. R. Padmanabhan** obtained his master degree in 1968 and Ph.D. from IIT Kharagpur in 1974. He is currently an Adjunct Professor in the department of ECE, at Amrita Vishwa Vidyapeetham, Coimbatore. He taught at the IIT Kharagpur, before doing Research and Development for private companies for several years. He is a Senior Member of the IEEE and a Fellow of both the Institution of Engineers (IEI) and the Institution of Electronics and Telecommunication Engineers (IETE). He has published books with Wiley, Tata McGraw-Hill, and Springer Verlag.

**Email:** trp@amrita.edu



**Deepak Mishra** has received the B.E. degree in Electronics and Communication from the Govt G.B. Pant. Engineering College, Uttaranchal, in 2001, M.Tech degree in Communications Systems from Department of Electronics Engineering, IIT, B.H.U in 2003 and Ph.D. degree also from IIT, BHU on the topic "Joint Source Channel Coding for Deep Space Application", in the year 2012. He has joined SAC, ISRO in year 2003. During this tenure, He was involved in various subsystems development of various ISRO projects. He is currently working as a Scientist /Engineer-SF. He has more than 40 papers in various international journals and conferences.

**Email:** deepakmishra@sac.isro.gov.in