An Efficient Class-G Stage for Switching RF Power Amplifier Applications

Kunhee Cho and Ranjit Gharpurey

Abstract—An efficient class-G stage based on a class-D power amplifier (PA) for switching RF PA applications is described. Class-G operation is achieved by introducing one additional transistor in a cascoded class-D PA, that can reduce area as well as enhance efficiency when compared to prior class-G designs. In addition, a multi-level switching operation is proposed which provides stacked class-G PA operation without using any additional switches. The stacked PA can avoid the requirement for an extra supply voltage for class-G operation. The efficiency and losses in the proposed design, as well as conventional designs, at various output power levels are analyzed by utilizing these in a 5-bit switched-capacitor PA (SCPA). A stacked class-G design with single supply voltage is also compared to an unstacked dual-supply class-G design. While the proposed approach has been explored in a SCPA, the approach can be applied to any switching RF PA architecture that employs a class-D PA.

Index Terms—Power amplifier, class-G PA, class-D PA, SCPA, switched-capacitor power amplifier, stacked PA.

I. INTRODUCTION

SWITCHING power amplifiers such as class-D, class-E, and class-F PAs designs are very attractive because they have better efficiency compared to linear PAs due to saturated operation. Switching PAs can be implemented in CMOS processes that enable system-on-chip (SOC) implementations by allowing integration of the RF and analog section of a transceiver with digital baseband and application processors. Digital processors are typically implemented in advanced deep-submicron CMOS technologies to increase circuit density and enhance performance. Switching PAs can also benefit from process scaling.

The efficiency of switching PAs is typically maximized when the output power of the PA is close to the maximum output power. To enhance the back-off efficiency, a class-G topology [1], [2], [3], [4], [5] or multiple supply-voltage-based design [6] can be used. Fig. 1 shows a typical class-G power amplifier design, and its efficiency. A class-G topology employs an additional lower supply voltage such that the RF PA uses the high primary supply voltage (V_{DDH}) for providing high output power levels, and the lower supply voltage (V_{DD}) for low output power levels. It is also possible to employ multiple supplies to further enhance back-off performance [6].

Class-G or multi-supply designs based on class-D^{-1} and class-E PAs have been reported in [1], [5], [6]. Although back-off efficiency improvement can be achieved here, additional

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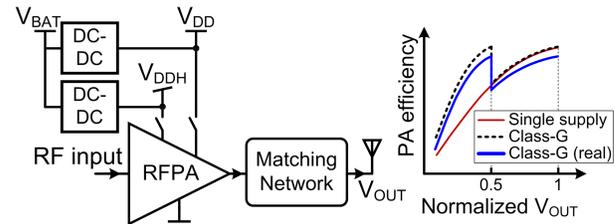

Fig. 1: General class-G power amplifier and efficiency.

switches are required in the path of each supply voltage to enable switching from one supply to another. These switches are typically implemented using large, thick gate-oxide transistors to reduce the conduction loss arising from the on-resistance of the switch, and tolerate high voltage levels.

In a class-D PA, the PA is composed of switches, and the output is switched between the main supply voltage (V_{DDH}) and ground (GND), based on the state of the switches. Since a class-D PA employs voltage-based switching, it is possible to implement a class-G topology with an additional switch between the PA output and the extra supply voltage (V_{DD}), but without an extra switch to turn-off the V_{DDH} path [2].

Class-G and multiple supply-voltage topologies have been used in different digital switching PA architectures such as a polar PA [1], a digital polar PA [5], a digital outphasing PA [6], and a switched-capacitor PA [2], [3], [4]. Most techniques based on a class-G topology show improved performance compared to a single-supply class-D design when the output power is low, because the RF PA employs a lower supply (V_{DD}) for this power range. Assuming that V_{DD} is half of V_{DDH}, the class-G stage provides performance benefit for normalized V_{OUT} from 0 to 0.5, compared to a single-supply. Theoretically, the efficiency is identical to the single-supply case for a normalized V_{OUT} from 0.5 to 1, however, in practice efficiency is reduced due to the loss from the extra devices in a class-G design. Furthermore, the extra DC-DC converter for generation of V_{DD} can also degrade the efficiency for the normalized V_{OUT} range from 0 to 0.5, in addition to increasing the implementation cost (Fig. 1).

A switched-capacitor power amplifier (SCPA) is a capacitive DAC that modulates the output amplitude by changing the capacitive divider ratio in the output stage. A class-G SCPA exhibits improved efficiency not only in the normalized V_{OUT} range of 0 to 0.5 but also in the range from 0.5 to 1 because $V_{DDH} - GND$ switching and $V_{DD} - GND$ switching can be employed simultaneously [2].

In this work, an efficient class-G PA based on a class-D
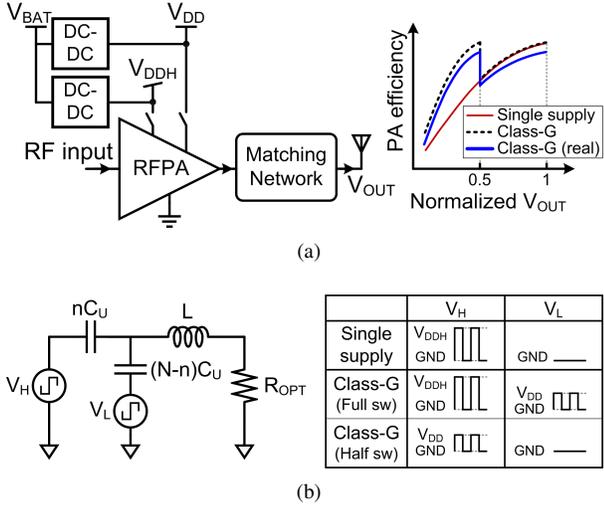
Fig. 2: Class-G switched-capacitor power amplifier (a) Structure and efficiency. (b) Equivalent circuit.

Fig. 3: (a) 4-Tr class-D PA. (b) 6-Tr class-G PA. (c) Proposed 5-Tr class-G PA.

PA is proposed that can enhance the efficiency as well as reduce the area compared to prior art. Moreover, the proposed switching approach can avoid the requirement for an additional lower voltage source (V_{DD}) within the PA that is typically required in a class-G topology. This can provide additional efficiency improvement in an actual implementation.

This paper is organized as follows. Section II describes the operation and drain efficiency of the class-G SCPA. Section III introduces the proposed class-G PA design and provides a relative comparison to prior class-D and class-G PAs in the context of an SCPA architecture. Section IV describes a stacked design with the proposed driving signals, to implement class-G operation without the requirement for additional voltage source in the PA. Conclusions are provided in Section V.

II. CLASS-G SWITCHED-CAPACITOR POWER AMPLIFIER

Fig. 2 shows a class-G SCPA design, with two supply levels, and its equivalent circuit. The design consists of N unit PA stages, where each unit PA stage has its own DC blocking capacitor (C_U), such that the total capacitor size is $C_{TOT} = N \cdot C_U$. Assume that the number of capacitors switched to a high voltage level (V_H) is n, while $N - n$ capacitors are switched to a low level (V_L). With a single supply voltage, n capacitors are switched to V_{DDH}, while $(N - n)$ capacitors are held at GND. Effectively, the circuit looks like a series connection of two capacitors with values $n \cdot C_U$, and $(N - n) \cdot C_U$, due to which the output amplitude is scaled by a series capacitive divider ratio of n/N. Class-G operation employs full-supply switching for normalized V_{OUT} from 0.5 to 1, and half-supply switching for normalized V_{OUT} from 0 to 0.5. For the half-supply switching mode, the operation is the same as the single-supply voltage case, however, the voltage swing at the selected high-level capacitor is reduced to V_{DD}, instead of V_{DDH}. Thus, the output amplitude is halved and the voltage swing at the output is reduced to V_{DD}. In a SCPA, each PA has its own DC blocking capacitor. Thus it is possible
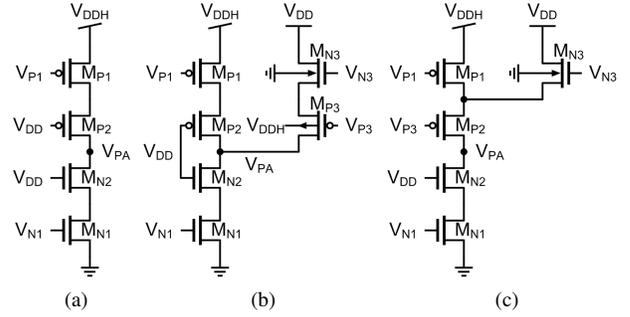
to combine $V_{DDH} - GND$ and $V_{DD} - GND$ switching in the full switching mode (Fig. 2b, inset table). This improves the efficiency in the normalized V_{OUT} range of 0.5 to 1 as well, since the voltage swing across two series capacitors is reduced to V_{DD}. The output amplitude in this case is scaled by $(N + n)/2N$ and $n/2N$ for full and half-switching modes, respectively [2].

The drain efficiency of SCPA can be expressed as,

$$\eta = \eta_{MN} \cdot \frac{P_{OUT}}{P_{OUT} + P_{SC} + P_{COND} + P_{SW}} \quad (1)$$

where η_{MN} is the loss from the matching network, P_{OUT} is the output power at the load, P_{COND} is the on-resistance loss from the PA, and P_{SW} is the switching loss from the PA. P_{SC} is the switching loss from the capacitor seen at the output of the PA (C_{SC}) by the switched capacitor array, where C_{SC} can be expressed as $(n \cdot (N - n)/N) \cdot C_u$. Thus, the loss, P_{SC}, can be expressed as,

$$P_{SC} = f \cdot C_{SC} \cdot (V_{SC})^2 \quad (2)$$

where V_{SC} is the voltage swing across C_{SC}. P_{SC} can be significantly reduced in a class-G topology because the voltage swing across C_{SC} is reduced from V_{DDH} and V_{DD}.

P_{COND} and P_{SW} are contributed by the PA, and depend on the PA architecture. Theoretically, P_{COND} and P_{SW} are zero in an ideal PA. However, a voltage drop exists across the switch in a real MOSFET device due to the on-resistance, which limits the output power. In addition, parasitic capacitance has to be charged and discharged to switch the output, that contributes switching loss, in addition to C_{SC}. In a class-G topology, P_{SW} can also be reduced at both high and low outputs following the same principle as the reduction in P_{SC}.

III. PROPOSED CLASS-G POWER AMPLIFIER

The four-transistor cascode is commonly used for implementing class-D PAs [7], [8], [9], [10] (Fig. 3a). This design can support a supply voltage (V_{DDH}) which is twice of the process supply voltage (V_{DD}) without using any thick-oxide gate transistors. A six-transistors (6-Tr) class-G design based on a class-D PA was described in [2], [3], [4]. The design employed two additional thin gate-oxide transistors (M_{P3} and M_{N3}) to provide a path to V_{DD} (Fig. 3b). The 6-Tr class-
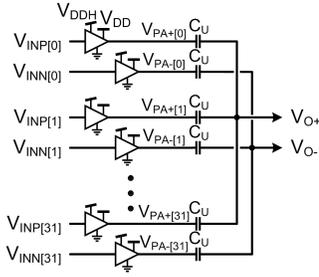
Fig. 4: 5-bit unary differential SCPA structure.

SCPA Res.	F_{SW}	R_{OPT}	C_U	$M_{P1}/M_{P2}/M_{P3}$	M_{N1}/M_{N2}	M_{N3}
5 bits unary	1 GHz	4 Ω	250 fF	180µm/120nm	50µm/120nm	70µm/120nm (6-Tr Class-G) 50µm/120nm (5-Tr Class-G)

TABLE I: PA parameters.

Fig. 5: Performance of 5-bit SCPA with different PA designs. (a) Efficiency. (b) DNL.

G PA can switch between V_{DDH} and GND, and V_{DD} and GND.

In a 6-Tr class-G PA, the leakage current in the V_{DD} path is avoided by proper gate control for M_{P3} and M_{N3}. However these devices lead to additional switching losses when the PA switches between V_{DDH} and GND. The dominant loss contributor is M_{P3} because this device is typically larger than M_{N3}, and both its drain and source are switching. The drain of M_{P3} is directly connected to the output of PA, V_{PA}, that switches at the V_{DDH} level, while the source of M_{P3} (source of M_{N3}) switches at the $V_{DD} - V_{TH.P}$ level. Thus, the additional switching loss by these devices ($P_{SW\,add.6Tr}$) can be expressed as,

$$P_{SW\,add.6Tr} = f \cdot (C_{GD.P3} + C_{DB.P3}) \cdot (V_{DDH})^2$$
$$+ f \cdot (C_{GS.P3} + C_{SB.P3}) \cdot (V_{DD} - V_{TH.P3})^2$$
$$+ f \cdot (C_{GS.N3} + C_{SB.N3}) \cdot (V_{DD} - V_{TH.P3})^2 \quad (3)$$

where C_{GS}, C_{GD}, C_{DB}, and C_{SB} are the gate-to-source, gate-to-drain, drain-to-body, and source-to-body parasitic capacitances, respectively. In addition, since the body nodes of M_{P3} and M_{N3} are connected to V_{DDH} and GND, respectively, to avoid leakage, this causes larger on-resistance due to increased V_{TH} for a given device size. To compensate for this, the size of M_{N3} is usually made larger than M_{N1} and M_{N2} to match the on-resistance at each supply/ground path [3], which further increases switching losses.

To reduce the switching loss due to these extra devices, a 5-Tr class-G PA is proposed, as shown in Fig. 3c. The lossy M_{P3} transistor is removed and M_{N3} is connected in parallel with M_{P1}. Thus, there is no additional device that is connected to V_{PA}. The gate of M_{P2} is still set to V_{DD} when V_{PA} switches between V_{DDH} and ground, but driven by the same V_{P3} that is used in a 6-Tr class-G PA when V_{PA} switches between V_{DD} and GND (Fig. 8a and Fig. 8b). Thus, the switching loss arising from the additional device ($P_{SW\,add.5Tr}$) compared to a 4-Tr class-D PA can be expressed as,

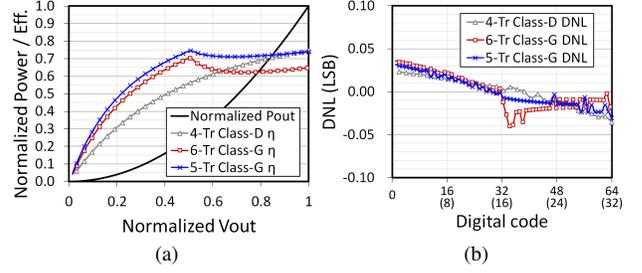$$P_{SW\,add.5Tr} = f \cdot (C_{GS.N3} + C_{SB.N3}) \cdot (V_{DD} - V_{TH.P2})^2 \quad (4)$$

The body of M_{P2} can be connected to its source, instead of V_{DDH}, because M_{P2} always sinks charge, due to which the source of M_{P2} is always at a higher potential than the drain of M_{P2}. Moreover, M_{N3} can be the same size as M_{N1} and M_{N2} because the body effect in M_{P2} is eliminated. Although the V_{TH} of M_{N3} is slightly higher than that of M_{N1} and M_{N2} due to body effect, the on-resistance is still similar because the V_{GS} of M_{N3} is slightly higher than V_{DD}, by nearly $I_{OUT} \cdot r_{on.N3}$.

In order to compare the PA performance, a 5-bit unary differential SCPA using different PA designs with a lossless matching network is designed (Fig. 4). V_{DDH} and V_{DD} are set at 2.4 V and 1.2 V, respectively. The parameters of the FETs used here are summarized in Table I.

Fig. 5a shows the simulated normalized P_{OUT} and drain efficiency of the 5-bit SCPA with different PAs for a normalized V_{OUT}. The maximum output voltage of 4-Tr class-D PA after the matching network is set as a normalized V_{OUT} of 1, since this is the highest physical V_{OUT} among 4-Tr class-D PA, 6-Tr class-G PA, and 5-Tr class-G PA. The normalized P_{OUT} is given by the square of the normalized V_{OUT}. Since a class-G PA has two different switching modes due to the use of two supply voltage levels, the actual resolution of the class-G SCPA is 6-bits. Thus, 32 data points are achieved for a class-D PA, and 64 data points are achieved for the class-G PA. Only even codes are marked for the class-G PA for clarity.

The 6-Tr class-G PA exhibits better efficiency compared to a 4-Tr class-D PA only when the normalized P_{OUT} is below 0.45 (∼- 3.5dB), due to additional loss from the extra devices. Additionally, the maximum P_{OUT} of the 6-Tr class-G PA is slightly lowered because of the extra parasitic capacitance, especially at the output node. By contrast, the proposed 5-Tr class-G PA has almost similar efficiency as well as output power around the peak level compared to a class-D stage, since the loss from M_{N3} is almost negligible. In addition, the efficiency of 5-Tr class-G PA is higher than the 6-Tr class-G PA over the full range of output power.

The PA can cause non-linearity due to parasitic capacitance and on-resistance of non-ideal switches. Ideally, the shape of V_{PA} is a square-wave that switches between the supply and GND, however, the shape of V_{PA} can vary as a function of the applied digital code due to non-idealities in the PA, especially when the device resistance in supply and GND paths is mismatched [7]. Fig. 5b shows the differential non-linearity (DNL) for different PAs. In order to minimize the
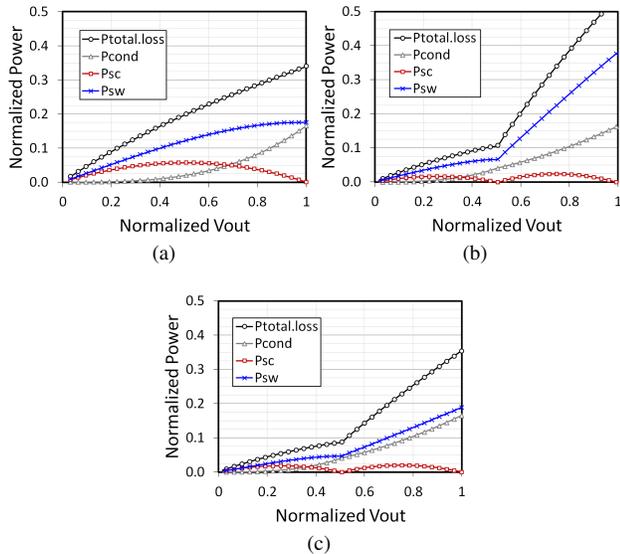
Fig. 6: Power loss analysis for different power amplifier designs. (a) 4-Tr class-D PA. (b) 6-Tr class-G PA. (c) 5-Tr class-G PA.

Fig. 7: Stacked differential PA. (a) Full supply voltage level (V_{DDH}) switching. (b) Half supply voltage level (V_{DD}) switching.

Fig. 8: 5-Tr class-G PA multi-level switching operation. (a) $V_{DDH} - GND$ switching. (b) $V_{DD} - GND$ switching. (c) $V_{DDH} - V_{DD}$ switching.

non-linearity caused by the PA, the on-resistance of each supply and GND path has to be matched. The 6-Tr class-G PA shows the worst DNL because the on-resistance of the V_{DD} path is not well-matched with V_{DDH} and GND paths. To match the on-resistance of the V_{DD} path with V_{DDH} and GND paths, the size of M_{P3} has to be made much larger than M_{P1} and M_{P2} which will decrease the efficiency even more. It is easier to match on-resistance in the 5-Tr class-G PA, since M_{P2} is shared in the V_{DDH} and V_{DD} paths, and hence only the on-resistance of M_{P1} and M_{N3} has to be matched.

The power loss of each PA is analyzed through simulation (Fig. 6) by considering the loss components P_{SC}, P_{SW}, and P_{COND}. As expected, P_{SC} is zero when the normalized V_{OUT} is halved in the class-G approach, because the entire switched-capacitor array is selected to switch between V_{DD} and GND, due to which C_{SC} becomes zero. In addition, P_{SC} is also significantly reduced because the voltage swing across C_{SC} is decreased from V_{DDH} to V_{DD}. A comparison between the 5-Tr class-G and 6-Tr class-G PA shows that the 5-Tr class-G can achieve much lower P_{SW}. This is because M_{P3} is removed and the size of M_{N3} is reduced. P_{SW} is reduced by half at peak V_{OUT}, and by 30% at half of peak V_{OUT} where the entire capacitor array switches at $V_{DDH} - GND$ and $V_{DD} - GND$, respectively. From an area perspective, the 5-Tr class-G PA can reduce the area by 28% relative to the 6-Tr class-G PA, based on transistor sizes alone.

IV. STACKED CLASS-G POWER AMPLIFIER

In order to implement a class-G PA, an additional power supply of V_{DD} is required. The extra supply voltage can be implemented by using a linear voltage regulator or DC-DC converter (Fig. 1). A DC-DC converter is preferred than a linear voltage regulator due to better efficiency. However, the efficiency-drop still exists and the output structure of
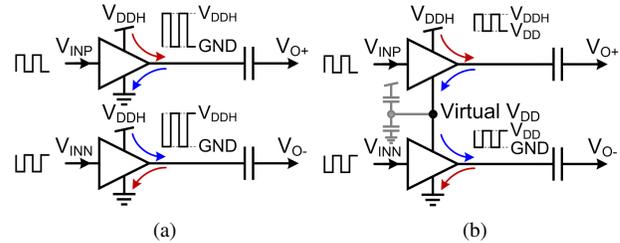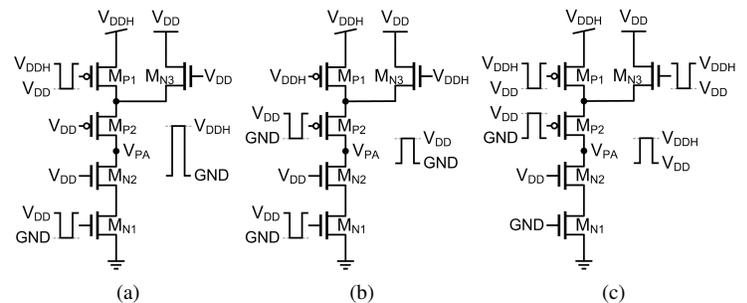
DC-DC converter has to be sufficiently large to source the PA. Moreover, a DC-DC converter typically requires large inductors to achieve high efficiency, which can increase cost.

Inherent class-G operation can be implemented by stacking two PAs. Stacked PAs can employ half of main supply voltage without using an extra power supply voltage. However, stacked designs typically require additional devices to switch between the supply and ground paths [11]. Furthermore, these devices have to be very large to minimize resistive losses.

The proposed class-G design (Section III) can be used to implement a stacked PA, that can avoid the requirement for extra switches for switching the supply and ground paths. In a PA design, a pseudo-differential design is commonly used to increase the output power by 6-dB, as well as to reduce the sensitivity to supply and ground inductance. Fig. 7 shows the stacked differential PA structure for full supply-voltage (V_{DDH}) and half supply-voltage (V_{DD}) switching. The V_{DDH} level switching operation is identical to a typical single supply voltage PA. For V_{DD} switching, the upper PA switches between V_{DDH} and V_{DD}, and the lower PA switches between V_{DD} and GND. When V_{INP} is high and V_{INN} is low, the current flows from V_{DDH} to V_{O+}, and from V_{O-} to GND, respectively. When the V_{INP} is low and V_{INN} is high, the current flows from V_{O+} to V_{O-} through the V_{DD} path. Since only an ac signal is transferred, the output power is same for the upper and lower PAs, if the voltage swing is identical. Thus, the virtual V_{DD} level is set to half of V_{DDH} automatically. To enable this stacked class-G operation without extra supply path switches, the proposed class-G PA has to
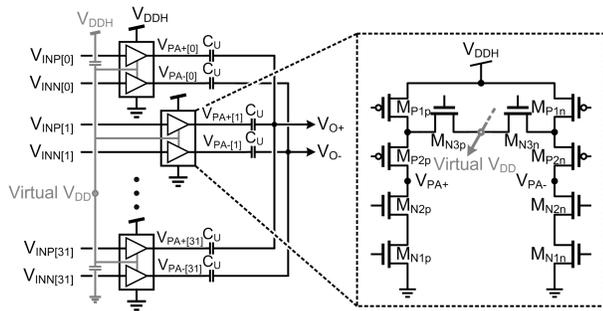
Fig. 9: Stacked class-G switched capacitor PA and schematic of stacked differential PA unit.
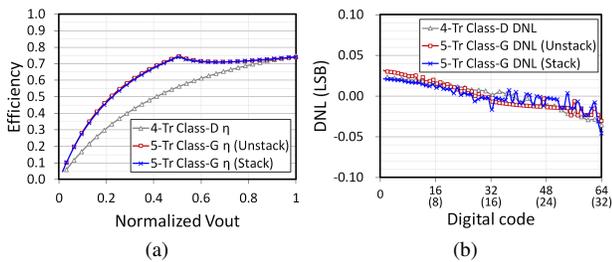

Fig. 10: Performance of stacked class-G SCPA. (a) Efficiency. (b) DNL.

switch between V_{DDH} and V_{DD} as well as V_{DD} and GND.

The multi-level driving sequence for stacked class-G operation is shown in Fig. 8. It is noted that the V_{DD} supply in Fig. 8 uses a virtual V_{DD} in the stacked class-G implementation. The driving signals for $V_{DD} - GND$ switching are the same as the prior class-G design, but the gate of M_{P2} is driven by the same signal that is used to drive M_{P3} in a 6-Tr class-G PA (Fig. 3b). The driving signals for $V_{DDH} - V_{DD}$ switching are implemented by appropriately switching M_{P1}, M_{P2}, and M_{N3} (Fig. 8c). The charge flows from V_{DDH} to V_{PA} by turning on M_{P1} and M_{P2}, and flows from V_{PA} to V_{DD} by turning on M_{P2} and M_{N3}. The source and drain connection of M_{P2} is reversed when the charge flows from V_{PA} to V_{DD}, in which case the potential of the body node is lower than the potential of the source node of M_{P2} (V_{PA}) by $I_{OUT} \cdot r_{on.P2}$. However, this voltage drop can be made negligible by using a sufficiently low on-resistance, so that it cannot turn on the PN body diode. The maximum simulated voltage drop across the M_{P2} source-to-body junction is only 45.5 mV, using the parameters in Table I. Although M_{P2} and M_{N3} can both source and sink the current by adding the $V_{DDH} - V_{DD}$ switching, the gate driver for these devices can use the existing drivers because the gate switching level of M_{P2} and M_{N3} remains the same as that used for $V_{DDH} - GND$ or $V_{DD} - GND$ switching.

The full design of the stacked class-G SCPA and the schematic of differential PA unit are shown in Fig. 9. The same 5-bit unary differential SCPA as above is used, but the supply voltage for V_{DD} at PA is removed and the V_{DD} nodes are connected together. The differential PA unit is comprised of two 5-Tr class-G PAs, but the driving signals for V_{INP} and V_{INN} are changed during half supply voltage level (V_{DD}) switching

such that V_{INP} is driven by the $V_{DD} - GND$ switching driver (Fig. 8b) and V_{INN} is driven by the $V_{DDH} - V_{DD}$ switching driver (Fig. 8c).

The drain efficiency and DNL of the stacked class-G PA are simulated and the results are compared with a 4-Tr class-D PA and an unstacked 5-Tr class-G PA using V_{DD} supply voltage (Fig. 4) as shown in Fig. 10. The drain efficiency is almost identical to the unstacked design. However the key advantage of the approach is that the V_{DD} supply in the PA is avoided by using the stacked PA approach. Thus, the efficiency can be greatly improved by adding a single NMOS FET (M_{N3}) in a cascoded 4-Tr class-D PA structure with multi-level driving signals. In addition, the linearity is also comparable to 4-Tr class-D PA because the on-resistance of V_{DD} path is still well matched with the V_{DDH} and GND paths.

While the proposed approach has been described in a SCPA, it can be applied to any switching RF PA architecture that employs a class-D PA such as approaches based on RF pulse-width-modulation [8] or digital outphasing [9].

V. CONCLUSION

An efficient class-G stage based on a class-D PA for switching RF PAs is described. The proposed approach can enhance efficiency compared to a cascoded class-D or a 6-Tr class-G design employed in prior work. By using the multi-level driving sequence in a stacked approach, the requirement for any additional supply for class-G stage is avoided. The proposed class-G PA when used in an SCPA shows improved efficiency over almost the entire output power range, compared to prior approaches. The proposed design can be applied to any switching RF transmitter architecture that uses class-D PAs.

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