85-to-127 GHz CMOS Signal Generation Using a Quadrature VCO With Passive Coupling and Broadband Harmonic Combining for Rotational Spectroscopy

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***Abstract*—A quadrature LC-VCO incorporating passive coupling and broadband harmonic combining for frequency multiplication by 4, and NMOS switched variable inductors is fabricated in 65 nm bulk CMOS to generate signals at 85 to 127 GHz. The passive quadrature coupling bypasses the need for a broadband on-chip bias-T, while reducing power consumption, phase noise, and the theoretical conversion loss for the 4th order harmonic generation by 3 dB over the linear superposition. The 39% frequency tuning range is at least 4x higher than the other CMOS implementations with center frequency over 90 GHz. At power consumption of 30–45 mW from a 1.5 V power supply, the measured output power varies from −15 to −23 dBm and phase noise at 10 MHz offset varies from −108 to −102 dBc/Hz over the output frequency range. These are sufficient for use in millimeter wave rotational spectroscopy.**

***Index Terms*—CMOS, frequency multiplication, passive coupling, quadrature voltage controlled oscillator, millimeter wave, rotational spectroscopy, wide frequency tuning range.**

I. Introduction

ELECTRO-MAGNETIC waves in the millimeter and sub-millimeter wave frequency range (100 to 1000 GHz) are being utilized in fast-scan rotational spectroscopy for detection and identification of gas molecules [1]. This technique can be used for monitoring indoor air quality, gas leaks, human breath, and others for a wide variety of safety, security and medical applications. Advances of the high frequency capability of CMOS [2] have made it possible to consider CMOS as an affordable means for implementing the electronics for these spectroscopy systems, in which a signal generation circuit operating at ∼100 GHz and higher with an ultra-wide frequency tuning range (∼50%) is a key component. The rotational spectroscopy application is particularly well suited for CMOS implementation because it requires only a few micro-watt of transmitted power to avoid the saturation of molecules [1]. This is significantly different from communication or radar applications in which much higher transmitted power is needed.

In recent years, numerous millimeter-wave CMOS signal generation circuits/LC oscillators have been reported [2]–[16]. These works can be categorized into three groups based on their design target. The first is generation of signals at frequencies as high as possible [2]–[7]. A 300 GHz fundamental mode VCO in 65 nm CMOS [6] demonstrated that the fundamental output frequency of an oscillator can indeed approach the $f_{\max}$ of technology. By employing a frequency multiplication technique in conjunction with an oscillator, signals can be generated beyond $f_{\max}$. As an example, a 553 GHz signal was generated by using a 4-push technique in 45 nm CMOS [7]. The second is increasing the tuning range while minimizing phase noise degradation [8]–[15]. A 57.5–90.1 GHz oscillator was reported [10]. A 44%-tuning range including a ∼2 GHz wide output frequency gap was reported using a magnetically-tuned multi-mode technique. The third focus has been increasing the output power. For example, a 283-to-296 GHz VCO in 65 nm CMOS with 0.76 mW peak output power [16] has been demonstrated. It showed that using a triple-push technique, the output power of CMOS signal generation circuit can be significantly improved at the sub-millimeter wave frequencies.

However, all reported wide tuning millimeter wave CMOS signal generation circuits with a frequency tuning range larger than 20% operate below 90 GHz. At ∼100 GHz, the tuning range has been limited to less than 11% [12]–[16], which is far below the desired. Approaches are needed to dramatically increase the tuning range of signal generation circuits with output frequency greater than 100 GHz.

This paper presents a CMOS signal generation circuit that outputs signals from 85 to 127 GHz (∼40% frequency tuning range) without a frequency gap. For spectroscopy at frequencies over 200 GHz, as illustrated in Fig. 1, this circuit (in the dashed box) needs to be cascaded with a broadband amplifier and a frequency doubler. To overcome the tuning range limitation of [7], the circuit uses an LC-VCO incorporating passive quadrature coupling and broadband harmonic combining

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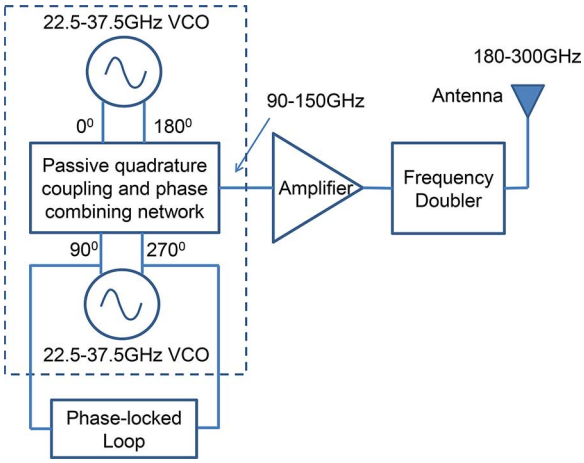

Fig. 1. Signal generation scheme for 180–300 GHz rotational spectroscopy.

for frequency multiplication by 4, and NMOS switched variable inductors. An analytical analysis shows that the proposed harmonic generation scheme has 3 dB lower fundamental-to-4th harmonic conversion loss than that of the linear superposition technique in [5].

The circuit was fabricated in 65 nm bulk CMOS. It generates signals with a measured output power level of ~ -15 to ~ -23 dBm and phase noise of ~ -108 to ~ -102 dBc/Hz at 10 MHz offset. The phase noise performance is sufficient for rotational spectroscopy. This circuit has at least 4x wider tuning range than the previously reported CMOS circuits that operate above 90 GHz [12]–[16], and has more than 5 dB higher output power and ~ 2 dB lower phase noise than those of the 57.5 to 90.1 GHz fundamental CMOS oscillator [10] at the same output frequencies (85 to 90 GHz) and power efficiency.

The rest of this paper is organized as follows. Section II discusses the signal generation architecture for rotational spectroscopy including its frequency plan. Section III presents circuit design considerations. Specifically, detailed analyses of the proposed passive quadrature coupling and broadband harmonic combining are presented. Section IV discusses circuit implementation and measurement results. Conclusions are drawn in Section V.

II. Signal Generator Architecture

A frequency tuning range of $\sim$50% at 100 GHz and higher desired for rotational spectroscopy is challenging for any electronic technologies including CMOS. The difficulty is due to the trade-off between frequency tuning and operation frequency arising from the fact that the capacitance of transistors needed to sustain operation becomes an increasing portion of the capacitance of LC tank that determines the operation frequency. This is exacerbated by the fact that the quality factor of varactors and the parasitic capacitance of transistors degrade with frequency which further increases the width of transistors needed to sustain oscillation and thus their capacitance. Because of this, most of CMOS signal generation circuits with fundamental oscillation frequencies above 90 GHz use small varactors [13]–[15], or even no varactors [16]. Recently, magnetic frequency tuning techniques based on transformers and varactors have been reported [10], [11], and as mentioned, used to demonstrate a 57.5–90.1 GHz oscillator [10]. However, these circuits [10], [17] quite often exhibit frequency tuning gaps.

These limitations could be mitigated by generating signals at relatively lower frequencies at first, where ultra wide frequency tuning can be more easily achieved. Then broadband frequency multiplication techniques can be applied to generate signals at the desired frequencies. Since frequency multiplication adds loss, it is critical to generate the signal at as high of frequency as possible.

Based on these considerations, a frequency generation scheme suitable for the 180–300 GHz rotational spectroscopy [1] is proposed and illustrated in Fig. 1. A critical component for this system is a VCO operating at low end of the millimeter wave frequency range generates fundamental signals at 22.5 to 37.5 GHz. Second, two identical VCO's are mutually coupled with a passive quadrature coupling and a phase combining network to generate a 4th-order harmonic at frequencies between 90 and 150 GHz. For frequency synthesis, a phase-locked loop can be used to lock the fundamental output of VCO. Thus, this scheme not only relaxes the requirement on high-frequency wide-tuning oscillator design, but also mitigates the PLL design challenges since it only needs to lock signals at 22.5 to 37.5 GHz.

Other than the 50% tuning range requirement, the phase noise of transmitted signal should be less than -88 dBc/Hz at 10 MHz offset for a 120 GHz carrier, and the signal power should be in the range between -20 and -30 dBm. The phase noise and output power specifications are not as demanding as that of other millimeter wave applications such as 60 GHz wireless communication and 77 GHz long range radars. The phase noise can broaden the widths of gas lines in a spectrum. These specifications are empirically derived from the characteristics of components in the sub-millimeter spectrometers at Dr. Frank De Lucia's laboratory of the Ohio State University [1].

III. Proposed Circuit Architecture

Fig. 2 shows the proposed signal generation circuit. Two identical wide tuning oscillators incorporating a variable inductor and varactors with cross-coupled core transistors ($\mathrm{M_{C1-4}}$) are quadrature coupled through four transistors ($\mathrm{M_{CPL1-4}}$) with source inductors ($\mathrm{L_{S1-4}}$). The dc bias current through the coupling transistors is zero. The 4th-order harmonics are combined and ac-coupled to a 50 Ω output load, R_{L} through a 300-fF coupling capacitor, $\mathrm{C_C}$.

A. LC Tank With a Wide Frequency Tuning Range

Fig. 3 shows the schematic of the wide-tuning LC VCO that forms the core of quadrature coupled VCO in Fig. 2. It contains a 3-bit binary-weighted accumulation-mode MOS varactor bank and an NMOS switch based tunable differential inductor that reduces VCO gain while increasing frequency tuning [18], [19], [22]. It is formed by cascading four inductor loops with three NMOS switches (SW1, SW2 and SW3) between two adjacent sections. The layout of the NMOS switch based tunable differential inductor is also depicted in Fig. 3. Since the effective tank inductance looking into the differential port mostly relies on the self-inductance of each section rather than mutual inductance,

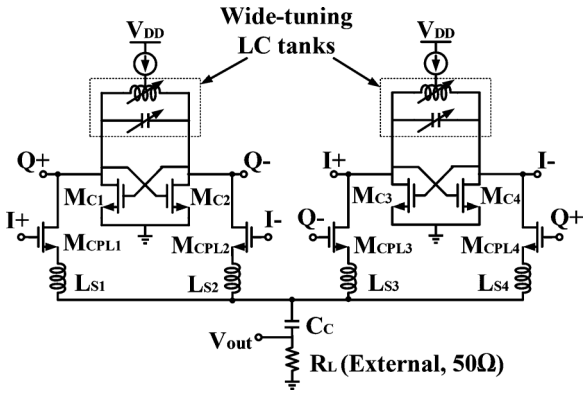

Fig. 2. Proposed signal generation circuit: wide-tuning LC VCO's coupled with a passive quadrature coupling and phase combining network.

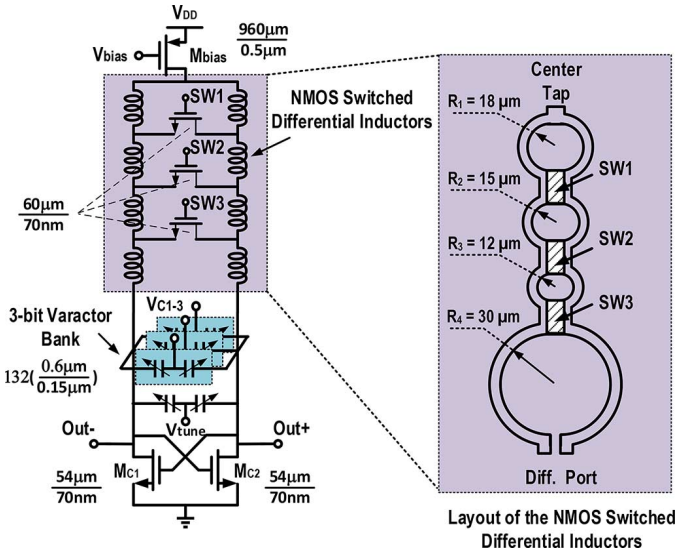

Fig. 3. Schematic of the wide tuning LC VCO and the layout of the NMOS switched differential inductors.

it is straightforward to design and implement. Moreover, since the switches are on differential nodes, the effective series resistance adding to the tank inductance is only a half of the on-resistance of NMOS switches [20], which helps to mitigate the Q degradation.

Selecting the switch size involves a trade-off between tank Q and frequency tuning range. A larger switch has smaller on-resistance but larger parasitic capacitance. A smaller on-resistance helps to mitigate the inductor Q degradation, but the associated larger parasitic capacitance prevents the switch from being fully turned off, thus limiting the frequency tuning. The switches were sized to have $\sim$5-Ω on-resistance so that the resistance is not the dominant factor determining the overall tank Q. The switches are biased at the half of V_{DD} or 0.75 V. Gate voltage of 2.2 V or gate to source voltages of 1.45 V is applied for the NMOS switches to lower the on-resistance.

It should be noted that the number of inductor bands (N) is determined by the desired frequency tuning ratio $(f_{\max}/f_{\min})$ and the maximum tank capacitance to minimum tank capacitance ratio $(C_{\text{tank\_max}}/C_{\text{tank\_min}})$. These also determine the desired inductance ratio for adjacent bands (L_n/L_{n+1}). Their relationships are

$$\frac{C_{\text{tank\_max}}}{C_{\text{tank\_min}}} \geq \left(\frac{f_{\max}}{f_{\min}}\right)^{\frac{2}{N}} = \frac{L_n}{L_{n+1}}. \quad (1)$$

Since the oscillation frequency range target was 22.5 to 37.5 GHz, and the accumulation-mode MOS varactor used has a maximum capacitance to minimum capacitance ratio of $\sim$3, the number of inductor bands was set to four. The minimum required $C_{\text{tank\_max}}/C_{\text{tank\_min}}$ is $\sim$1.3. This in conjunction with the varactor tuning ratio of 3 allows the use of a larger cross-coupled NMOS pair with necessary gain to compensate the tank loss, while providing sufficient frequency overlap between adjacent inductor bands.

The inductors were simulated and modeled using a 3-D EM simulator, ANSYS HFSS. The total dielectric layer thickness between the top copper layer and substrate is $\sim$4.5 μm. The substrate resistivity is $\sim$10 $\Omega\cdot$ cm. Since the thickness of top copper layer is less than 1 μm, the differential switched inductor trace was implemented using the aluminum pad layer ($\sim$1 μm) stacked with the top copper layer to increase its Q-factor. The switch settings for different inductor bands and their simulated inductance and Q-factors (differential Q and including the switch losses), as well as the overall tank Q are summarized in Table I. The inductor without switches has a Q-factor of $\sim$15. With the switches, the effective Q-factor degrades to $\sim$10, and the minimum self-resonant frequency is $\sim$70 GHz (with all the switches off). The effective Q-factor of inductors including switches is approximately flat over the bands. This is due to the fact that the Q-factor of inductor is higher at higher frequency in combination with the fact that the switch resistance accounts for a bigger portion of the overall series resistance of inductor setting for higher frequency bands. The overall tank Q ranges from 3.3 to 5. The tank-Q at higher frequency band is determined by that for varactors and the impact of Q degradation due to the NMOS switches is reduced.

B. Passive Quadrature Coupling and Phase Combining Network

The coupling and phase combining networks in Fig. 2 look similar to the 4-push structure proposed in [7] at a glance. It however is a new design incorporating several unique features. First, the coupling network does not require DC power while providing the mutual injection locking paths between the two tanks, and forcing them to run in quadrature phases, similar to that in conventional transistor-coupled quadrature VCO's. This not only reduces the power consumption but also reduces phase noise, because the coupling transistors with zero bias contribute the minimum noise. More importantly, this passive combining eliminates the need for a broadband bias tee shown in Fig. 4. The bias-T inductance L needs to be at least 1 nH to provide impedance of $\sim$600 Ω at 100 GHz and should be low loss. It is challenging if not almost impossible to realize such an on-chip inductor with self-resonant frequency greater than 100 GHz not to mention over 200 GHz needed. On top of this, the bias-T inductance and the parasitic capacitance C_{par} associated with the

TABLE I
INDUCTOR BAND SETTINGS, SIMULATED INDUCTANCE AND Q-FACTORS

Band	Differential Inductor Switch Setting			Simulated Diff. Ind. (pH)	Simulated Inductor Q-factor[(a)] (Stacked M7 and ALCAP)	Simulated Inductor Q-factor[(a)] (M7 only)	Simulated Minimum Tank Q-factor
	SW1	SW2	SW3				
Band1	Off	Off	Off	300	8.8@23GHz	7@23GHz	5@23GHz
Band2	On	Off	Off	233	8.6@27GHz	7.2@27GHz	4@27GHz
Band3	On	On	Off	181	9.7@32GHz	8.3@32GHz	3.5@32GHz
Band4	On	On	On	140	10.3@36GHz	8.9@36GHz	3.3@36GHz

(a) Q-factor is computed using (-Im(Y_{11})/Re(Y_{11})).

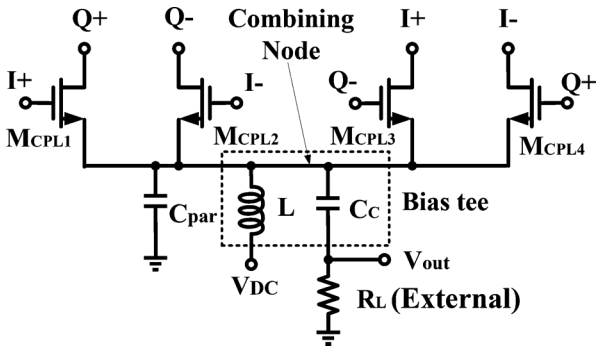

Fig. 4. Combining network with a bias-tee.

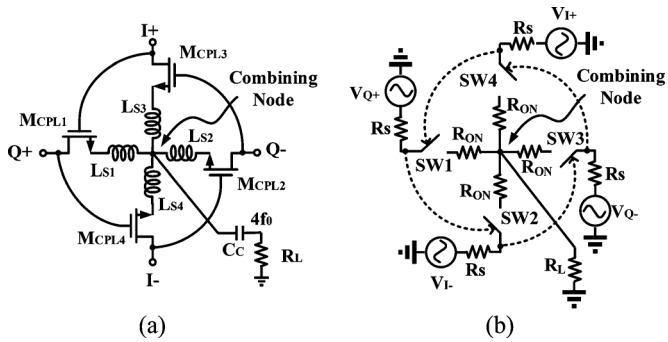

Fig. 5. (a) Quadrature coupling and phase combining network, and (b) its simplified circuit.

combining node form an LC tank that limits the signal bandwidth and increases the frequency dependence of output power. Because of these, it is highly desirable to not use an on-chip bias Tee, and the proposed passive coupling network completely bypasses this problem.

Second, the coupling network forms a passive quadrature-phase sub-harmonic mixer that performs frequency multiplication by 4. To understand this mixing effect, the network is redrawn as shown in Fig. 5(a). In order to glean design insights, the circuit is further simplified as illustrated in Fig. 5(b), where the zero-biased coupling transistors are replaced by four switches with ideal switching characteristics (turn on fully when the switch control voltage is larger than zero). The switches have an on-resistance, R_{ON} and infinite off-resistance. The source inductors in the combining network are removed to simplify the analysis. The four input ports are driven by four voltage sources ($\mathrm{V_{Q+}}$, $\mathrm{V_{Q-}}$, $\mathrm{V_{I+}}$, and $\mathrm{V_{I-}}$) with a finite source resistance, R_S, and the network delivers power to the external load resistance, R_L on the combining node.

Assuming the four voltage sources have a signal amplitude of A at frequency ω and source impedance of $R_S$with quadrature phases, i.e.,

$$\begin{cases} V_{Q+} : \mathrm{A} \cdot \sin(\omega t) \\ V_{Q-} : \mathrm{A} \cdot \sin(\omega t - \pi) \\ V_{I+} : \mathrm{A} \cdot \sin(\omega t - \frac{3\pi}{2}) \\ V_{I-} : \mathrm{A} \cdot \sin(\omega t - \frac{\pi}{2}). \end{cases} \tag{2}$$

The effective voltage waveforms ($\mathrm{V_{1-4}}$) at the source nodes of switches assuming ideal switching will be determined by a multiplication of a sine wave and a square wave (from 0 to 1) with a quadrature phase relative to the sine wave. By using the Fourier series representation of square wave, the four effective source voltage waveforms are as shown in (3) at the bottom of the page.

$$\begin{cases} V_1 = [R_\mathrm{L}/(2R_\mathrm{L} + R_\mathrm{S} + R_\mathrm{ON})] \cdot \mathrm{A} \cdot \sin(\omega t) \left[\frac{1}{2} + \frac{2}{\pi} \sum\limits_{n=1}^{\infty} \frac{1}{2n-1} \sin\left((2n-1)\left(\omega t - \frac{\pi}{2}\right)\right)\right] \\ V_2 = [R_\mathrm{L}/(2R_\mathrm{L} + R_\mathrm{S} + R_\mathrm{ON})] \cdot \mathrm{A} \cdot \sin\left(\omega t - \frac{\pi}{2}\right) \left[\frac{1}{2} + \frac{2}{\pi} \sum\limits_{n=1}^{\infty} \frac{1}{2n-1} \sin\left((2n-1)(\omega t - \pi)\right)\right] \\ V_3 = [R_\mathrm{L}/(2R_\mathrm{L} + R_\mathrm{S} + R_\mathrm{ON})] \cdot \mathrm{A} \cdot \sin(\omega t - \pi) \left[\frac{1}{2} + \frac{2}{\pi} \sum\limits_{n=1}^{\infty} \frac{1}{2n-1} \sin\left((2n-1)\left(\omega t - \frac{3\pi}{2}\right)\right)\right] \\ V_4 = [R_\mathrm{L}/(2R_\mathrm{L} + R_\mathrm{S} + R_\mathrm{ON})] \cdot \mathrm{A} \cdot \sin\left(\omega t - \frac{3\pi}{2}\right) \left[\frac{1}{2} + \frac{2}{\pi} \sum\limits_{n=1}^{\infty} \frac{1}{2n-1} \sin\left((2n-1)(\omega t)\right)\right] \end{cases} \tag{3}$$

Because at any given time, two of the four switches are simultaneously turned on, $R_L/(2R_L + R_S + R_{\rm ON})$ is needed to account for the voltage division between $R_S + R_{\rm on}$ and R_L in parallel with $R_S + R_{\rm on}$. The total output voltage on the combining node is then the sum of four effective source voltage waveforms:

$$\begin{aligned} \mathrm{V}_L &= (V_1 + V_2 + V_3 + V_4) \\ &= -\frac{32R_L}{2R_L + R_S + R_{\rm ON}} \cdot \mathrm{A} \cdot \sum_{n=1}^{\infty} \frac{n \cdot \cos\left(4n\omega t + \frac{\pi}{2}\right)}{(4n-1)(4n+1)\pi} \\ &= -\frac{32R_L}{15\pi(2R_L + R_S + R_{\rm ON})} A\cos\left(4\omega t + \frac{\pi}{2}\right) \\ &\quad - \frac{64R_L}{63\pi(2R_L + R_S + R_{\rm ON})} A\cos\left(8\omega t + \frac{\pi}{2}\right) - \cdots. \end{aligned} \tag{4}$$

Equation (4) shows that, after phase combining, all harmonics except $4n$th order $(n = 1, 2, 3, \ldots)$ are cancelled. The 4th harmonic power delivered to the load will be

$$P_{4\mathrm{th}_{\rm harmonic}} = \left(\frac{R_L}{2R_L + R_S + R_{\rm ON}}\right)^2 \left(\frac{16\sqrt{2}}{15\pi}\right)^2 \left(\frac{A^2}{R_L}\right). \tag{5}$$

This power is maximized when $R_L = (R_S + R_{\rm ON})/(2)$, and is

$$P_{4\mathrm{th}_{\rm harmonic},\max} = \left(\frac{16\sqrt{2}}{15\pi}\right)^2 \times \frac{A^2}{8(R_S + R_{\rm ON})}. \tag{6}$$

The total available fundamental power from the four signal sources is

$$P_{\rm avs,fund.} = 4 \times \frac{A^2}{8R_S} = \frac{A^2}{2R_S}. \tag{7}$$

When switches are lossless ($R_{\rm ON} = 0$), from (6) and (7), the theoretical maximum fundamental-to-4th order harmonic power conversion efficiency is

$$\begin{aligned} \text{Power Conversion Efficiency} &= \frac{P_{4\mathrm{th}_{\rm harmonic},\max}}{P_{\rm av,fund.}} \\ &= \left(\frac{8\sqrt{2}}{15\pi}\right)^2 = 5.76\% \end{aligned} \tag{8}$$

In another words, the minimum fundamental-to-4th order harmonic power conversion loss is $-10\log((8\sqrt{2})/(15\pi))^2 = 12.4$ dB. This conversion loss is 3 dB lower than that resulting from the linear superposition technique in [5]. To double check the results, a behavioral simulation using ideal switches and resistors has been performed in Cadence Spectre and the result is identical to that from the analysis.

Fig. 6 illustrates the quadrature mixing for this 4x frequency multiplication. Fig. 7 shows the fundamental-to-4th order harmonic power conversion loss as a function of R_L/R_S computed using Matlab assuming $R_{\rm ON} = 0$. As suggested, the conversion loss is minimized when $R_L = R_S/2$. Fig. 8 shows the fundamental-to-4th conversion loss versus the phase shift between the input sine wave and the switch control voltage. The quadrature phase relationship between the input sine wave and switch control voltage results the minimum conversion loss.

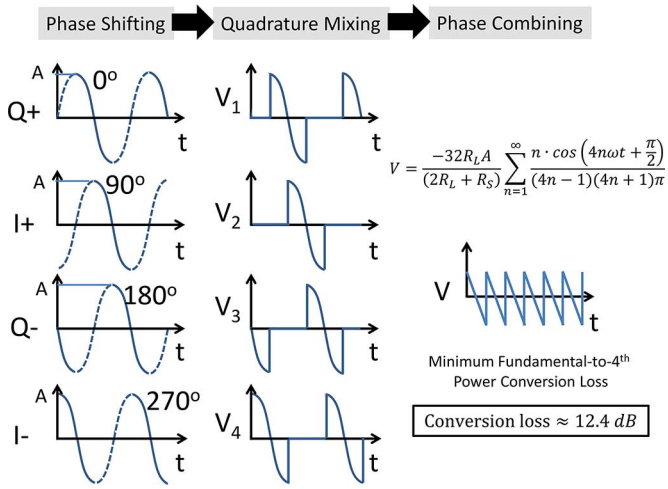

Fig. 6. Quadrature mixing for frequency multiplication by 4.

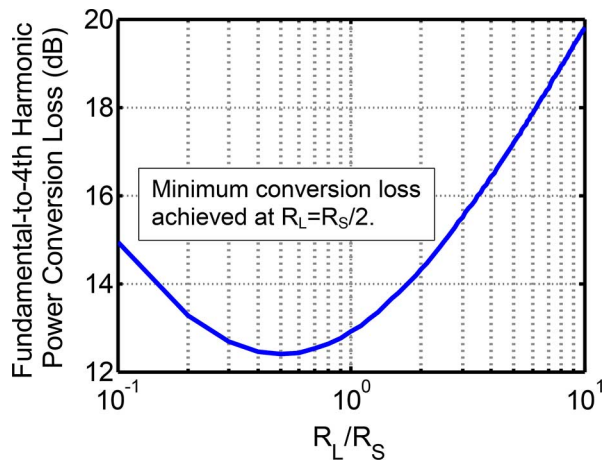

Fig. 7. Fundamental-to-4th harmonic power conversion loss versus R_L/R_S.

Fig. 9 shows a simulated waveform of source current flowing through one of the coupling transistors. It contains a rich set of harmonics due to the nonlinear operation of coupling transistors. After phase combining, all harmonics other than $4n$th orders $(n = 1, 2, 3\ldots)$ are cancelled [7]. Additionally, because the 8th and higher order harmonics are attenuated by the frequency response of combining network, as illustrated in Fig. 10, only the signal at the 4th order harmonic frequency is present at the output.

The size choice of coupling transistor involves a trade-off between oscillation frequency and output power (Fig. 11). This is due to the fact that a larger size coupling transistor gives lower on-resistance but more parasitic capacitance. The width ratio of coupling transistor to core transistor $(\mathrm{W_{CPL}/W_C})$ was selected to be 0.75. Four additional source inductors $(\mathrm{L}'_S\mathrm{s})$ were added in the network (Fig. 2). The primary purpose of adding the source inductors is to resonate out the parasitic capacitance of 4th harmonic on the combining node, and to increase the nonlinearity in the switch operation, so that more power can be generated and delivered to the load at the 4th harmonic frequency. Moreover, the source inductors change the phase of the injected current in such a way that it is now partially in-phase with the tank voltage. As illustrated in Fig. 12, without the source inductor,

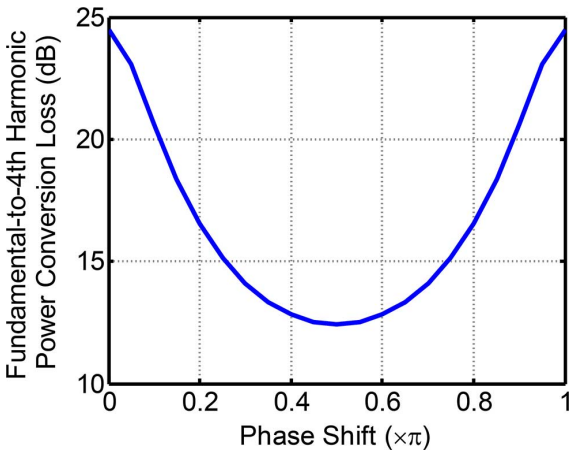

Fig. 8. Fundamental-to-4th harmonic conversion loss versus phase shift between the drain and gate voltages of switch when $R_L = R_S/2$.

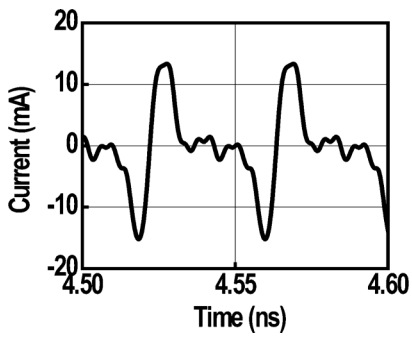

Fig. 9. Simulated waveform of source current through a coupling transistor.

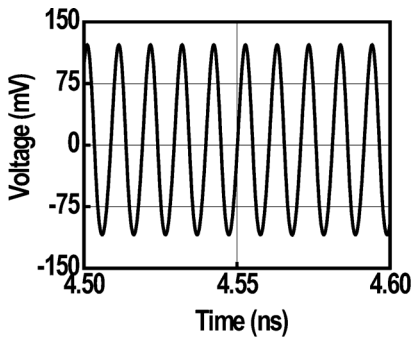

Fig. 10. Simulated voltage waveform at the combining node.

the injection current $\mathrm{I_{inj}}$ is in-phase with $\mathrm{V_Q}$ (since $\mathrm{V_Q}$ is the same as $\mathrm{V_{GS}}$), thus 90 degree out-of-phase with the tank voltage $\mathrm{V_I}$. This orthogonal injection forces the oscillation frequency to deviate from the resonant frequency of tank, thus degrading the phase noise. Adding the source inductors shifts the phasor of injection current $\mathrm{I_{inj}}$ toward the phasor of tank voltage, $\mathrm{V_I}$. This results in a component of injection current that is in-phase with the tank voltage, which helps to decouple the trade-off between quadrature phase accuracy and phase noise, thus reducing phase noise. Fig. 13 shows the simulated output power versus source inductance. An optimal value of ~30 pH was chosen to maximize the power in the band with the lowest output power.

The simulated 4th harmonic output power delivered to a 50 Ω load is about −10 dBm. This in conjunction with the VCO

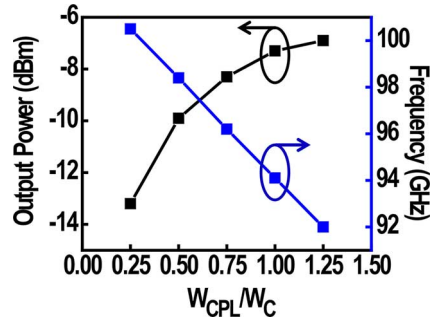

Fig. 11. Simulated output frequency and power vs. $\mathrm{W_{CPL}/W_C}$.

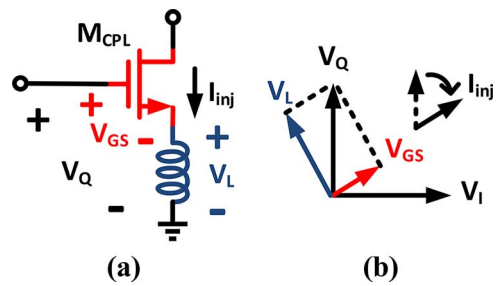

Fig. 12. Illustration of injection current phase. (a) Schematic and (b) phasor diagram.

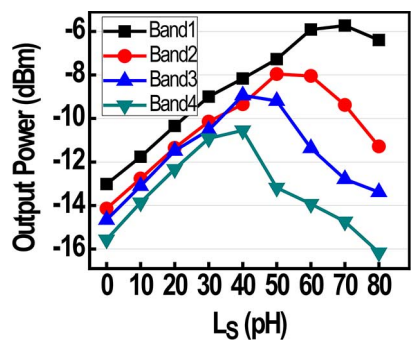

Fig. 13. Simulated output power vs. $\mathrm{L_s}$ in four different bands.

output resistance of 40 Ω estimated from the load-pull (resistive) simulation and fundamental VCO signal swing of 1 V means the power conversion loss is ~15 dB. In the load pull simulation, the load resistance was swept downwards from 100 Ω. An optimum load resistance was identified when the delivered power is maximized. Assuming $R_L = R_S/2$ (since two switches are on at a time), R_S is estimated.

Compared to the analytical conversion loss of 12.4 dB, the discrepancy is less than 3 dB. This discrepancy is attributed to the parasitics including the on-resistance and capacitances of transistors, the finite threshold voltage and the transistor non-idealities that were not taken into account in the simple analysis.

Lastly, the phase combining node is self-biased at half $\mathrm{V_{DD}}$ and its voltage swing is much smaller than that of fundamental due to the rejection of harmonics except the $4n$th ones. Therefore, the gate voltages of the coupling transistors ($\mathrm{M_{CPL1-4}}$) do not have to be higher than $\mathrm{V_{DD}}$ to turn on the transistors, and additional AC coupling capacitors and a bias network are not needed. Furthermore, the combining node is a virtual ground to

the fundamental signals, thus the impact of output load, R_L to the tank Q is reduced.

C. I/Q Mismatch Analysis

As discussed, only the $4n$th ($n = 1, 2, 3, \ldots$) harmonics can be generated at the combining node. However, any amplitude or phase mismatches between the in-phase and quadrature-phase signals will cause the output power leaking into other undesired harmonics and will lower the 4th harmonic conversion efficiency. With an amplitude mismatch, ΔA and phase mismatch, $\Delta\phi$, (3) can be amended as shown in (9) at the bottom of the page.

From (4), (6), and (9), the output harmonic power conversion ratio (defined as the harmonic power delivered to the load divide by the total available fundamental power from the VCO) versus the phase and amplitude mismatches are calculated. The results are shown in Figs. 14(a) and (b), respectively. The 2nd and 6th harmonics are the dominant harmonic leakage terms when the amplitude and phase mismatches are present. The 2nd and 6th harmonics increase rapidly with small amplitude mismatch and phase mismatch, but they saturate at larger mismatches. Even with a 6% amplitude mismatch or a 2-degree phase mismatch, the 2nd and 6th harmonic power is at least 20 dB lower than the 4th order harmonics power, and the 4th harmonic power is insensitive to the I/Q mismatch.

IV. Implementation and Measurement Results

The signal generation circuit was implemented in 65 nm bulk CMOS and Fig. 15 shows a die photograph of the test chip. The layout was optimized for symmetry to minimize mismatches. L_s's were implemented using only the top copper layer. Stacking with the aluminum pad layer for the source inductors was not practical due to the minimum width design rule for the aluminum layer (the size of source inductors was too small to be implemented by the aluminum layer with a minimum width of ~ 5 μm). The current from the coupling transistors was combined in the middle. Thanks to a butterfly style layout of the source inductors in Fig. 16, the combining network occupies only a small additional area. A 50 Ω Grounded CPW (GCPW) was implemented using the aluminum layer to route the combined signal to a GSG pad for measurements. The overall chip size is 1000 μm $\times$ 550 μm including the pads.

As illustrated in Fig. 17, an Agilent N9030A PXA Signal Analyzer, an Agilent 11970W harmonic mixer, an Agilent E8257D Signal Generator, and a VDI WR6.5 sub-harmonic mixer were used for output spectrum measurement in W and D-band, respectively. A VDI WR10 Amplifier Multiplier Chain, A VDI PM4 Erickson Power Meter, and an Agilent E8361A PNA plus an N5260-60003 Frequency Extension Module were used to calibrate the power loss in the measurement setup including those for the probes, cables, adapter and mixers.

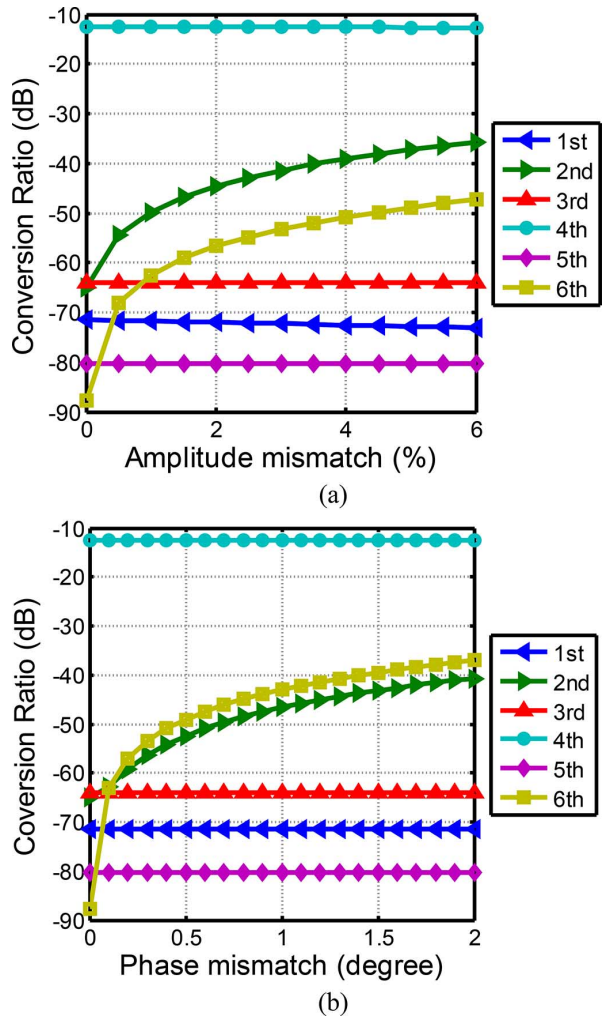

Fig. 14. Harmonic power conversion ratio versus (a) amplitude mismatches, and (b) phase mismatches when $R_L = R_S/2$.

Fig. 18 shows the measured frequency tuning range for all bands. The bias current for the circuit was set to be $\sim$20 mA in total except for the "band 3 high bias" and "band 4 high

$$
\begin{cases}
V_1 = [R_{\rm L}/(2R_{\rm L} + R_{\rm S} + R_{\rm ON})] \cdot {\rm A} \cdot \sin(\omega t) \left[\frac{1}{2} + \frac{2}{\pi}\sum\limits_{n=1}^{\infty} \frac{1}{2n-1} \sin\left((2n-1)\left(\omega t - \frac{\pi}{2} - \Delta\phi\right)\right)\right] \\
V_2 = [R_{\rm L}/(2R_{\rm L} + R_{\rm S} + R_{\rm ON})] \cdot ({\rm A} - \Delta A) \cdot \sin\left(\omega t - \frac{\pi}{2} - \Delta\phi\right) \left[\frac{1}{2} + \frac{2}{\pi}\sum\limits_{n=1}^{\infty} \frac{1}{2n-1} \sin\left((2n-1)(\omega t - \pi)\right)\right] \\
V_3 = [R_{\rm L}/(2R_{\rm L} + R_{\rm S} + R_{\rm ON})] \cdot A \cdot \sin(\omega t - \pi) \left[\frac{1}{2} + \frac{2}{\pi}\sum\limits_{n=1}^{\infty} \frac{1}{2n-1} \sin\left((2n-1)\left(\omega t - \frac{3\pi}{2} - \Delta\phi\right)\right)\right] \\
V_4 = [R_{\rm L}/(2R_{\rm L} + R_{\rm S} + R_{\rm ON})] \cdot ({\rm A} - \Delta A) \cdot \sin\left(\omega t - \frac{3\pi}{2} - \Delta\phi\right) \left[\frac{1}{2} + \frac{2}{\pi}\sum\limits_{n=1}^{\infty} \frac{1}{2n-1} \sin((2n-1)(\omega t))\right].
\end{cases} \tag{9}
$$

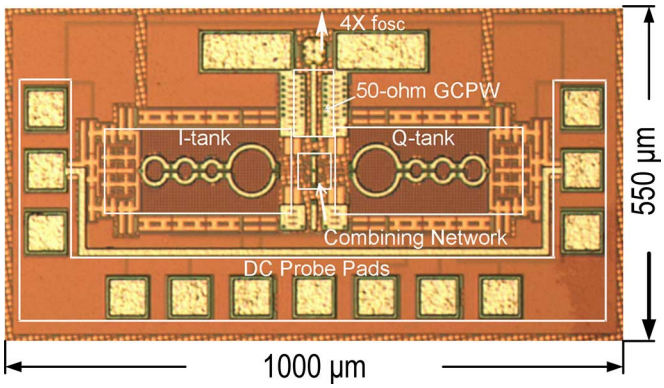

Fig. 15. Die photograph of the signal generation circuit.

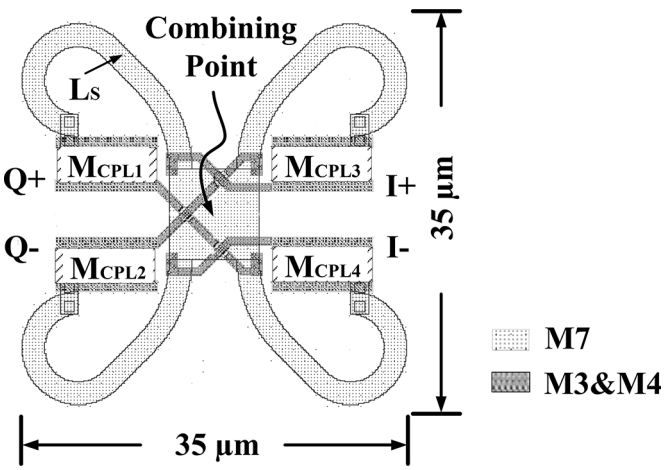

Fig. 16. Butterfly layout of the source inductors.

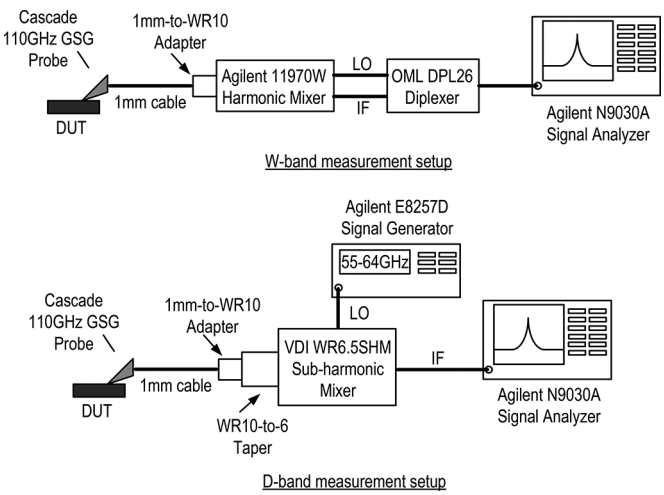

Fig. 17. Measurement setups for W-band and D-band.

bias" cases in which the bias current was increased to ∼30 mA to further extend the frequency tuning as well as to increase output power. Increasing the bias current however degrades phase noise because the oscillator enters the voltage limited region at the bias of ∼20 mA. The power consumption varied between 30 and 45 mW from a 1.5 V power supply. The simulated voltages across any two terminals of transistors are less

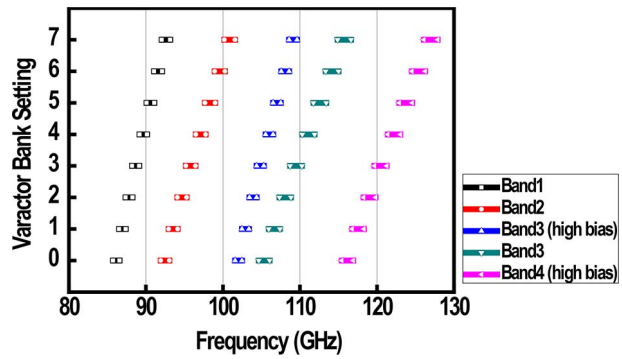

Fig. 18. Measured frequency tuning range.

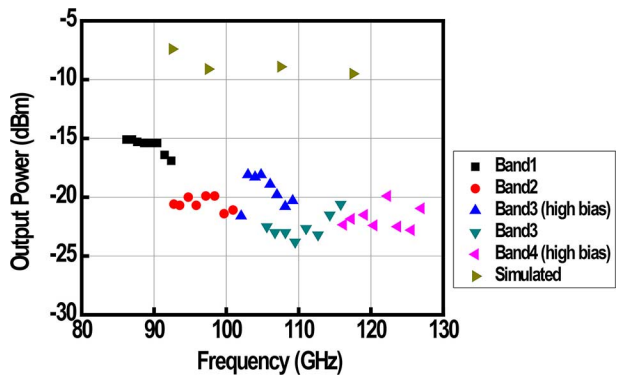

Fig. 19. Measured and simulated output power across all frequencies.

than 1.2 V. The measured signal frequency can be tuned from 85 to 127 GHz without any gaps unlike for the 57.5–90.1 GHz oscillator [10]. The corresponding tuning range is 39%, which is ∼4x higher than that for the previously reported widest tuning CMOS signal generation circuit with output frequencies over 90 GHz [15].

Fig. 19 shows the measured signal output power of the circuit after de-embedding the losses of the measurement setup, as well as the simulated output power. The measured signal power ranges between −15 and −23 dBm over the output frequency range. The simulated output power across all frequency bands is −7 to −9.5 dBm. Compared to the measured output power, the difference is over 10 dB. This discrepancy between the simulation and measurement could be due to the inaccuracy of non-linear transistor model that is critical for determining the harmonic generation. Specifically, the high-order nonlinearities of transconductance, g_m, parasitic capacitances (e.g., gate-to-source capacitance C_{gs}, gate-to-drain capacitance C_{gd}, drain-to-body capacitance C_{db}), and the output conductance g_{ds} are unlikely to be characterized and properly modeled for the millimeter wave operation. The discrepancy is also partially due to the unexpected measured output impedance deviation from the simulation. The simulated output impedance is inductive while the measured is capacitive. This impedance deviation could result in ∼2 to 4 dB output power degradation as observed from simulations. Nevertheless, the lower-than-expected output power is still useful for rotational spectroscopy in which output power of a few μW's is needed.

TABLE II
COMPARISON WITH STATE-OF-THE-ART MILLIMETER WAVE CMOS SIGNAL GENERATION CIRCUITS

References	[12]	[13]	[14]	[15]	[16]	[10]	This Work
Technology	65nm CMOS	65nm CMOS	32nm SOI	65nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS
Supply Voltage (V)	0.8	1.5	1.2	1	1.2	1.2	1.5
Center Frequency (GHz)	100.9	94.6	102.2	118	289.5	73.8	106.7
Frequency Tuning Range (%)	11.2	5.8	4.1	7.8	4.5	44.2[f]	39.4
DC Power (mW)	3.5 to 11.9	9	7.6	5.6	325[a]	8.4 to 10.8	30 to 45[b]
PN@10-MHz offset[c] (dBc/Hz)	-104.5	-106	-100.8	-103.9	-98	-104.6/ -112.2	-101.6/ -108.2
FOM_T[d] (dBc/Hz)	-176.5	-171.2	-164.6	-175.7	-155.2	-184.2/ -192.2	-179.3/ -185.9
Output Power (dBm)	N/A	-4 to -8[e]	N/A	>-28.5	-1.2	-20 to -25	-15 to -23
PN@10-MHz offset at 85 to 90GHz (dBc/Hz)	--	--	--	--	--	-105 to -106	-107 to -108
Output Power at 85 to 90GHz (dBm)	--	--	--	--	--	less than -20	~-15
Chip Area (mm^2)	0.0025 (core)	0.24	0.0014 (core)	0.22	0.36	0.03 (core)	0.55

(a) 4 VCO's. (b) Q-VCO. (c) Phase noises are reported at center frequency. Estimated from 1-MHz offset if 10-MHz offset phase noise is not reported. (d) $FOM_T = PN - 20log\left(\frac{f_0}{\Delta f} \times \frac{FTR}{10}\right) + 10log\left(\frac{P_{DC}}{1mW}\right)$. (e) Output buffers are used. (f) It has frequency tuning gap.

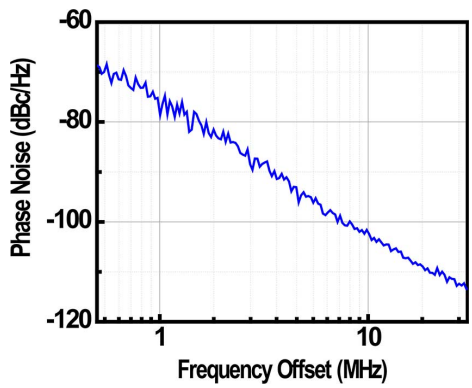

Fig. 20. Measured phase noise plot for a 126.9 GHz carrier (in Band 4).

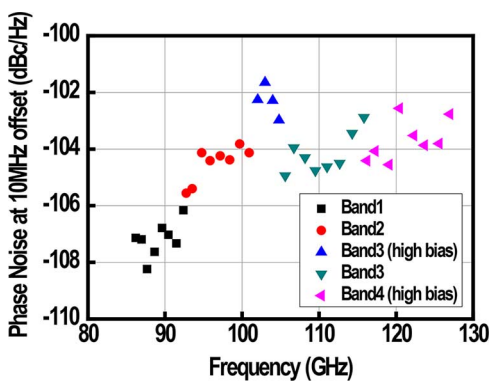

Fig. 21. Measured phase noise at 10 MHz offset across all frequencies.

The signal generation circuit was locked in a phase-locked loop with a bandwidth of ~500 kHz for the phase noise measurement [21]. Fig. 20 is an example of the measured phase noise plot. The phase noise at a 10 MHz offset from a 126.9 GHz carrier (in Band 4) is well above the instrument noise floor. Fig. 21 shows the measured phase noise at 10 MHz offset across all frequency bands. It varies from −108 to −102 dBc/Hz at 85 to 127 GHz, which is within the rotational spectroscopy design specification of −88 dBc/Hz@10 MHz offset for a 120 GHz carrier.

V. CONCLUSION

This work has shown that it is possible to realize a signal generation circuit that outputs signals from 85 to 127 GHz (~40% frequency tuning range) suitable for millimeter wave rotational spectroscopy in 65 nm CMOS. This is accomplished by using a new broadband harmonic combining technique and extending the use of NMOS switch based variable inductors into millimeter wave frequencies. Furthermore, this work has shown that passive quadrature coupling that bypasses the need for a broadband on-chip bias-T reduces power consumption, phase noise, and conversion loss for the 4th order harmonic generation by ~3 dB over the linear superposition [5]. Table II summaries and compares the performance of state-of-the-art CMOS millimeter wave signal generation circuits. The signal generation circuit reported in this paper has a frequency tuning range which is more than 4x higher compared to the previously reported CMOS signal generation circuit with center frequency over 90 GHz, and achieves FOM_T of −179 to −186 dBc/Hz which is at least 4 dB lower than that of the others [12]–[15]. In addition, this circuit exhibits ~2 dB lower phase noise and ~5 dB higher output power than [10] while having the same FOM_T at the same output frequencies (85 to 90 GHz) and power efficiency, and not having a frequency gap. Lastly,

this work paves the way for implementing a single CMOS transmitter for rotational spectroscopy at 180–300 GHz.

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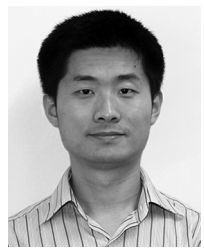

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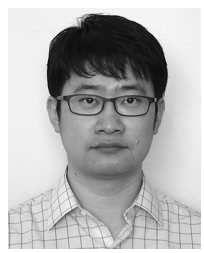

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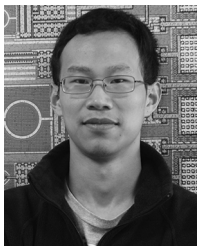

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