A New Five-Level Buck-Boost Active Rectifier

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***Abstract*—In this paper a new single-phase five-level buck-boost active rectifier is introduced called capacitor tied switches (CTS). The proposed rectifier has two independent DC outputs that can be connected to two different loads. Different switching states and the average mode of the proposed topology are analyzed to design the associated controller aims at regulating the two output DC voltages, generating five-level voltage at the input of the rectifier and finally draw unity power factor and sinusoidal current from AC grid. From AC grid view, the rectifier works in boost mode however the generated DC voltage can be split into two separate outputs which may be less than the AC peak voltage or even more leads to work in both buck and boost operation mode. Full simulation results are shown and analyzed to validate the effective operation and good dynamic performance of the proposed five-level buck-boost rectifier.**

Index Terms—multilevel converter, Packed U-Cell, active PFC rectifier, buck-boost rectifier, Capacitor Tied Switches (CTS).

I. INTRODUCTION

By developing power semiconductors, active rectifiers emerged into power market as improved power quality rectifiers that could draw low THD (Total Harmonic Distortion) and high power factor current from the AC source since regulating the output DC voltage with low ripples. Such converters that are also called PWM rectifiers or PFC (power factor correction) rectifiers can shape the input current into desirable sinusoidal waveform by turning ON and OFF the active switches at arbitrary intervals [1-3].

PFC boost rectifiers produce higher DC voltage at the output than the peak value of the AC source voltage [4, 5] while the PFC buck rectifiers can reduce the output DC voltage to the lower value than the AC maximum voltage [6]. PFC boost rectifiers are attractive converters for high power industries while the buck ones are appropriate candidates for battery chargers [7]. The existing buck converters have low ratio of output voltage to the AC input one and they need LC filters for both input AC and output DC sides. Likewise, the output DC voltage of PFC boost rectifiers should be higher than the input AC peak voltage sufficiently to eliminate the input current harmonics and draw a unity power factor current from the grid. As well, a high input filter inductor and output capacitor are necessary to get acceptable results [8, 9]. In addition to above-mentioned drawbacks of buck and boost rectifiers, both types of converters suffer from high switching frequency that can produce EMI (electromagnetic interference) problems [10]. On the other hand, some of these rectifiers have two-stage configuration in which the first stage includes a diode rectifier to provide DC voltage from the input AC source and the second stage is in charge of stepping up or down the input DC value as a DC-DC converter. The two-stage rectifiers have less active switches but working in higher frequency than the other single-stage PFC rectifiers results in higher power losses [11, 12]. Hybrid topologies of such rectifiers have been proposed as buck-boost rectifier which can generate higher or lower DC voltage at the output. Such topologies use too many bidirectional active switches and they still need to use the input LC filters [13-15]. Some multilevel rectifiers have been recently introduced with acceptable results including low switching frequency, low harmonic voltage/current and high power factor [16, 17]. These multilevel rectifiers have more than one DC output terminals that should be connected to identical loads in order to operate in buck mode which is the main drawback. As well, to work in boost mode, the DC output terminals of such multilevel rectifiers are connected to only one load and works as series DC sources [9, 18-27].

In this paper, a new multilevel rectifier has been introduced that can overcome most of the above-mentioned problems. The proposed topology (CTS) has been derived based on the Packed U-Cell (PUC) converter presented firstly by Al-Haddad et al [28, 29]. The new topology has two DC output terminals that can be connected to two separated loads and generates five-level voltage waveform at the rectifier input where it is connected to the grid through an inductive filter. It can work in both buck and boost modes with low switching frequency just by changing the DC voltage reference while there are no AC capacitive and DC inductive filters in its configuration. The main advantage of the proposed CTS rectifier is generating high ratio DC voltage in buck mode as well as producing the DC voltage amplitude equal to the AC source peak value. A PI controller has been designed and implemented on this converter to produce the required reference waveform which is sent to multicarrier PWM and generated pulses run the associated power switches. Some simulations have been performed to validate the high efficiency and good dynamic performance of the new PFC rectifier topology in operating in both buck and boost mode while drawing sinusoidal and unity power factor current from the AC grid.

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II. Proposed CTS Rectifier Configuration

The proposed rectifier topology shown in figure 1 has been derived from the PUC multilevel converter [28] by changing the two lower switches directions S_3 and S_6 and the second DC bus C_2 polarity. Due to rectifier application, it can be said that 6 switches are tied by two capacitors as output DC terminals. Unlike the PUC converter in which two unequal DC buses were used, in CTS rectifier the two DC voltages are set to be equal (E) and the input voltage of the rectifier (V_{ad}) would be a five-level type of waveform. The switching states associated to the introduced rectifier topology have been listed in table 1.

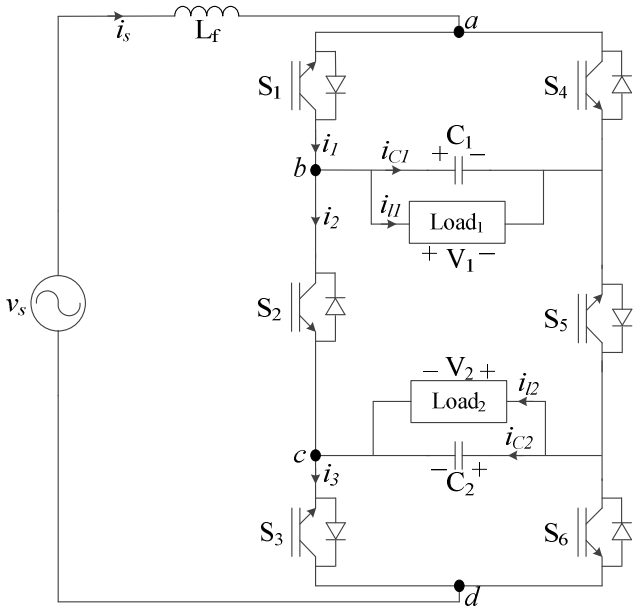

Figure 1: proposed five-level buck-boost PFC rectifier (CTS)

TABLE I
SWITCHING STATES OF CTS RECTIFIER

Switching State	i_s Sign	S_1	S_2	S_3	S_4	S_5	S_6	V_{ad}	V_{ad} voltage levels
1	$i_s > 0$	1	0	1	0	1	0	V1+V2	+2E
2	$i_s > 0$	1	0	0	0	1	1	V1	+E
3	$i_s > 0$	0	0	1	1	1	0	V2	+E
4	$i_s \geq 0$	1	1	1	0	0	0	0	0
5	$i_s < 0$	0	0	0	1	1	1	0	0
6	$i_s < 0$	1	1	0	0	0	1	-V2	–E
7	$i_s < 0$	0	1	1	1	0	0	-V1	–E
8	$i_s < 0$	0	1	0	1	0	1	-V1-V2	–2E

It is clear from the table 1 that each pair of switches S_1-S_4, S_2-S_5 and S_3-S_6 is working in complementary manner.

As far as $V_1 = V_2 = E$, there are two redundant switching states for voltage levels of +E and –E. Moreover, another redundancy is on the zero voltage level. Such redundant switching states help regulating the output DC voltages by choosing proper switching pattern. By controlling the output DC voltages, V_{ad} would have five levels with the maximum value of +2E. The principal concept of proposing this topology as a buck-boost rectifier relies on this maximum value of V_{ad} which should be more than the AC source peak value (v_{smax}). The following relations can be written:

$$V_{ad} > v_s \rightarrow 2E > v_{s\ \max} \rightarrow E > \frac{v_{s\ \max}}{2} \quad (1)$$

For instance, if RMS voltage of the AC source is 120V, then the maximum value would be 170V and the following relations would be obtained:

$$E > \frac{v_{s\ \max}}{2} \rightarrow E > 85V \quad (2)$$

Based on above equation, each DC terminal can be more than 85 volt in order to make the rectifier works in boost mode and suppress the input current harmonics. Noticing the output DC voltage amplitude which is 85 V in a 120V RMS grid, it is obvious that the converter is working as buck mode. Therefore, it can be concluded that however generating output DC voltages from 85 V to 170 V each, ensure that the converter is in buck mode, but while maximum value of V_{ad} is 2E then the grid will see a boost converter. From the grid point of view, this boost converter only uses a line inductor as a current filter to make the input current in-phase with the AC voltage while from the loads point of view; this converter is a buck type rectifier generating DC voltages lower than the AC peak voltage. Thus, the buck mode of operation is achieved without using large filters in both AC and DC sides of the rectifier. It can be said that the DC voltage is divided into two separate output terminals to deceive the AC grid seeing a boost voltage while in fact the DC output voltages are less than the input AC voltage.

Simply, the same concept is used in boost mode of operation however, each amplitude of the DC output voltages are more than the AC source amplitude. In this mode, not only the DC voltages are higher than the input AC voltage, but also the V_{ad} maximum value is higher than the peak value of the AC source voltage.

Eventually, it can be concluded that for a 170 V maximum AC grid, the CTS converter can generate dual output DC voltage varying from 85 V to 170 V while operating in buck mode; similarly the output voltage can vary from 170 V as equal to AC peak source amplitude and a much higher value when operating in boost mode. However, in all cases, the AC grid will see a boost type of multilevel rectifier with more than 170 V maximum at its dc bus output voltage. These characteristics lead to the design of a high density buck type of rectifier with low EMI at the ac side, while having the advantages of multilevel converter waveforms.

III. Modelling and Controller Design

In continue the detailed model of the proposed CTS rectifier is derived based on figure 1. The switching functions are defined as:

$$S_i = \begin{cases} 0 & if\ S_i\ is\ Off \\ 1 & if\ S_i\ is\ On \end{cases} \quad i = 1,\ 2,\ 3 \tag{3}$$

The rectifier voltage can be formulated as:

$$V_{ad} = V_{ab} + V_{bc} + V_{cd} \tag{4}$$

Where the points a, b, c and d are demonstrated in figure 1 and each voltage can be computed based on the switching function:

$$\begin{aligned} V_{ab} &= (S_1 - 1)V_1 \\ V_{bc} &= (1 - S_2)(V_1 + V_2) \\ V_{cd} &= (S_3 - 1)V_2 \end{aligned} \tag{5}$$

By substituting equation (5) into (4), therefore:

$$\begin{aligned} V_{ad} &= (S_1 - 1)V_1 + (1 - S_2)(V_1 + V_2) + (S_3 - 1)V_2 \\ &= (S_1 - S_2)V_1 + (S_3 - S_2)V_2 \end{aligned} \tag{6}$$

Using equation (6), the following model can be achieved for AC current (i_s).

$$L_f \frac{di_s}{dt} = v_s - V_{ad} \tag{7}$$

$$\frac{di_s}{dt} = \frac{1}{L_f}\left[v_s + V_1(S_2 - S_1) + V_2(S_2 - S_3) \right] \tag{8}$$

Since one of switches in each pair of S_1&S_4, S_2&S_5 and S_3&S_6 are turned ON, the switches current can be shown as a function of load current and switching function

$$\begin{cases} i_1 = S_1 i_s \\ i_2 = S_2 i_s \\ i_3 = S_3 i_s \end{cases} \tag{9}$$

Where,

$$i_1 = i_2 + i_{C1} + i_{l1} \tag{10}$$

$$i_{C1} = (S_1 - S_2)i_s - i_{l1} \tag{11}$$

$$\frac{dV_1}{dt} = \frac{(S_1 - S_2)i_s}{C_1} - \frac{V_1}{C_1 Z_1} \tag{12}$$

That Z_1 is the impedance value of the $Load_1$. Similarly, the second DC bus voltage can be modeled as the following by assuming that Z_2 is the $Load_2$ impedance. Loads are assumed as pure resistive in modelling.

$$i_3 = i_2 + i_{C2} + i_{l2} \tag{13}$$

$$i_{C2} = (S_3 - S_2)i_s - i_{l2} \tag{14}$$

$$\frac{dV_2}{dt} = \frac{(S_3 - S_2)i_s}{C_2} - \frac{V_2}{C_2 Z_2} \tag{15}$$

Equations (8), (12) and (15) give the average model of the proposed converter. Based on these equations, a simple PI controller has been designed to regulate the capacitors voltages (V_1 & V_2) as well as synchronizing the grid current (i_s) to provide a unity power factor five-level rectifier with low harmonic current. Figure 2 shows the implemented controller schematic.

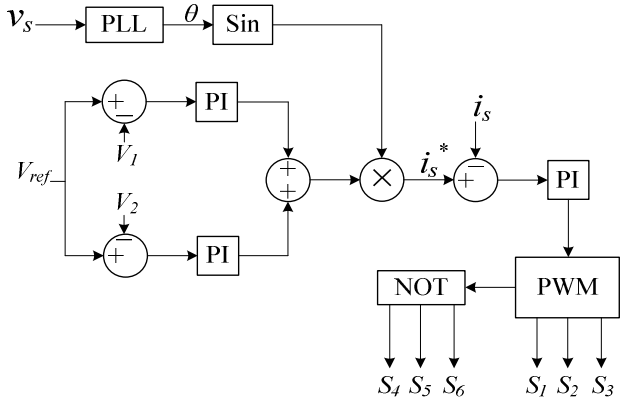

Figure 2: proposed rectifier controller

Regarding figure 2, a phase locked loop (PLL) block is used to synchronize the voltage and current of the grid. i_s^* is the reference current which should be drawn by the rectifier in order to ensure the power factor correction. A multicarrier PWM has been used to generate required pulses which are sent to the associate switches.

IV. Simulation Results and Discussion

In this section the proposed CTS buck-boost rectifier has been simulated in Matlab/SPS environment to validate the dual mode operation (buck and boost), multilevel voltage waveform generation and power factor correction. The sampling time has been fixed at 20us and the solver type was FixedStepDiscrete. Full system parameters are given in table 2.

TABLE II
SIMULATED SYSTEM PARAMETERS

AC Grid Voltage	120 V RMS
AC Grid Frequency	60 Hz
Line Inductor (L_f)	2.5 mH
DC voltages (V_1&V_2)	100 V (Buck Mode) 200 V (Boost Mode)
DC Capacitors (C_1&C_2)	1500 µF
DC Load 1	40Ω, 20mH
DC Load 2	30Ω, 30mH
Switching Frequency	5 KHz

In first test, the DC voltages are changed from 100 V to 200 V to show the transition of converter operation from buck to

boost mode. Figure 3 shows the results when the rectifier is operating in buck mode with 100 V DC on each load and at the time 7.44s the reference DC voltage is increased to 200 V. therefore the rectifier goes to boost mode quickly while the AC voltage and current waveforms (v_s and i_s) illustrated in figure 3-a have acceptable sinusoidal shapes. Moreover, as it is obvious in figure 3-b, the angle between source voltage and current is almost zero in both buck and boost mode of operation and the power factor is near 100% all the time. As far as the DC load voltages track the change as shown in figures 3-d and 3-e, the rectifier input voltage V_{ad} is generated as a five-level waveform consequently which is depicted in figure 3-c. As well, it is clear that the modulation index is higher when the output voltage is 100 V as buck mode than the boost mode of the rectifier. It should be noted that even in buck mode the rectifier voltage includes five levels and there is no need to DC side large filters. All in all, this test proves the ability of proposed CTS rectifier to work in buck and boost mode while drawing low harmonic and unity power factor current from the grid without need of using bulky filters.

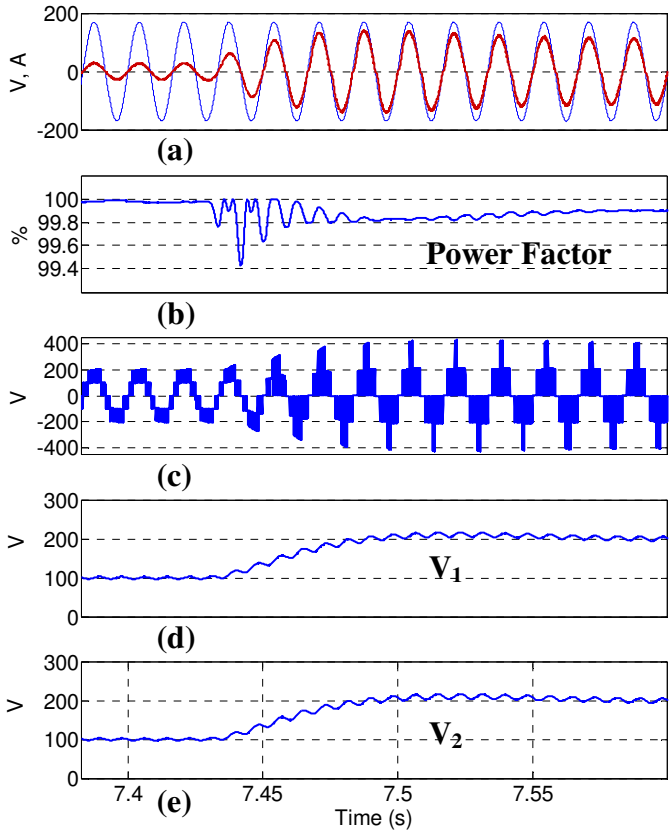

Figure 3: simulation results during change in DC voltages from 100 V to 200 V (transition between buck and boost modes). a) v_s and i_s *current waveform multiplied by 4 b) power factor c) input voltage of the CTS rectifier V_{ad} d) V_1 e) V_2

FFT analysis of rectifier voltage (V_{ad}) and grid current (i_s) for both buck and boost modes have been illustrated in figure 4 and 5 in a zoomed window, respectively. Such information can validate the low harmonic content of generated waveforms by proposed converter. The 5 KHz switching frequency generates the highest amount of harmonic which is evident in the following figures.

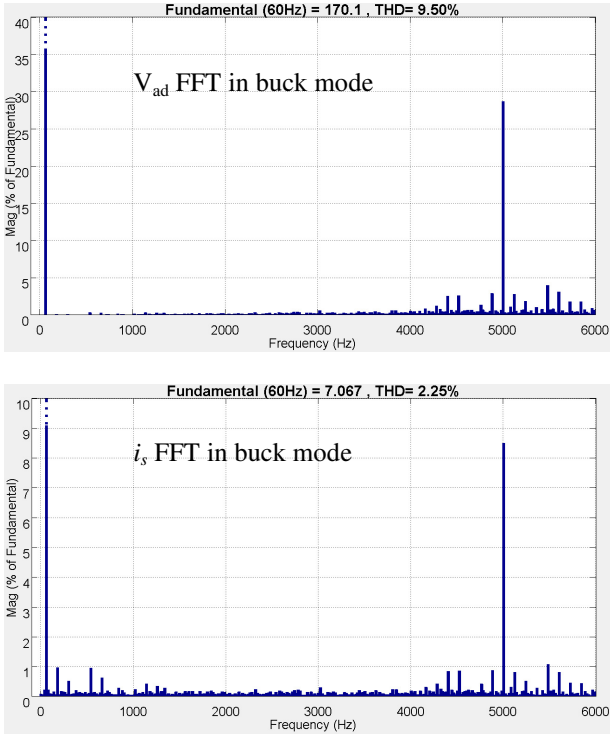

Figure 4: harmonic spectrum of V_{ad} and i_s in buck mode (100 V DC output)

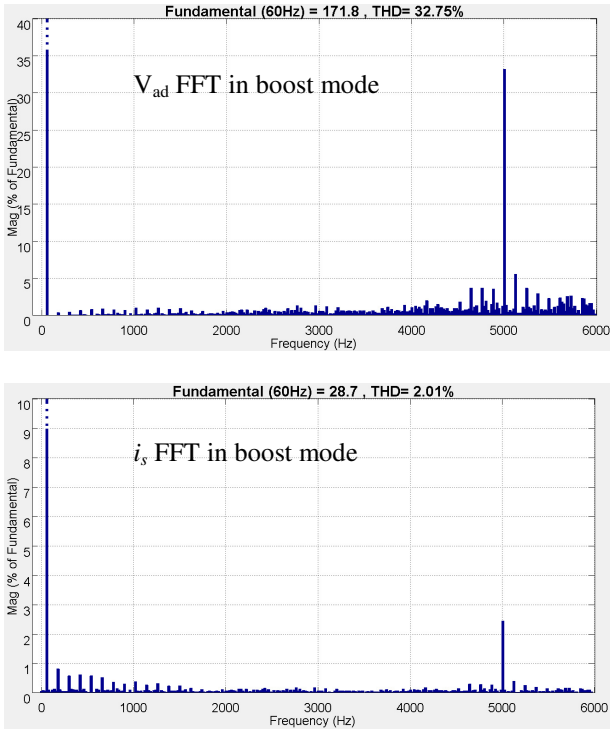

Figure 5: harmonic spectrum of V_{ad} and i_s in boost mode (200 V DC output)

In continue, two other tests have been performed to validate the good dynamic performance of the proposed rectifier and

the implemented controller in loads changes conditions. Therefore two different resistors have been added to the existing two RL loads in series, separately. At first, at the time 2.9s, a 10Ω resistor was added to the RL $Load_1$ and afterwards at the time 3.2s another 20Ω resistor has been added to the RL $load_2$. Consequently, the loads and grid side currents are raised step by step. Figure 6 and 7 show the simulation results in loads changes conditions for buck and boost mode of operation, respectively. Low DC voltage and current ripples are clear in these figures.

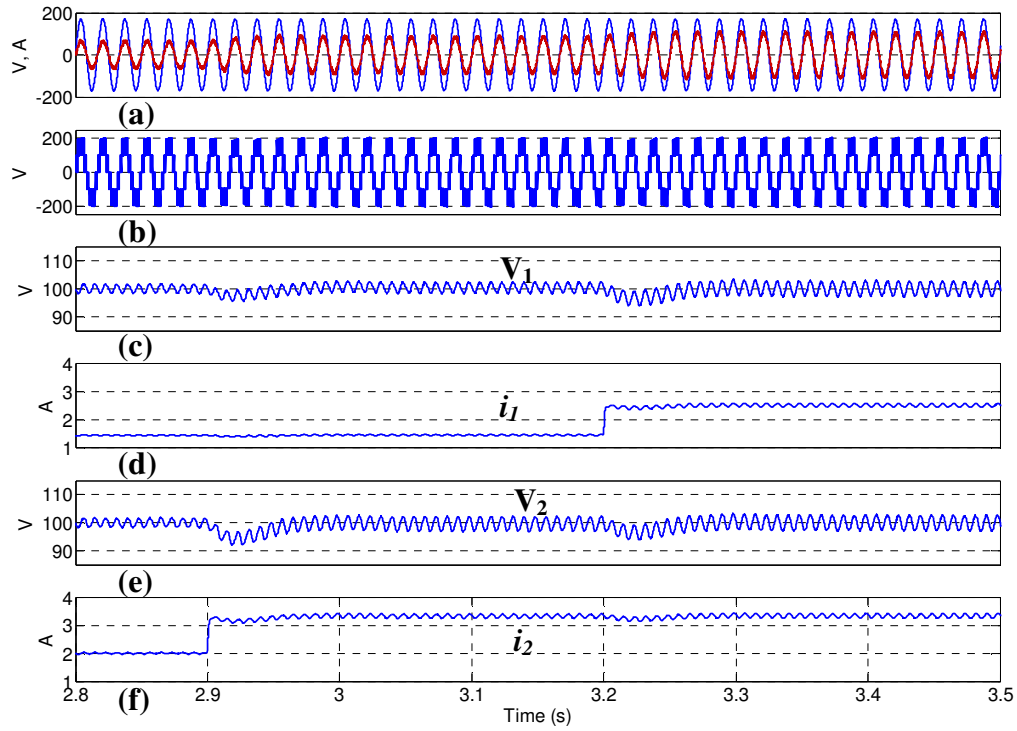

Figure 6: simulation results during load changes in buck mode. A) v_s and i_s *current waveform is multiplied by 15 b) input voltage of the CTS rectifier V_{ad} c) V_1 d) i_1 e) V_2 f) i_2

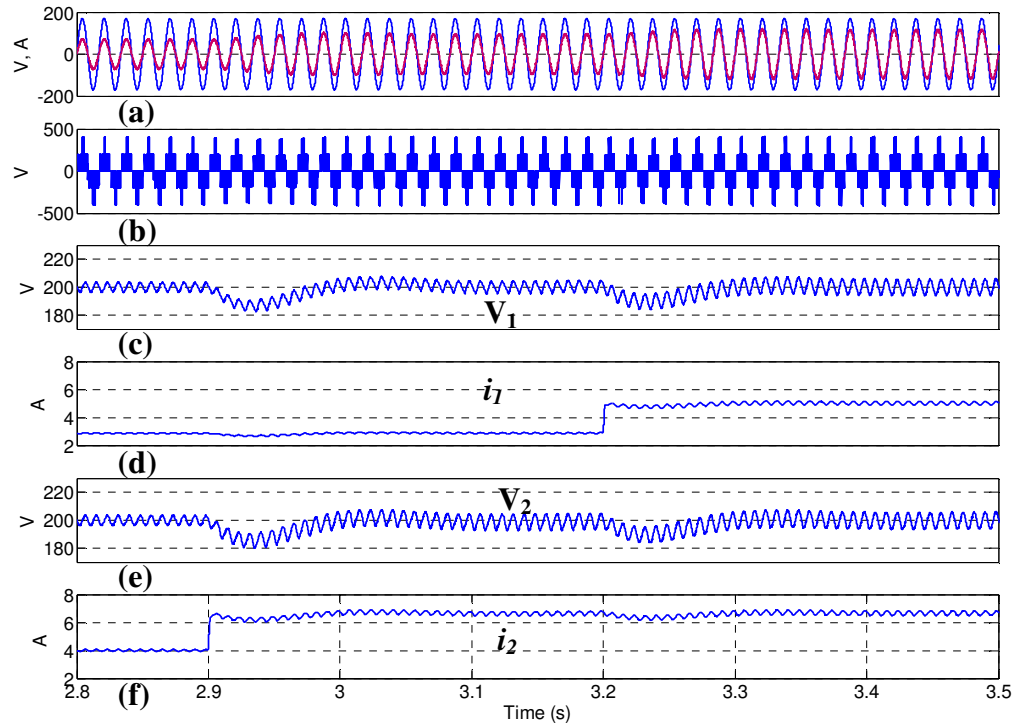

Figure 7: simulation results during the loads changes in boost mode. A) v_s and i_s *current waveform is multiplied by 15 b) input voltage of the CTS rectifier V_{ad} c) V_1 d) i_1 e) V_2 f) i_2

Moreover, regarding figures 6 and 7, it is obvious that fast response of the designed controller makes it possible to track any changes in the system including change in reference DC voltage, transition between bucks and boost modes as well as any kind of load variations.

V. CONCLUSION

In this paper a new topology of buck-boost active rectifier has been introduced based on slight modification of the third U-cell of the PUC original design. The proposed rectifier called CTS includes six switches tied by two capacitors as two output independent DC terminals and generates five-level voltage waveform at the input. The latter draw low harmonic current in-phase with the grid voltage making the operation at unity power factor rectifier easy in both buck and boost mode. This topology does not need additional bulky filters while switching at low frequency which constitute a big advantage of the presented CTS rectifier. Simulation results including regulated DC voltages, high power factor, and low supply THD current mainly obtained by the five-level rectifier input voltage. Moreover, good dynamic performance, fast response and reliable operation of the implemented controller and CTS converter topology were proven and discussed in details.

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