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Single phase transformerless inverter topology with reduced leakage current for grid connected photovoltaic system

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ABSTRACT

Leakage current is the main concern of the grid connected transformerless photovoltaic (PV) inverters. Many single phase transformerless inverter topologies with reduced leakage current have been introduced in the past few years. These are mainly classified on the basis of leakage current reduction methods Galvanic isolation without- common mode voltage (CMV) clamping and with-CMV clamping. It has been shown that leakage current generation is highly dependent on CMV. CMV of the topologies without- CMV clamping oscillates and oscillation amplitude depends on switches' junction capacitances and parasitic parameters of the topology. In order to eliminate the leakage current completely, CMV must be constant throughout the inverter operation. Moreover, inverter should also be capable to inject definite amount of reactive power into the grid, as demanded by the international regulations. In this study, reduced leakage current CMV clamped topology is proposed which can eliminate leakage current and capable of injecting reactive power into the grid. Total harmonic distortions (THD) of injected grid current at various solar irradiance levels are also analyzed. In order to verify the theoretical explanations, the proposed topologies are simulated in Matlab/Simulink environment. Finally, the simulated results are validated experimentally.

1. Introduction

PV systems are mainly categorized as: stand-alone system and grid connected system. Stand-alone system supply power directly to load or electrical appliance. It is integrated with energy storage (battery) system. In contrast, grid connected PV system supply generated energy into the utility grid for direct transmission, distribution, and consumption. As energy storage system is not needed, grid connected PV system is more cost effective and maintenance free [1–5]. It account for more than 99% of the globally installed PV power [6].

Based on the galvanic isolation, grid connected PV inverter topologies are grouped into transformerless and with transformer. The main functions of transformer are to provide voltage amplification and galvanic isolation between PV modules and the grid [7]. Thus, it prevents flow of dc current and leakage current injection into the grid [8]. Transformer can be of low frequency (LF) or high frequency (HF), depending on PV modules configuration. LF transformers are heavy, bulky and expensive and these reduce the system efficiency because of power loss in windings [9–11]. Even though, significant reduction in size and weight can be achieved by using HF transformer. The efficiency of the entire system is still low due to multiple converter stages (dc-dc and dc-ac) [12]. Hence, transformerless inverter topologies are introduced for PV application to overcome these issues. It can improve the system efficiency by 1–2% [13]. Furthermore, they are lighter, smaller and lower in cost.

Although the transformerless PV inverter has many advantages, high leakage current is the main concern. Because of the absence of transformer, a galvanic connection is formed which provide path for leakage current to flow from PV module to the grid [10,14]. At the same time, parasitic capacitor, which is formed between PV cells and metallic frame of module, generates high leakage current if high frequency potential is applied across it. The leakage current increases the total harmonic distortion (THD) of the grid current, electromagnetic interference (EMI) and system losses, and it causes personal safety problems [10,11,14–17].

There are mainly three modulation techniques: unipolar, bipolar and hybrid modulation, which can be used for single phase full bride (H4) transformerless PV inverter. CMV, leakage current and efficiency characteristics change according to the modulation schemes. In case of unipolar modulation and hybrid modulation three- level voltage ($0 \rightarrow +V_{PV} \rightarrow 0 \rightarrow -V_{PV} \rightarrow 0$) is generated across filter, yielding lower core loses [18]. However, they generate high

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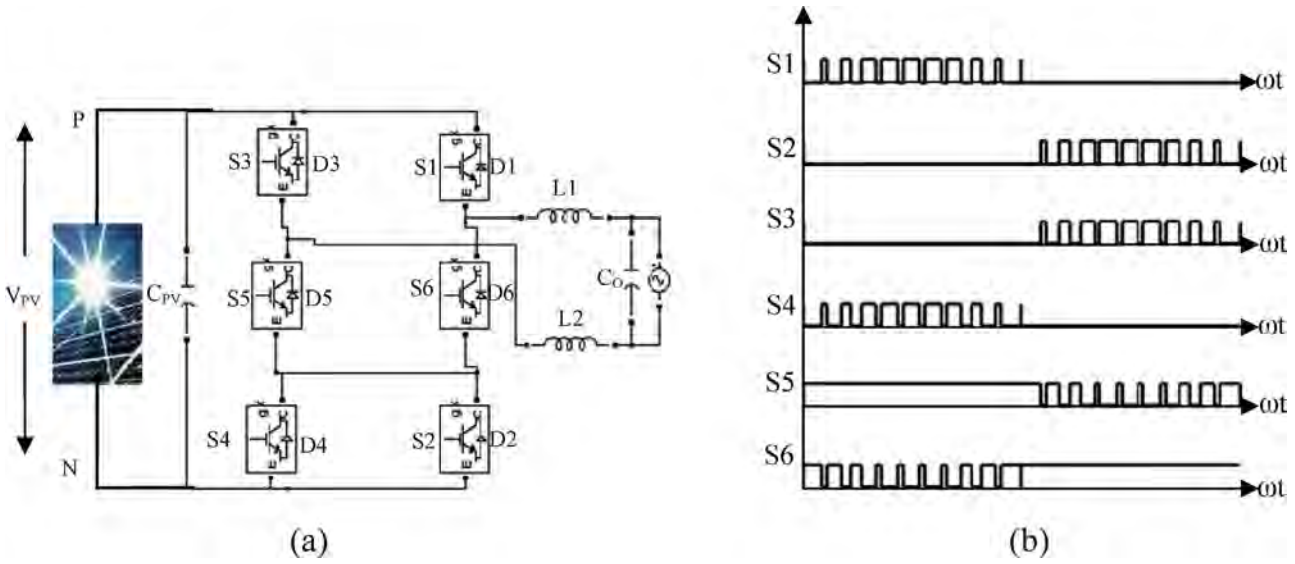


Fig. 1. The existing H6- topology and switching waveforms.

leakage current because of high frequency CMV. In case of bipolar modulation two-level voltage ($+V_{PV}$, $-V_{PV}$) is generated, yielding higher core losses. Moreover, it generate constant CMV, hence leakage current is low.

Leakage current problems can be solved by using bipolar sinusoidal pulse width modulation (SPWM) technique. However, efficiency of bipolar SPWM inverter is lower compared to unipolar SPMW inverter because of higher core losses of filter inductors and switching losses [7]. Thus, many inverter topologies have been introduced, which have advantages of both unipolar and bipolar modulation techniques: high efficiency and low leakage current. These topologies are mainly classified on the basis of leakage current reduction methods: Galvanic isolation without- CMV clamping and with-CMV clamping. The detailed classification was presented in Ref. [18]. CMV of the topologies based on without-CMV clamping oscillates and oscillation amplitude depends on switches' junction capacitances and parasitic parameters of the topology [13,19]. It has been shown that leakage current generation is highly dependent on CMV, especially, high frequency components. In order to minimize the leakage current completely, CMV must be constant throughout the inverter operation (power transfer states and zero voltage states). Moreover, inverter should also be capable to inject definite amount of reactive power into the grid as demanded by the international regulations [20]. It is reported [21] that without CMV clamped topologies, such as HERIC, H5 and H6 families, do not comply with IEEE-1547 standard [22] and these inject more than 5% grid current THD at low solar irradiance levels. It is due to oscillation of CMV during zero voltage states. Hence, these topologies are equipped with extra common mode filter (CMF) which burdens on cost and power density of the inverters [13].

In this paper, reduced leakage current CMV clamped topology is proposed which can eliminate leakage current and is capable of injecting reactive power into the grid. The CMV of the proposed topology remains constant throughout inverter operations and it eliminates the requirement of extra CMF. Moreover, THD analysis of the proposed topology is carried out at various solar irradiance levels (100–1000 W/m2) and the results are found within specified limit.

This paper is organized as follows. Section 2 presents analysis on existing H6 transformerless inverter topology. Leakage current generation and switches' junction capacitances are discussed in Section 3. Proposed topologies are presented in Section 4. In Section 5, simulation analysis is carried out. Section 6 presents power loss and junction temperature calculation. Experimental results are presented in Section 7 and finally, Section 8 concludes the paper.

2. Analysis on existing H6 topologies

In Ref. [23], a H6 without CMV clamped topology, as shown in Fig. 1(a), was proposed to overcome the drawback of the MOSFET based H6 topologies presented in Refs. [24,25]. These MOSFET based topologies were not capable to handle the reactive power flow. The existing H6 topology composed of six active switches S1–S6 which was derived from H4 topology by inserting two additional switches S5 and S6. Control strategies of switches are illustrated in Fig. 1(b). Depending on grid voltage polarity, switches S1–S4 are commutated diagonally at switching frequency to generate unipolar inverter output voltage. During positive grid voltage, S1 and S4 are switched at high frequency; S2 and S4 are OFF, S5 is ON and S6 is switched complementary to S1 and S4. During negative grid voltage, S1 and S4 are switched at high frequency; S2 and S4 are OFF, S5 is ON and S6 is switched complementary to S1 and S4. The switches S5 and S6 and their anti-parallel body diodes D5 and D6 provide path for freewheeling current during zero voltage state.

In this without-CMV clamped topology, output terminals (A and B) are connected to positive V_{PV} and negative V_{PV} (N) during active modes of inverter. Hence, during conduction periods, CMV can be $V_{PV}/2$ (e.g. during positive grid voltage polarity, $V_{CMV} = (V_{AN} + V_{BN})/2 = (V_{PV} + 0)/2 = V_{PV}/2$). However, during zero voltage or freewheeling periods, PV modules are disconnected from the grid. Therefore, the inverter output terminals (A and B) are floating with respect to the dc link. Hence, CMV ($V_{CMV} = (V_{AN} + V_{BN})/2$) is oscillating during this period and can not be determined by switching state. The CMV amplitude oscillation depends on switches' junction capacitances and parasitic parameters of the topology. Common mode (CM) and differential mode (DM) voltages of existing H6 topology are given in Table 1.

3. Leakage current generation and switches junction capacitances

In practical applications, junction capacitance of switches' varies from several hundred picofarads to few nanofarads [13] which cannot be ignored. When inverter commutates from power transfer state to freewheeling state (galvanic isolation or decoupling state),

Table 1
CM and DM characteristics of H6 topology.

	H6 topology			
	During positive grid voltage		During negative grid voltage	
Operation mode	Active mode	Freewheeling mode	Active mode	Freewheeling mode
CMV	$V_{PV}/2$	$V_{PV}/2$(floating)	$V_{PV}/2$	$V_{PV}/2$(floating)
DMV	$+V_{PV}$	0	$-V_{PV}$	0

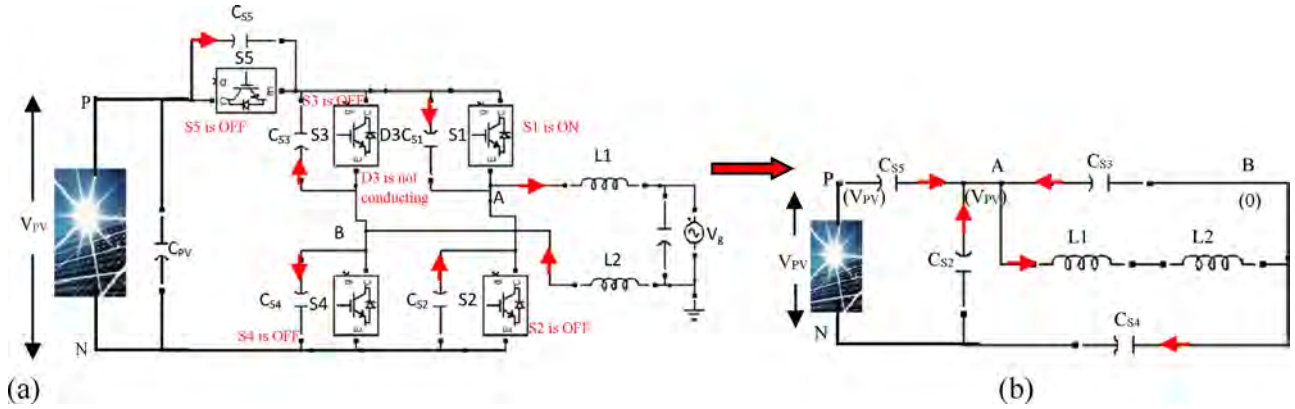


Fig. 2. Transient state model of H5 topology.

slopes of output voltages V_{AN} and V_{BN} depend on junction capacitance of switches'. As a result, CMV gets affected and contributes to leakage current generation because CMV is one of the main causes for leakage current. In order to investigate the leakage current generation due to junction capacitances, the H5 topology [26] is adopted. The grid and PV modules are directly connected through filter inductors during power transfer stage. Therefore, the effect of junction capacitance on CMV is insignificant. However, switches S5 and S4 are switched OFF simultaneously during transient state as shown in Fig. 2(a) and diode D3 does not conduct to go in freewheeling state. At this instant, the capacitors C_{S5} and C_{S2} are charged, and C_{S4} and C_{S3} are discharged. The equivalent simplified circuit of transient state is depicted in Fig. 2(b).

When diode D3 starts conducting during freewheeling state, the voltages V_{AN} and V_{BN} can be derived by using KCL,

$$V_{AN} = V_{BN} = \frac{C_{S2} + C_{S5}}{C_{S2} + C_{S5} + C_{S4}} \times V_{PV} \tag{1}$$

During freewheeling state, the CMV can be expressed by using equation,

$$V_{CMV} = \frac{V_{AN} + V_{BN}}{2} = \frac{C_{S2} + C_{S5}}{C_{S2} + C_{S5} + C_{S4}} \times V_{PV} \tag{2}$$

It is clear from Eq. (2) that CMV will remain constant and is equal to $V_{PV}/2$, only if $C_{S4} = C_{S2} + C_{S5}$. Unfortunately, it is not possible in practical applications. Hence, junction capacitors and output filter inductors form a resonant circuit to provide path for leakage current as shown in Fig. 3.

In order to completely eliminate the leakage current, galvanic isolation accompany with CMV clamping should be employed to keep CMV constant throughout inverter operation. Generally, the clamping branch consists of active switches (IGBTs) or passive switches (diodes) and a capacitor divider, which guarantee that CMV is fixed to half of the input DC link voltage during freewheeling periods. Hence, a modified H6 topology with active CMV clamping is proposed, which is discussed in Section 4.

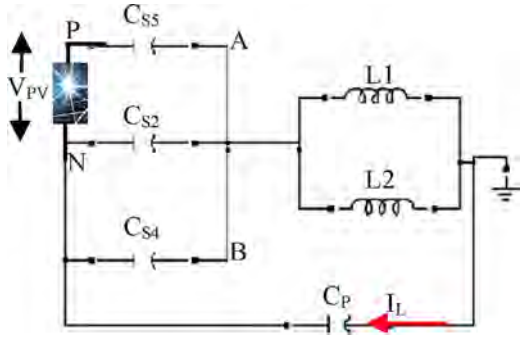


Fig. 3. Resonant circuit formed during freewheeling path.

4. Proposed topology and modulation strategy

Based on the above analysis, improved CMV clamped H6 topology is proposed for the grid connected PV system as shown in Fig. 4(a). The proposed topology is modified by adding an active switch (IGBT), S7 to the existing H6 topology. The voltage divider is made up of C_{PV1} and C_{PV2}. Switches S1–S4 are switches of H4 topology. The switches, S5 and S6, and anti-parallel diodes, D5 and D6, provide current path during freewheeling periods. Switching control pulses of the proposed topology are illustrated in Fig. 4(b). The Switches S1–S4 are switched at high frequency to generate unipolar inverter output voltage during power transfer state. While, the switch S7 is commutated at high frequency during freewheeling period to clamp the CMV and avoid floating of terminals A and B.

4.1. Operation modes of proposed topology

In order to generate the unipolar three-levels voltage, inverter operations are divided into four modes in a full grid voltage cycle (positive and negative grid voltages). These operation modes are described as follows:

Mode-I: During positive grid voltage

The switches S1 and S4 commutate at high frequency and S2 and S3 are OFF as shown in Fig. 4(b). Switch S5 is ON and S6 is switched

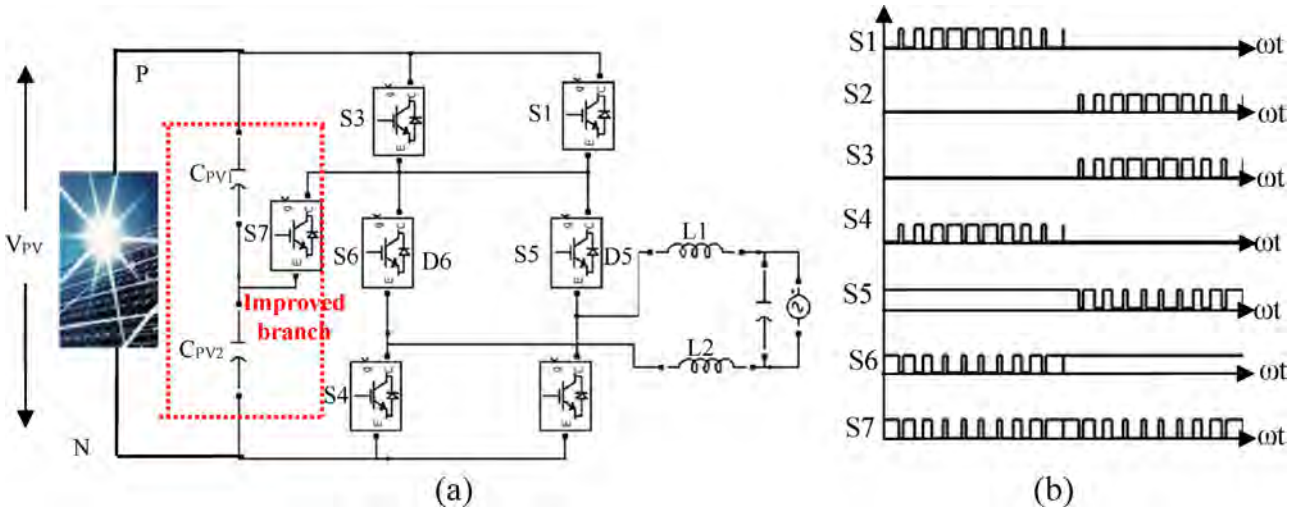


Fig. 4. Proposed H6 topology and switching waveforms.

Table 2
Operation and main features of proposed topologies.

	Proposed topology			
	During positive grid voltage		During negative grid voltage	
Operation mode	Active mode	Freewheeling mode	Active mode	Freewheeling mode
Switches state	S5 is ON; S1 and S4 are switched at f_s, S2 and S3 are OFF.	S5 and D6 are ON; S7 is switched at f_s.	S6 is ON; S3 and S2 are switched at f_s, S1 and S4 are OFF.	S6 and D5 are ON; S7 is switched at f_s
Current Path	S1, L1, Grid, L2, S5, S4	L1, Grid, L2, D5, S6	S3, L2, Grid, L1, S6, S2	L2, Grid, L1, S5, D6
CMV	$V_{PV}/2$	$V_{PV}/2$ (fixed)	$V_{PV}/2$	$V_{PV}/2$ (fixed)
DMV	$+V_{PV}$	0	$-V_{PV}$	0

complementary to S1 and S4. Active current flows through S1, L1, grid, L2 and S4. The voltage V_{AB} is V_{PV} and CMV becomes,

$$V_{CMV} = \frac{V_{AN} + V_{BN}}{2} = \frac{V_{PV} + 0}{2} = \frac{V_{PV}}{2} \quad (3)$$

Mode-II: Freewheeling period during positive grid voltage

The switches, S1 and S4 are OFF and S6 and S7 are ON. Freewheeling current flows through L1, grid, L2, anti-parallel diode D6 and S5. The terminal voltages V_{AN} and V_{BN} are clamped to $V_{PV}/2$ by the switch S7. Hence CMV becomes,

$$V_{CMV} = \frac{V_{AN} + V_{BN}}{2} = \left(\frac{V_{PV}}{2} + \frac{V_{PV}}{2}\right) \div 2 = \frac{V_{PV}}{2} \quad (4)$$

Mode-III: During negative grid voltage

The switches S2 and S3 commutate at high frequency and S1 and S4 are OFF as shown in Fig. 4(b). The switch S6 is ON and S5 is switched complementary to S2 and S3. Active current flows through S3, S6, L2, grid, L1 and S2. The voltage V_{AB} is V_{PV} and CMV becomes,

$$V_{CMV} = \frac{V_{AN} + V_{BN}}{2} = \frac{0 + V_{PV}}{2} = \frac{V_{PV}}{2} \quad (5)$$

Mode-IV: Freewheeling period, during negative grid voltage

The switches S2 and S3 are OFF whereas, S6 and S7 are ON. Freewheeling current flows through L2, grid, L1, anti-parallel diode D5 and S6. The terminal voltages V_{AN} and V_{BN} are clamped to $V_{PV}/2$ by the switch S7. Hence CMV becomes,

$$V_{CMV} = \frac{V_{AN} + V_{BN}}{2} = \left(\frac{V_{PV}}{2} + \frac{V_{PV}}{2}\right) \div 2 = \frac{V_{PV}}{2} \quad (6)$$

It is clear from Eqs. (3)–(6) that CMV is constant and equal to $V_{PV}/2$ in all the four operation modes. It is shown in simulation and experimental results that improved clamped branch fixes the CMV to $V_{PV}/2$ throughout inverter operation and is independent of switches' junction capacitors. The operation modes and main features of proposed topology are summarized in Table 2.

5. Simulation results

Performance analysis of existing H6 and the proposed topology are carried out on Matlab/Simulink. All simulations are based on the same parameters. The PV array consists of 12 series connected Sanyo HIP-225 HDE1 modules. P&O algorithm is implemented for maximum power tracking [27]. The stray parasitic capacitance (C_{PV}) is modeled with two capacitors of 100nF/kW connected to the PV terminals and the ground. The ground resistance (R_G) of 11 Ω is taken [11]. The output filter inductor is 3 mH each. The grid phase voltage is 230 V (RMS) with frequency (f) of 50 Hz. The switching frequency (f_s) is 10 kHz. The switches' junction capacitors of 10 pF are taken. In order to analyse the reactive power handling capability, 0.95 lagging power factor is applied. In order to demonstrate the effectiveness of the inverter model following transients condition have been applied. (i) Sudden change in Solar Irradiance (from 1000 W/m2 to 500 W/m2), (ii) transient from unity power factor to lagging power factor and (iii) transient from unity power factor to leading power factor (iv) sudden dip in grid voltage (230 V–180 V rms). Fig. 5 shows the inverter model is capable of handling transient regimes.

Figs. 6–9 show simulated waveforms of DM and CM characteristic of the existing H6 and the proposed H6 topologies at unity and 0.95 lagging power factor. It can be seen that these topologies are generating unipolar three-level inverter output voltage. This reduces output current ripple, inductor losses of filter and filter size as compared to bipolar modulation. However, CM characteristic voltages waveforms, V_{AN}, V_{BN} and CMV of existing H6 topology

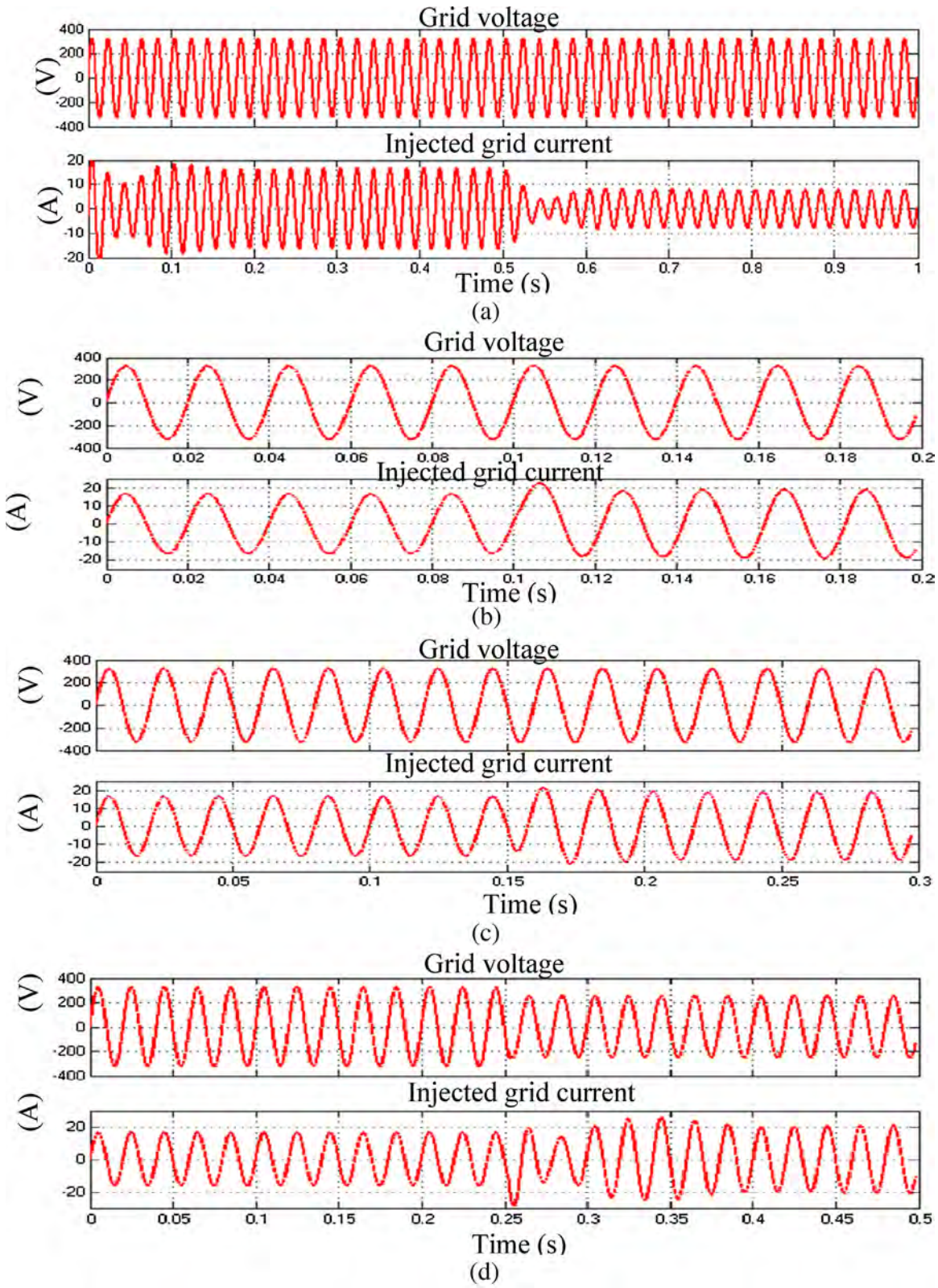


Fig. 5. Transients applied to modeled inverter (a)Sudden change in Solar Irradiance (from 1000 W/m2 to 500 W/m2), (b) transient from unity power factor to lagging power factor, (c) transient from unity power factor to leading power factor and (d) sudden dip in grid voltage (230 V–180 V rms).

as shown in Figs. 6 (b) and 8 (b), are oscillating. The amplitude of oscillation varies with switches' junction capacitances. Hence, leakage current is not completely eliminated. Moreover, Figs. 8 and 9 show reactive power carrying capability of the topologies. It can be observed that the grid current distortions have not been increased much with reactive power flow.

The above discussed problems of existing H6 transformerless inverter topology such as leakage current and oscillation of CMV due to switches' junction capacitors have been resolved by the use

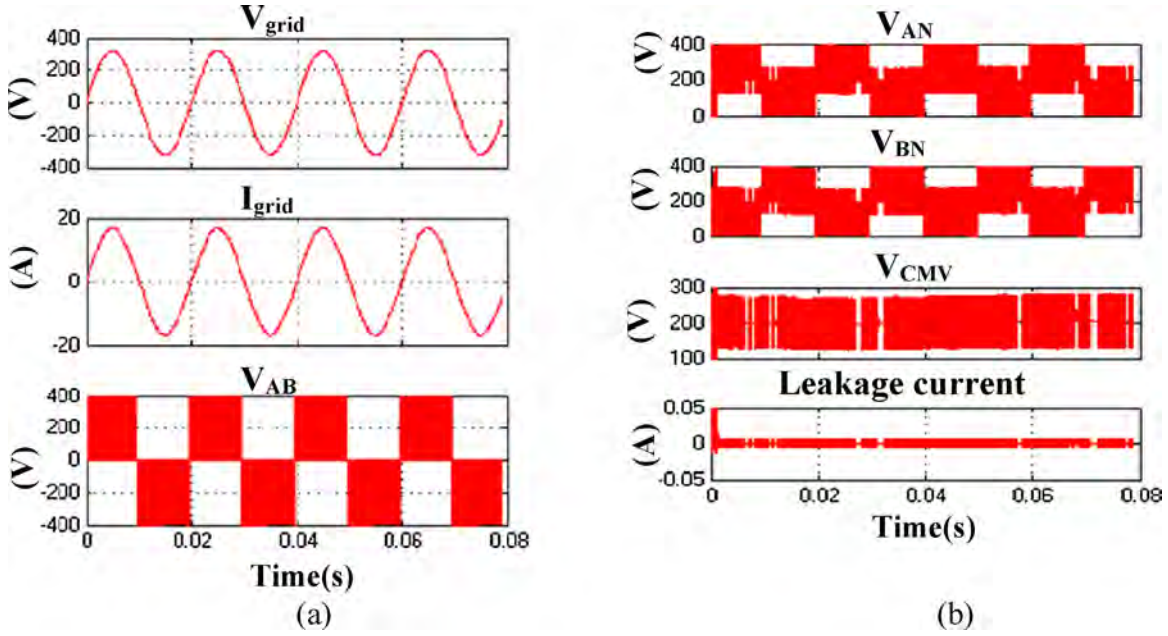


Fig. 6. The existing H6 topology (a) DM characteristics at UPF, (b) CM characteristics.

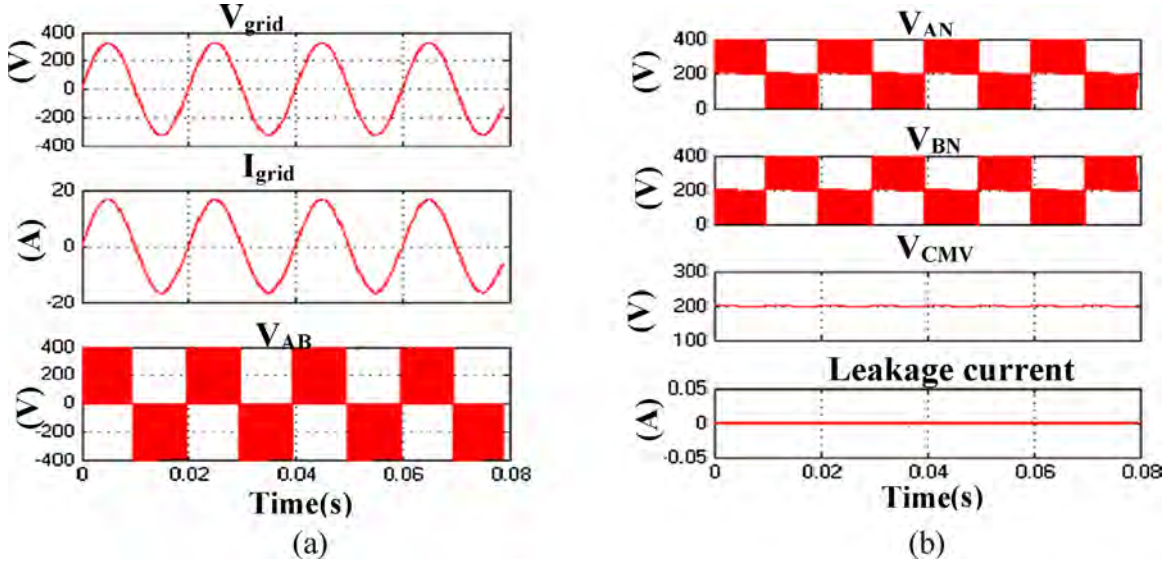


Fig. 7. Proposed H6 topology at UPF (a) DM characteristics, (b) CM characteristics.

of clamping branch in the proposed topology. CM characteristics voltages V_{AN} and V_{BN} of the proposed topology, as shown in Figs. 7 (b) and 9 (b), are exactly complementary to each other. Hence, CMV is completely clamped to 200 V throughout the inverter operation (conduction as well as freewheeling period). As a result, leakage current is totally eliminated. Moreover, the proposed topology has excellent reactive power handling capability without having distortion in grid current as depicted in Fig. 9(a).

6. Power losses and junction temperature calculation

Losses in semiconductor switch are evaluated on the basis of the device specifications given in datasheets and calculations [28–33]. The losses analysis is carried out by using PSIM thermal module [33]. Specifications of the IGBT and diodes used in the simulations are given in Table 3.

Table 3
Parameters for losses analysis [33,34].

Parameter/specification	Value
IGBT	FGA3060ADF, 600 V, 30 A (Fairchild Semiconductor)
Diode	ISL9R3060G2, 600 V, 30 A (Fairchild Semiconductor)
Frequency	50 Hz
Saturation voltage	1.8 V
Forward voltage	2.3 V
Junction temperature, $T_{j(max)}$	175 °C
Turn-ON switching loss @ 400 V	1430 μJ
Turn-OFF switching loss @ 400 V	310 μJ
P_{Cond_IGBT} calibration factor	1
P_{SW_IGBT} calibration factor	1
P_{Cond_Diode} calibration factor	1
P_{SW_Diode} calibration factor	1

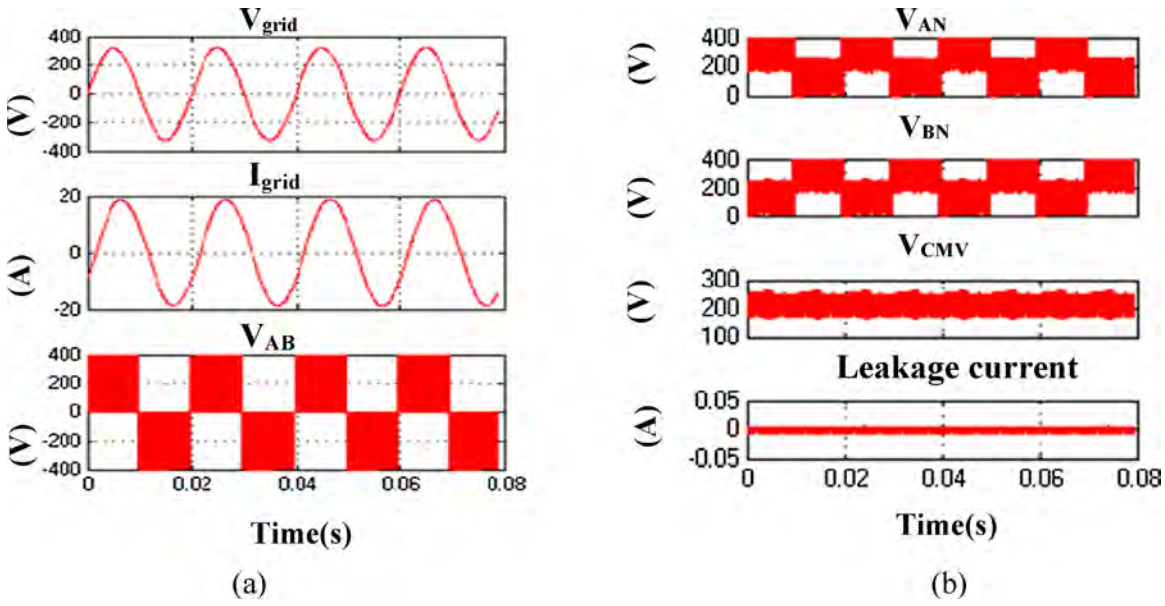


Fig. 8. The existing H6 topology with reactive power flow (a) DM characteristics, (b) CM characteristics.

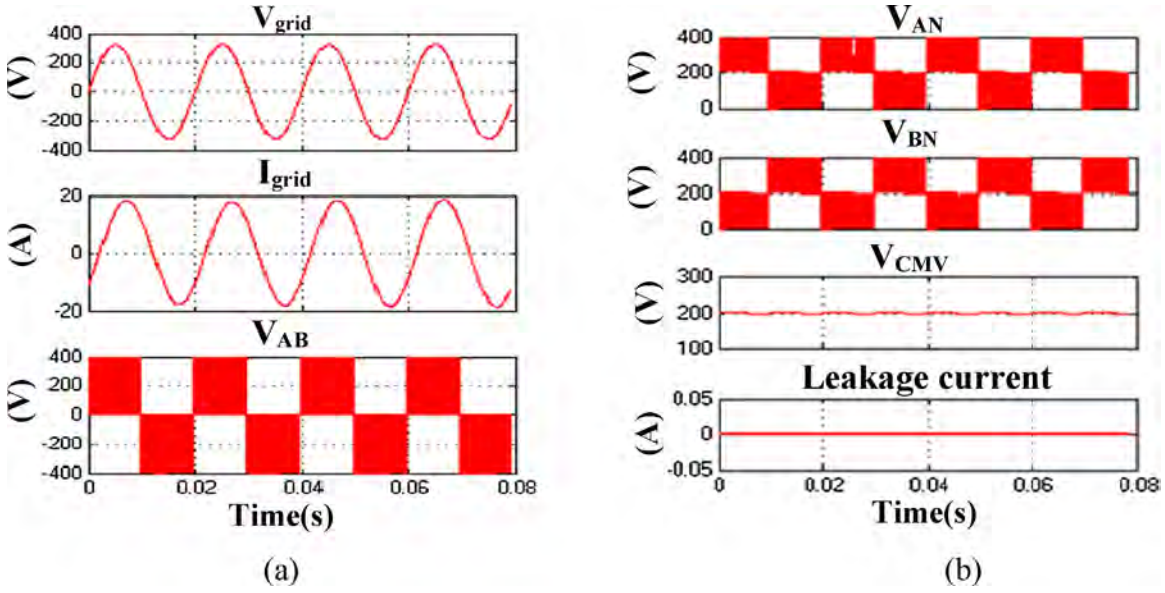


Fig. 9. Proposed H6 topology with reactive power flow (a) DM characteristics, (b) CM characteristics.

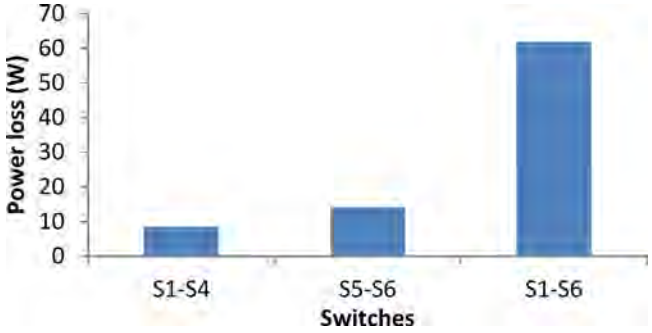


Fig. 10. The switches power loss.

The power loss calculation of IGBT and anti-parallel diode are described as follows.

6.1. IGBT loss calculations

The conduction losses (P_{Cond_IGBT}) of IGBT can be calculated by using the following equations,

$$P_{Cond\_IGBT} = V_{ce}(sat) \times I_c \tag{7}$$

where, $V_{ce}(sat)$ is IGBT saturation voltage and I_c is the collector current.

The IGBT turn-ON (P_{ON_IGBT}) and turn-OFF losses can be calculated by,

$$P_{ON\_IGBT} = E_{ON} \times f \times \frac{V_{CC}}{V_{CC\_datasheet}} \tag{8}$$

$$P_{OFF\_IGBT} = E_{OFF} \times f \times \frac{V_{CC}}{V_{CC\_datasheet}} \tag{9}$$

where, E_{ON} and E_{OFF} are the IGBT turn-ON and turn-OFF energy losses respectively; f is the frequency as defined in the input parameters; V_{CC} is the actual dc bus voltage, and $V_{CC\_datasheet}$ is the dc bus voltage in the E_{ON} and E_{OFF} characteristics of the datasheet.

The IGBT switching losses (P_{SW_IGBT}) can be calculated by equations,

$$P_{SW\_IGBT} = P_{ON\_IGBT} + P_{OFF\_IGBT} \tag{10}$$

$$P_{SW\_IGBT} = E_{ON} \times f \times \frac{V_{CC}}{V_{CC\_datasheet}} + E_{OFF} \times f \times \frac{V_{CC}}{V_{CC\_datasheet}} \tag{11}$$

6.2. Diode loss calculation

The diode conduction loss (P_{Cond_Diode}) is calculated using the following equations,

$$P_{Cond\_Diode} = V_F \times I_F \tag{12}$$

where, V_F is the diode forward voltage drop and I_F is the diode forward current. The diode turn-on losses are neglected. The diode turn-off losses (P_{OFF_Diode}) due to reverse recovery are given as:

$$P_{OFF\_Diode} = E_{rr} \times f \times \frac{V_R}{V_{R\_datasheet}} \tag{13}$$

Or

$$P_{OFF\_Diode} = \frac{1}{4} \times Q_{rr} \times V_R \times f \tag{14}$$

Or

$$P_{OFF\_Diode} = \frac{1}{8} \times T_{rr} \times I_{rr} \times V_R \times f \tag{15}$$

where, E_{rr} is the reverse recovery energy losses; Q_{rr} is the reverse recovery charge; V_R is the reverse blocking voltage; $V_{R\_datasheet}$ is the reverse blocking voltage in the E_{rr} characteristics of the datasheet; T_{rr} is the reverse recovery time; I_{rr} is the peak reverse recovery current; and f is the frequency as defined in the input parameters. Whenever E_{rr} is given, it will be used to calculate the losses. If E_{rr} is not given, Q_{rr} will be used. If both E_{rr} and Q_{rr} are not given, t_{rr} and I_{rr} will be used to calculate the diode turn-off losses. The diode switching losses (P_{SW_Diode}) can be given as,

$$P_{SW\_Diode} = P_{ON\_Diode} + P_{OFF\_Diode} \tag{16}$$

The total power losses of proposed H6 inverter and individual switches are shown in Fig. 10. It can be seen that the power losses of switches S1–S4 are same which less than the S5 and S6. The switches power loss increase the junction temperature. The junction temperature of switches should be less than the maximum junction temperature provided by the manufacturers. The junction temperature is function of the switches power loss and thermal resistance, which can be expressed as,

$$T_j = R_{th(s-a)} \times P + R_{th(c-s)} \times P + R_{th(j-c)} \times P + T_a \tag{17}$$

where, Tj, $R_{th(s\text{-}a)}$, $R_{th(c\text{-}s)}$, $R_{th(j\text{-}c)}$, P and T_a are the junction temperature, thermal impedance (ambient to heat sink), thermal impedance (heat sink to circuit element), thermal impedance (circuit element to heat sink), power loss and ambient temperature respectively.

The thermal impedance can be modeled as a Foster model reported in Refs. [35–37]. Details of the thermal modeling of power semiconductors can be found in Ref. [37].

7. Experimental Results

In order to validate the simulation results for the existing H6 and proposed H6 topologies experimentally, a universal inverter has been built using the same components. Inverter specifications are illustrated in Table 4. Control algorithms were implemented in OPAL-RT (OP-5600), a real time digital simulator. DC power supply (Chroma 62000 H-S) was utilized in place of PV system. The stray parasitic capacitances (C_{PV}) of PV modules are emulated with two capacitors of 300 nF connected to the positive and negative terminal of dc supply and the neutral of the load. The different waveforms were captured using digital oscilloscope.

Table 4
Inverter specifications [32].

Parameter/specification	Value
Rated power	3 kW
DC input voltage	400 V
Grid voltage	1-Ph–230 V (RMS), 50 Hz
Switching frequency	10 kHz
Dead time	2.5 μs
dc-link capacitors	2200 μF
IGBT	FGA3060ADF, 600 V, 30 A
Diode	ISL9R3060G2, 600 V, 30 A
Filter inductors	3 mH
Filter capacitor	6 nF
Stray capacitors	300 nF

Experimental DM and CM characteristics waveforms of the existing H6 and proposed H6 topologies are shown in Figs. 11–14. DM characteristics of these topologies, as shown in Figs. 11 (a)–14 (a), are similar to the simulation results. Inverter output voltages V_{AB} of both topologies are unipolar and the injected grid current is synchronized with the grid voltage. The RMS value of leakage current, as shown in Figs. 11 (c)–14 (c), for H6 and proposed H6 topologies are 22.3 mA, 8.3 mA and 23.7 mA, 9.1 mA at unity and lagging power factors respectively. The proposed CMV clamped topology is generating much lower leakage current compared to without CMV clamped H6 topology. This is because high frequency components of CMV are not completely clamped in case of without CMV clamped H6 topology. The voltages V_{AN} and V_{BN} of H6 are oscillating as shown in Figs. 11 (b) and 13 (b). Hence, CMV oscillates and oscillation amplitude depends on switches' junction capacitances. As a result, leakage current is high in H6 topology. Moreover, Fig. 13 shows reactive power carrying capability of H6 topology, it can be observed that grid current distortions have not been increased with reactive power flow, as shown in Fig. 13(a). Its reactive power carrying capability is good. In contrast, CM characteristics voltages V_{AN} and V_{BN} of proposed topology at unity and lagging power factor, as shown in Figs. 12 (b) and 14 (b), are exactly complementary to each other. Hence, CMV is constant throughout inverter operations. As a result leakage current is reduced to very low value which eliminates requirement of additional CM filter. Moreover, proposed topology has excellent reactive power handling capability without having distortion in grid current as depicted in Fig. 14(a). The effect of switches' junction capacitances on CMV characteristics voltages V_{AN}, V_{BN} and CMV of H6 and the proposed topologies are illustrated in Fig. 15(a) and (b) respectively. It can be observed that improved clamped branch fixes the CMV to 200 V throughout inverter operation and is independent of switches' junction capacitors.

The injected grid current THD of H6 and proposed H6 topologies are measured by FLUKE 43B power quality analyzer. Injected grid current THD for these topologies are 2.1%, 1.7% and 3.8%, 2.3% at unity and lagging power factors respectively. The grid Current THD are also measured at various solar irradiance levels (100–1000 W/m2) as illustrated with the grid injected current waveforms in Table 5a. It has been observed that the topology H6 is generating high THD at low solar irradiance levels. Topology H6 does not comply with international standard (THD < 5%) after 600 W/m2. The high value of THD may be due to oscillation of CMV due to switches' junction capacitors.

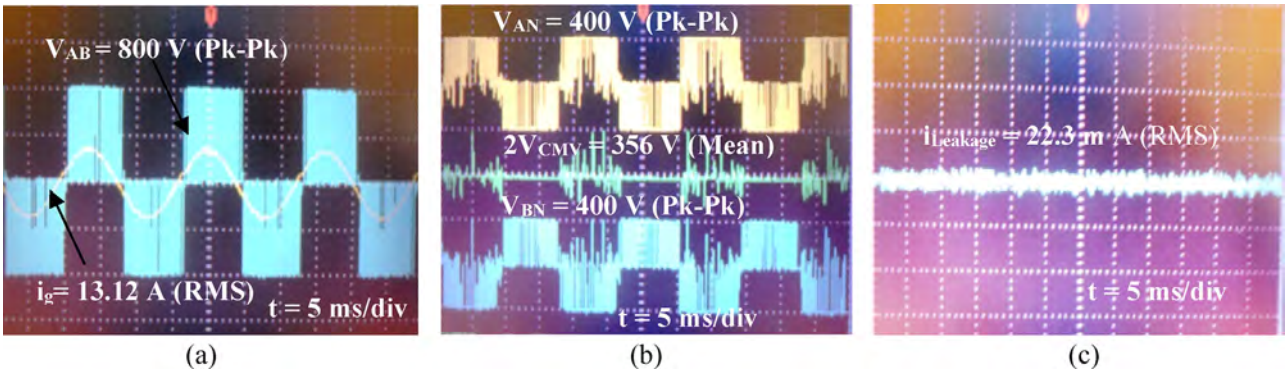


Fig. 11. H6 topology (a) inverter output voltage and load current at UPF, (b) V_{AN} (upper), CMV (middle), V_{BN} (lower) and (c) leakage current.

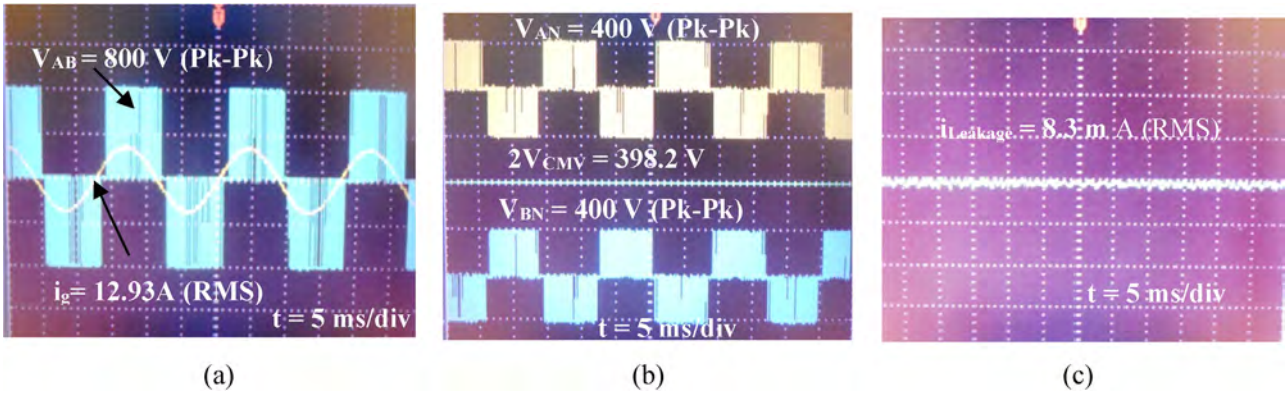


Fig. 12. Proposed H6 topology (a) inverter output voltage and load current at UPF, (b) V_{AN} (upper), CMV (middle), V_{BN} (lower) and (c) leakage current.

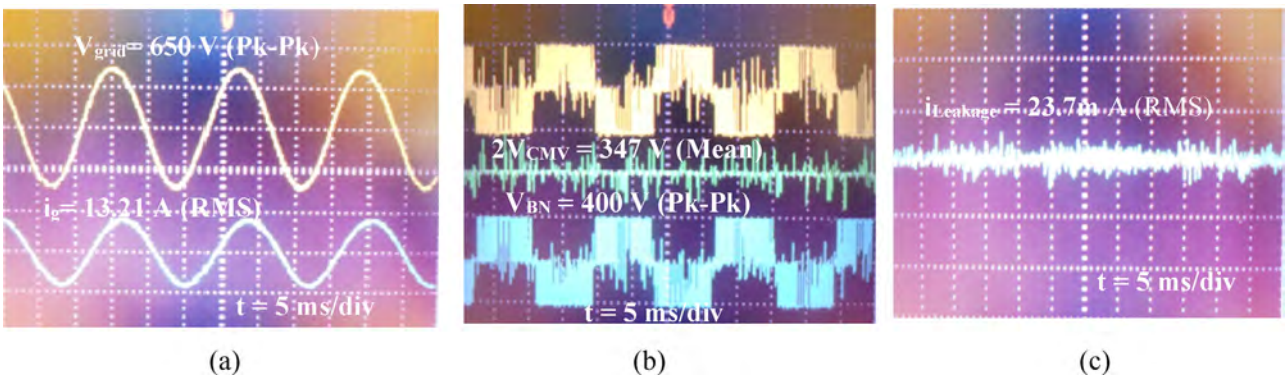


Fig. 13. H6 topology (a) inverter output voltage and load current wit reactive power flow, (b) V_{AN} (upper), CMV (middle), V_{BN} (lower) and (c) leakage current.

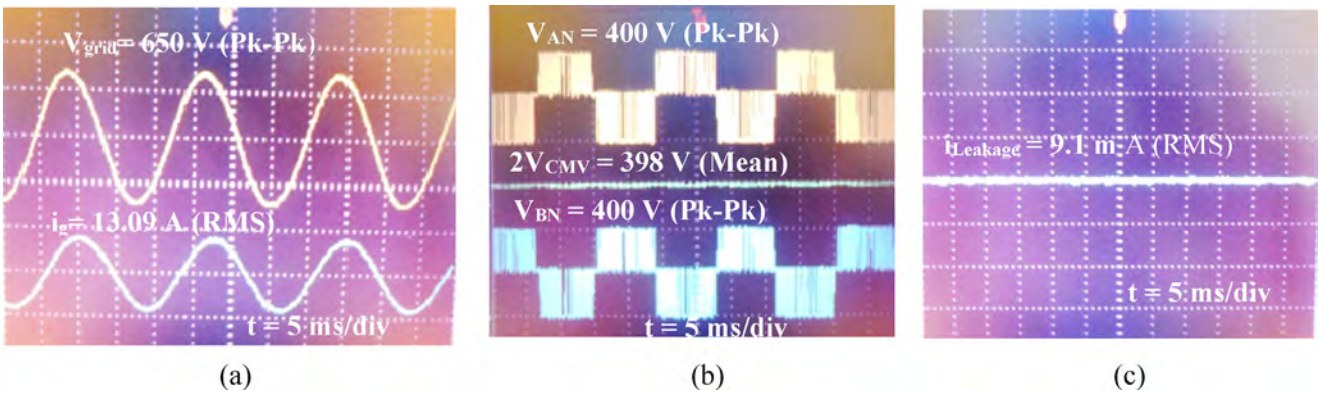


Fig. 14. Proposed H6 topology (a) inverter output voltage and load current with reactive power flow, (b) V_{AN} (upper), CMV (middle), V_{BN} (lower) and (c) leakage current.

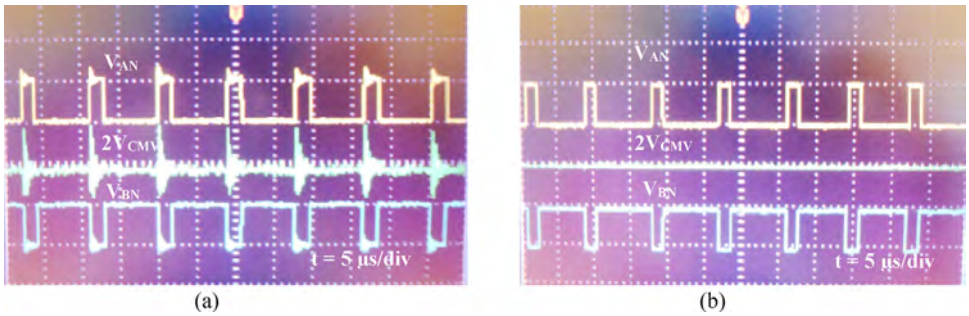
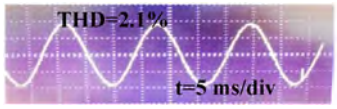
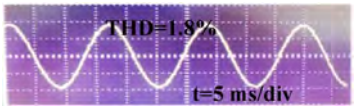
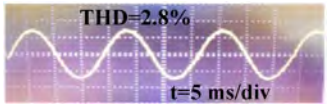
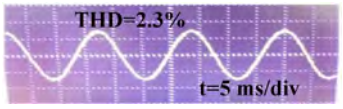
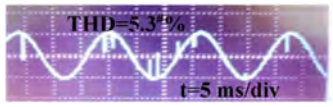
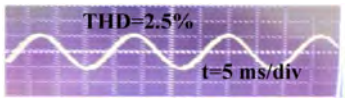
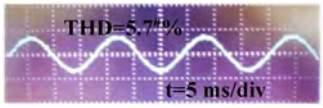
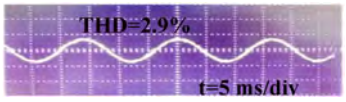
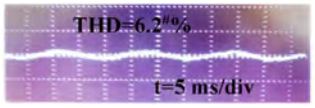
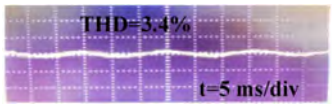


Fig. 15. CM characteristics of (a) H6 topology and (b) proposed H6.

Table 5a
Injected grid current THD with waveforms.

Solar irradiance (W/m2)	Total harmonic distortion (THD) in injected grid current	
	H6-I topology	Proposed H6-II
1000		
800		
600		
400		
100		

#Do not comply with IEEE 1547 Standard.

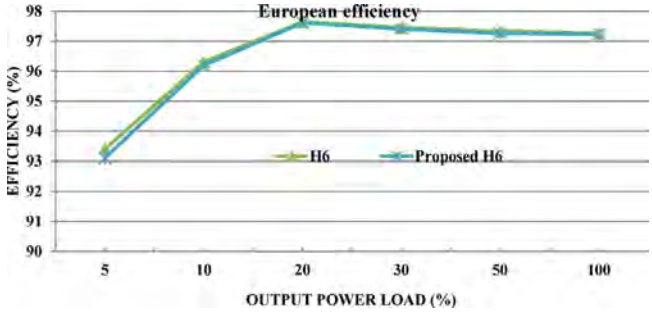


Fig. 16. Measured efficiency of H6 and the proposed topologies.

Measured efficiencies of the topologies for different percentage of output power load are shown in Fig. 16 for the European efficiency (η_{EU}). The efficiency can be calculated by using the equation,

$$\eta_{EU} = 0.03\eta_{5\%} + 0.06\eta_{10\%} + 0.13\eta_{20\%} + 0.10\eta_{30\%} + 0.48\eta_{50\%} + 0.2\eta_{100\%} \quad (18)$$

Table 5b
Performance comparisons of H6 and proposed H6 topologies.

Features	Existing H6	Proposed H6
PWM	Unipolar	Unipolar
CMV (mean 2 V_{CMV}) at UPF	356 V	398.2 V
CMV (mean 2 V_{CMV}) with reactive power flow	347 V	398 V
Leakage current (mA) at UPF	22.3 mA	8.3 mA
Leakage current (mA) with reactive power flow	23.7 mA	9.1 mA
THD (%)at UPF	2.1%	1.7%
THD (%) with reactive power flow	3.8%	2.3%
Efficiency (%)	97.12%	97.04%
Extra CM filter	Required	Not required

The calculated European efficiency (η_{EU}) for H6 and proposed H6 topologies are 97.12% and 97.04% respectively. Performance comparison of H6 and proposed H6 topologies are given in Table 5b.

8. Conclusion

In this paper, CMV clamped H6 transformerless inverter topology for grid connected PV system is presented. It has been shown that leakage current generation is highly dependent on common mode voltage (CMV), especially, high frequency components. In

existing H6 topology CMV oscillates and amplitude of oscillation is dependent on switches' junction capacitors. The effect of these capacitors on leakage current generation is significant during zero voltage states of inverter. Proposed topology has clamped the CMV to half of the dc link voltage during zero voltage states. As a result, leakage current is reduced to a very low value and is independent of junction capacitors. Performance analysis of the existing H6 and proposed topologies are carried out on Matlab/Simulink, and results are experimentally validated. The advantages of proposed topology are described as follows:

1. Improved clamping branch in the proposed topology has fixed CMV to half of the dc link voltage throughout inverter operations. As a result leakage current is almost reduced to zero.
2. THD of the proposed topology is within the specified limit and complies with the international regulation at various solar irradiance levels (100–1000 W/m2). This is because of fully unipolar modulation strategy and CMV clamping. The existing topology generates current THD more than 5% at low solar irradiance level, which will reduce significant power generation.
3. No extra CM filter is required to nullify the effect of junction capacitors switches. This can improve the power density and cost.

Hence, the derived active clamped H6 transformerless inverter topology is optimized candidate for high-performance grid connected PV system.

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