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Coplanar Full Adder in Quantum-Dot Cellular Automata via Clock-Zone Based Crossover

D. Abedi, G. Jaberipur, and M. Sangsefidi

***Abstract*— We use a coplanar QCA crossover architecture in the design of QCA full adders that leads to reduction of QCA cell count and area consumption without any latency penalty. This crossover uses non-adjacent clock zones for the two crossing wires. We further investigate the impact of these gains on carry flow QCA adders. These designs have been realized with QCADesigner, evaluated, and tested for correctness. For better performance comparison with previous relevant works, we use a QCA-specific cost function, as well as the conventional evaluation method. We show 23% cell count and 48% area improvements over the best previous QCA full adder design. Similar results for 4-, 8-, 16-, 32-, and 64-bit adders are 29% (22%), 24% (51%), 19% (54%), 13% (69%), and 9% (49%) cell count reduction (less area consumption), respectively.**

***Index Terms*—Quantum-dot cellular Automata, Full adder, carry flow adder.**

I. Introduction

As the nanometer scale CMOS devices are facing new realization challenges (e.g., increased leakage current leading to considerable static power dissipation) [1] new technologies are emerging as possible replacements for CMOS. Quantum-dot cellular automata (QCA) [2] represent one of such innovative platforms. The basic QCA cell, that is capable of representing a logical bit, occupies nano-scale area. A primitive QCA cell commonly contains two electrons, whose two possible coulomb repulsion [2] placements represent "1" and "0".

QCA realization of the full adder (FA), as the most commonly used digital arithmetic cell, has been the subject of considerably many research papers (e.g., [3][4][5][6][7]). To show the impact of such very fast and low power arithmetic cell, word wide QCA adders [3][5][6][8] and multipliers [6][9] have been designed. One problem with designing QCA composite cells and circuits is how to efficiently design the crossover wires to reduce costs (i.e., both QCA cell count and implementation complexity). Multi-layer solution bears high cost due to, for instance, fabrication issue [10]. Nor is favorable the Logical crossing [11], due to its high area overhead. However, to achieve coplanar crossover wiring, 45-degree rotated QCA cells have been proposed [4].

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This has its own problems, such as low robustness [12] and implementation cost overhead, due to coexistence of two types of QCA cells [10]. Nevertheless, another coplanar QCA crossover wires design takes advantage of time-division multiplexing that is supported by special 8-phase clocking scheme with three types of clocking signals [13]. This single type cell alternative is highly robust and easy to design. However, a recent technique [14], [15] that also uses single type cells, takes advantage of non-adjacent zones of a 4-phase clocking scheme to resolve the wire crossing in one layer.

In this paper, we utilize the latter crossover technique in designing our QCA full adder (QFA) and the corresponding carry flow [6] adders. We compare our performance figures with those of relevant previous works via conventional metrics (i.e., number of clocks, cell count and area) and the QCA-specific cost function of [16].

The rest of this presentation is organized as follows. Sections II, and III briefly cover a general introduction to QCA and the previous relevant works on QFA and QCA adders, respectively. Details of the used crossover, the proposed QFA design and the corresponding carry flow adders are offered in Section IV. In Section V, we compare the performance of QFAs and the corresponding n-bit adders with two different conventional and QCA-specific metrics. Finally we conclude in Section VI.

II. QCA in brief

The primitive cell in QCA technology, as depicted in Fig. 1(a), contains four electron place holders or quantum dots. Normally two electrons are injected into the cell, where they occupy two dots on the two ends of one of the diagonals of the containing square cell. Other placements (i.e., along the edges) are not possible since the two electrons tend to repulse one another. Therefore, two polarities are possible. The slash like polarity (/) represents binary 1 (see Fig. 1(b)), and the backslash (\) one represents binary 0 (see Fig. 1(c)). Placing two of such cells next to each other would form // (see right-top part of Fig. 2(a)) or \\ (see left-bottom part of Fig. 2(a)) compositions due to coulomb repulsion. However, placement of two cells such that they approach via only one corner leads to polarity switch from / to \ composition or vice versa (see the two middle cells in Fig. 2(a)).

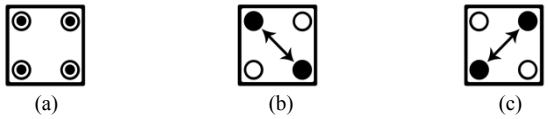

Fig. 1. QCA cell, (a): empty, (b): "1" polarity, (c): "0" polarity.

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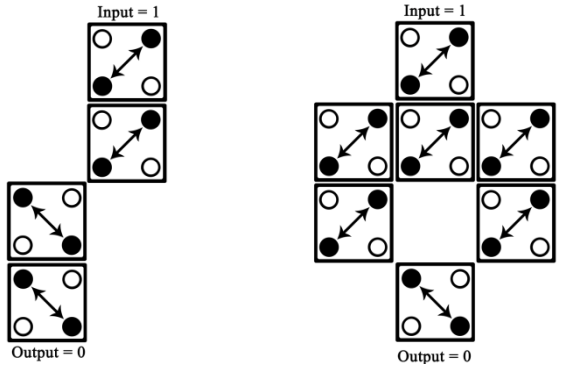
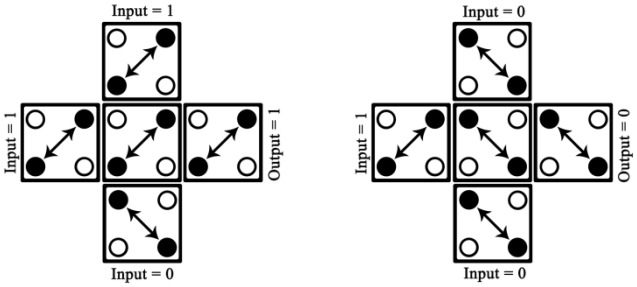


(a) (b)

Fig. 2. (a) QCA inverter, (b) A robust inverter.



(a) (b)

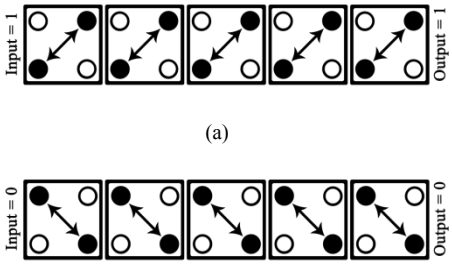
Fig. 3. QCA majority gates: (a) majority "1", (b) and majority "0".

A. QCA gates

There are two primary QCA gates:

1) QCA Inverter (QI): A pair of orthogonal / and \ cells, as the two middle cells in Fig. 2(a), works as a QCA inverter. Note that the top and bottom cells are merely for input and output. For example, an input "1" is shown to be inverted in Fig. 2(a). Since there is a probability for each QCA cell to fail, a more robust double path inverter has been designed as in Fig. 2(b) [17].

2) QCA majority (QM) gate: Another more important primary QCA gate realizes the 3-input majority function. This gate is composed of five QCA cells with a cross-shape structure (see Fig. 3). Polarity of the central cell, as known as device cell, is enforced, via the coulomb repulsion, to be equal to the majority of polarities of three input cells. The device cell's polarity is transferred to the output cell. For example, Figs. 3(a) and 3(b) depict two QM gates with two "1" and two "0" inputs, respectively. Moreover, A QM gate with one input fixed to "0" or "1" acts as an AND or OR gate, respectively. Therefore, the combination of QM and QCA inverter make a complete logic set.



(a) (b)

Fig. 4. QCA wires: transmitting "1" (a) and "0" (b).

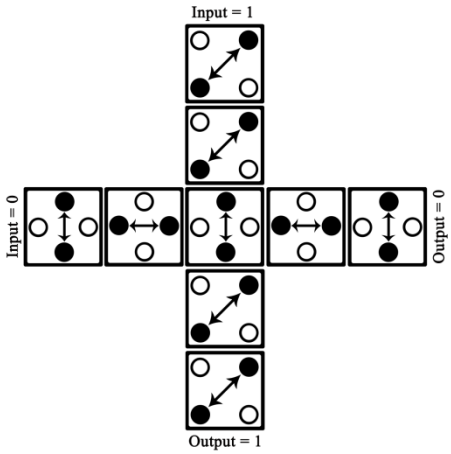


Fig. 5. A crossover with rotated cells.

B. QCA transmission wire

An array of QCA cells is capable of transmitting a "1" or a "0", which enters the first cell, down to the last cell. This is called a QCA wire, where an input "1" or "0" enforces all the cells to / or \ polarity, as is depicted by Figs. 4(a) and 4(b), respectively.

C. Crossover

The collection of two intersecting QCA wires is known as a crossover (hereafter also referred to as QX). There are a few crossover design alternatives that are briefly described below:

- **Multi-layer approach**: This QX architecture uses two substrate layers to avoid interference [18].
- **Coplanar approach**: One-layer QX is possible via 45-degree rotation of all QCA cells of one of the wires, as in the horizontal wire of Fig. 5 [4]. This structure is unfortunately not robust enough [12] [10].
- **Multi-phase clocking scheme**: A more robust QX that is presented in [13], uses three types of clock signals for time division multiplexing. This is supported by an 8-phase clocking scheme that tends to slow down the transmission.
- **Ternary cell approach**: Yet another coplanar robust crossover technique [19], uses a ternary cell at the intersection of the two wires, which tends to consume additional QCA area.

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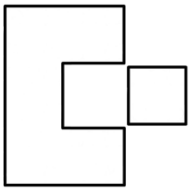
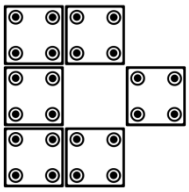
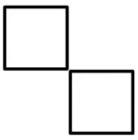
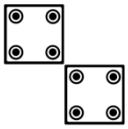
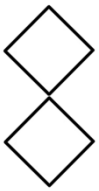
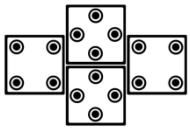
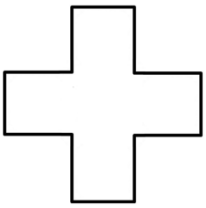
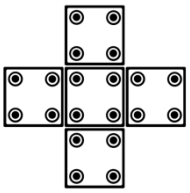
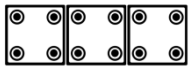
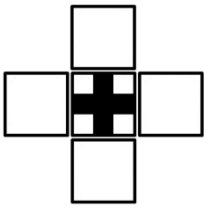
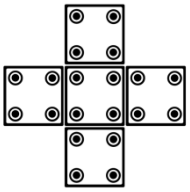
- **Logical crossing**: This scheme uses XOR gates without wire crossings. However, its area and latency overheads are considerably high [11].
- **Clock-zone based approach**: The most recent, robust, fast, and low cost coplanar QX design, is due to [15], and [14]. In this design, the phase difference of the two clock zones, corresponding to the two crossing wires, is 180 degrees. More details on this are provided in Section IV.A.

Table I contains the abstract symbols and actual layout for the above QCA components. The abstractions can be used for illustration of composite QCA circuit (e.g., full adder).

TABLE I
QCA COMPONENT SYMBOLS

QCA primary component		Abstract symbol	Actual
QI (Not)	Robust		
	Corner approach		
	Rotated		
QM (Majority)			
Wire			
QX (Crossover)			

D. QCA fabrication technologies

QCA cells are realized within different fabrication technologies [20]; namely Metal Island [21], Semiconductor [22], Molecular [23], and Magnetic [24]. First two products require very low working temperature, while those of others work in room temperature. The Molecular alternative provides very small QCA cells (contrary to Magnet) with ultra high working frequency. However, there are some shortcomings such as difficulty of realization of rotated cells [25].

III. RELATED WORKS

In this section, we provide brief descriptions for the previous QFAs and QCA adders.

A. QCA full adders

The simplest description of full adders in terms of majority and inverting functions, that we have encountered, is due to [26], as is described by Eqn. set 1, which can be realized via three QMs and two QIs.

$$c_{out} = \mathcal{M}(x, y, c_{in}),\ S = \mathcal{M}(\overline{c_{out}}, \mathcal{M}(x, y, \overline{c_{in}}), c_{in}) \quad (1)$$

Given that $\overline{c_{out}} = \overline{(x \vee y)c_{in} \vee xy} = \overline{x \vee y} \vee \overline{xy}\ \overline{c_{in}}$, the sum equation can be verified as follows.

$$\begin{aligned} S &= \overline{c_{out}}\ c_{in} \vee (\overline{c_{out}} \vee c_{in})(xy \vee (x \vee y)\overline{c_{in}}) \\ &= \overline{c_{out}}\ (c_{in} \vee xy \vee x \vee y) \vee c_{in}xy \\ &= (\overline{xy}\ \overline{c_{in}} \vee \overline{x \vee y})(c_{in} \vee x \vee y) \vee c_{in}xy \\ &= \overline{c_{in}}(x \oplus y) \vee c_{in}(xy \vee \overline{x \vee y}) \\ &= x \oplus y \oplus c_{in} \end{aligned}$$

Another sum formula has been recently proposed in [8], where one of the inverters is omitted, at the cost of increasing the sum latency by that of one QM. This formula is presented and justified in Eqn. 2.

$$\begin{aligned} s &= \mathcal{M}(\overline{c_{out}}, \mathcal{M}(c_{in}, y, \overline{c_{out}}), x) \\ &= \overline{c_{out}}\ x \vee (\overline{c_{out}} \vee x)(c_{in}y \vee (c_{in} \vee y)\overline{c_{out}}) \\ &= \overline{c_{out}}(x \vee y \vee c_{in}) \vee xc_{in}y \\ &= (\overline{x}\ \overline{y} \vee \overline{x}\ \overline{c_{in}} \vee \overline{c_{in}}\ \overline{y})(x \vee y \vee c_{in}) \vee xc_{in}y \\ &= \overline{x}\ \overline{y}c_{in} \vee \overline{x}\ \overline{c_{in}}y \vee x\overline{y}\ \overline{c_{in}} \vee xyc_{in} \\ &= x \oplus y \oplus c_{in} \end{aligned} \quad (2)$$

B. QCA n-bit adders

Following the alternative n-bit adder designs (e.g., ripple carry, carry look-ahead, parallel prefix) that are commonly realized in CMOS, similar QCA adders have been proposed that are briefly described below.

- **Ripple carry QCA adder:** The first QCA adder that we have encountered is due to [2], where a straightforward n-bit ripple carry adder is realized via cascading n QFAs.
- **Carry flow adders**: This is basically the same as the previous design, except for the c_{in}-c_{out} delay that is reduced to ¼ clock cycle [6].
- **Conditional sum QCA adders:** Conditional sum adders have been realized in QCA via mimicking the corresponding CMOS architectures in [9] (i.e., replacing the basic AND, OR, NOT, MUX, and FA cells with their QCA counterparts).
- **Carry look-ahead (CLA) QCA adders:** Carry look-ahead QCA adder designs with 4-bit basic blocks are offered in [5][9][27], where the group generate and group propagate signals are realized in a straightforward manner

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based on QCA equivalent cells for AND and OR gates. However, Pudi and Sridharan [28] have efficiently used QMs in realizing group generate signals, as is reproduced and justified in Eqn. 3, where G/P variables denote group generate/propagate signals, p_l/g_l refer to the propagate/generate signal in 2^l-weighted position, and it is well known that $g_l p_l = g_l$, and $g_l \vee p_l = p_l$.

$$G_{l:i} = M\left(G_{l:j}, p_l, P_{l-1:j} G_{j-1:i}\right) =$$
$$G_{l:j} p_l \vee (G_{l:j} \vee p_l) P_{l-1:j} G_{j-1:i} =$$
$$(g_l \vee p_l G_{l-1:j}) p_l \vee (g_l \vee p_l G_{l-1:j} \vee p_l) P_{l-1:j} G_{j-1:i} =$$
$$(g_l \vee p_l G_{l-1:j}) \vee p_l P_{l-1:j} G_{j-1:i} = G_{l:j} \vee P_{l:j} G_{j-1:i} \quad (3)$$

- **Parallel prefix QCA adders:** Straightforward realization of parallel prefix QCA adders would implement the group generate, propagate, and carry signals, based on QCA AND and OR gates, with total of two QMs per parallel prefix node. However, that of [8] uses only one QM to derive the generate output of parallel prefix nodes whose left input pair is an original one (e.g., first level nodes of all parallel prefix realizations, and last level nodes of Brent-Kung network). This can be justified via Eqn. 4.

$$G = g_l \vee p_l G_r = g_l p_l \vee (g_l \vee p_l) G_r = \mathcal{M}(g_l, p_l, G_r) \quad (4)$$

- **2-bit QCA adder cell:** A special n-bit adder design is based on radix-4 QCA adder cells, where the critical delay path for c_{in}-c_{out} consists of only one QM (i.e., half of the conventional design that uses two QCA FAs for the same 2-bit adder cell). However, this impressing speed-up is achieved at the cost of ten QMs, instead of six QMs of conventional 2-FA design [29].

IV. The new QFA and QCA ripple carry adder

Since the main contribution in the design of our new QFA is the utilization of the clock-zone based crossover of [15] and [14], we begin with the corresponding details in support of self containment.

A. Details of clock-zone based QX design

Fig. 6 depicts an instance of the utilized QX, where the clock-zones of vertical and horizontal wires are marked with 2, and 0, respectively, except for the central cell, which is unmarked, since either one can be valid, as is explained below. We actually take advantage of two zones of the four-phase zone-based clocking scheme of the QCADesigner. The aforementioned clocking marks correspond to Clock0, and Clock2 of the signal curves in Fig. 7, which is identically produced by Coherence vector and Bistable simulation engines with default QCADesigner parameters. This figure also shows that the Relax and Hold phases of Clock0 coincide with the Hold and Relax phases of Clock2, respectively. Therefore when the central cell is clocked by Clock2 (Clock0), signal X (Y) passes through.

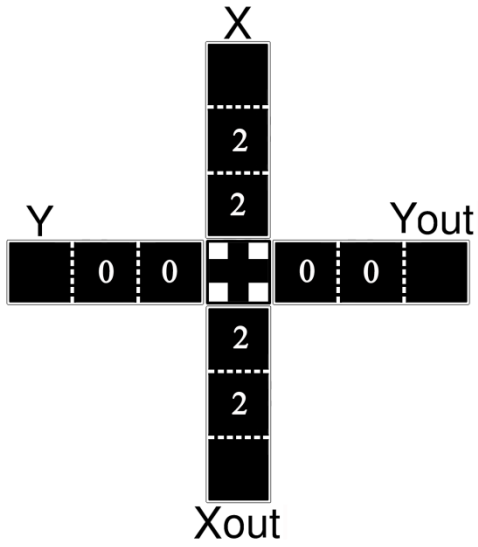

Fig. 6. Clock-zone based QX.

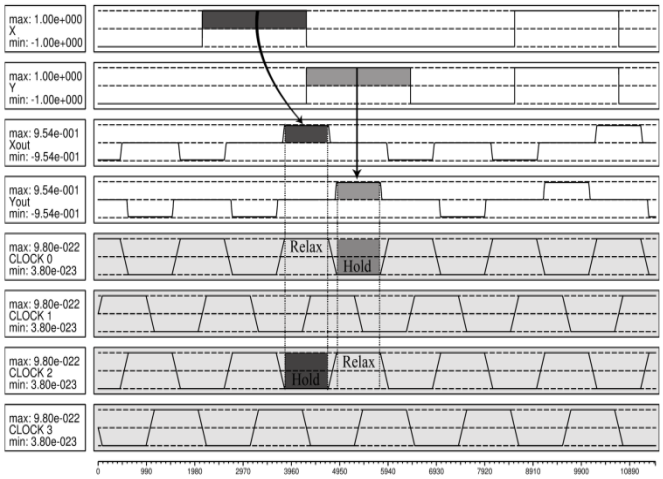

Fig. 7. I/O and clocking signals for clock-zone based QX.

B. The impact of clock-zone based QX in other technologies

Realization of coplanar QX via 45-degree rotated cells, as in [25], is difficult to fabricate in molecular technology. However, in the clock-zone based design, when the central cell is relaxing, the two adjacent cells can transform their polarity, as is experienced in [30]. Nevertheless, regarding the clocking floorplan, as is pointed out in [16], molecular QCA often use columnar regions, where phase difference of the clock signals for adjacent cells is 90 degree. This restriction can cause difficulty for the proposed crossover scheme to be realizable. Likewise, its fabrication in magnet technology can introduce difficult problems, especially due to its 3-phase clocking and columnar regions. In short the proposed design is best suited for semiconductor QCA.

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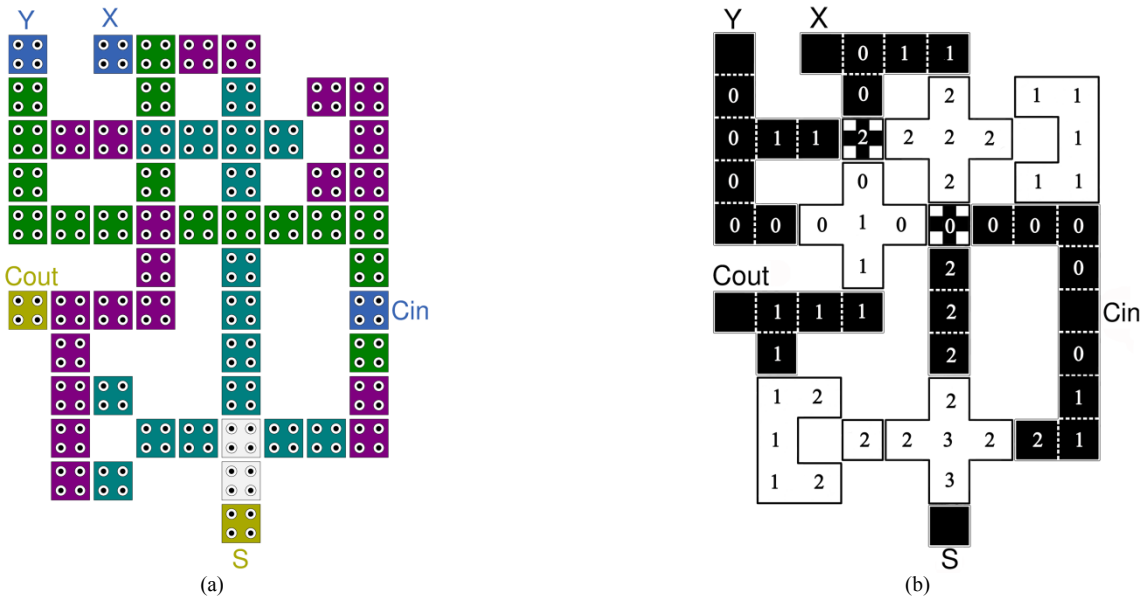

Fig. 8. The new coplanar QFA; a: QCADesigner layout, b: Symbolic layout with clock-zone numbers.

C. *The new QCA full adder*

We implement Eqn. 1 for the sum output and use simple QM for the carry output of our QFA, but utilize the clock-zone based QX of [14] and [15] for the required coplanar crossover wires. As such, Fig. 8a depicts the 1-level layout of the proposed QFA, where there are a total of 59 QCA cells, the latency is 1 clock cycle, and the area amounts to 0.043 μm^2.

To explain the function of this new QFA, we provide Fig. 8b, where the used symbols were described in Table I, and the numbers indicate the clock zones. This crossing over scheme, with 180 degree phase difference for the clock cycles of the two crossing wires, guarantees that the coplanar crossover wires work properly. Figs. 9a and 9b depict the correct functioning of the proposed QFA via the input/output signal patterns, for one FA and four cascaded FAs, respectively. These curves are provided by the QCADesigner [31], where the simulation engines, for Fig. 9a and 9b, are the same as those of Fig. 7.

D. *The new n-bit ripple carry QCA adder*

Recall the QFA of Fig. 8, where c_{in} and c_{out} placements are suitable for efficient cascading of FAs. We use these FAs to design n-bit carry flow adders. For example, Figs. 10 and 11 depict the QCA layout of these adders for $n = 4$, and $n = 32$, where the corresponding performance figures will be reported in the next section. Note the spiral sum paths, in the 32-bit architecture, which help in avoiding additional area cost.

V. Performance Evaluation and Comparisons

We evaluate the performance of our new QFA and the previous relevant designs via the conventional metrics. However, that of our QCA ripple carry adder and the previous QCA n-bit adders are evaluated via the composite metrics of [16].

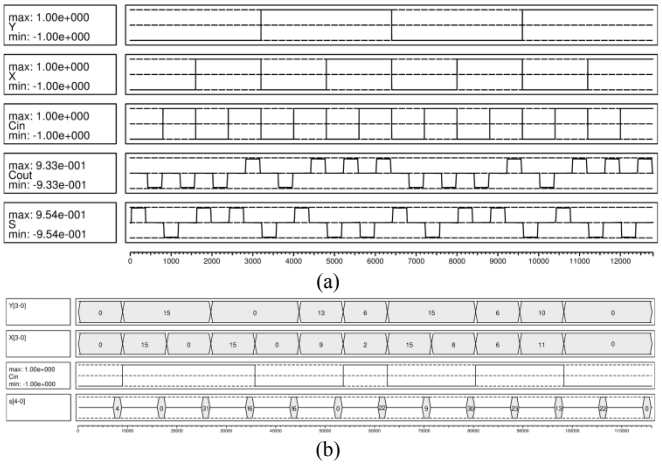

Fig. 9. I/O patterns for the proposed QCA Adder; a: Single FA, b: 4 FAs.

- **Evaluation of QFAs and adders via conventional metrics:** Table II contains the performance figures of several QFA realizations that are all based on Eqn. set 1, except for the one presented in [8], which is based on Eqn. 2. The ratios in this table clearly show the superiority of our design. In particular, the cell count and area of the proposed QFA is 145%, 272% (72%, 125%) less than that of [32] ([33]), which is also coplanar.

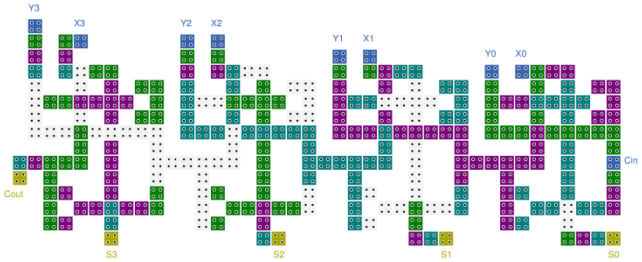

Fig. 10. The proposed 4-bit QCA adder.

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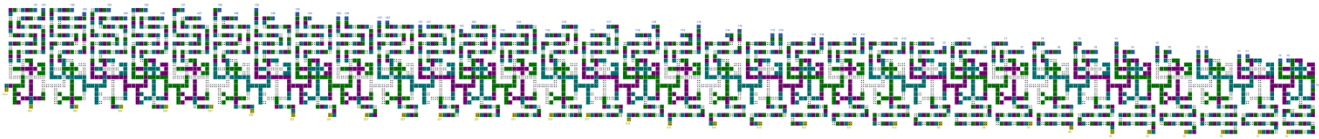

Fig. 11. The proposed 32-bit QCA adder.

TABLE II
COMPARISON OF QCA FULL ADDERS

QFA	Cell		Area		Latency	Layer
	Count	Ratio	μm^2	Ratio	(clk)	type
[34]	95	1.61	0.087	2.02	2	Multiple
[6]	73	1.23	0.080	1.86	¾	Multiple
[33]	102	1.72	0.097	2.25	2	Coplanar
[32]	145	2.45	0.16	3.72	1	Coplanar
[3]	93	1.57	0.087	2.02	1	Multiple
[8]	79	1.33	0.064	1.48	1	Multiple
New	59	1	0.043	1	1	Coplanar

Table III contains the figures of merit for some previously designed QCA n-bit adders for $n \in \{4, 8, 16, 32, 64\}$, where the cell count of the proposed adder is 9% (for 64-bit adder) to 29% (in case of 4-bit adder) less than the best previous results in [8]-RCA (i.e., the RCA of [8]). Regarding the area consumption, that of the proposed adder is 22%, 51%, 54%, and 69% less than that of the best previous one due to [8]-RCA, for 4-, 8-, 16-, 32-bit, without any delay penalty. Moreover, 49% area saving is experienced in the proposed 64-bit adder with respect to that of [29] (i.e., previously least area consuming), but at the cost of considerable speed loss.

TABLE III
PERFORMANCE FIGURES FOR VARIABLE SIZE QCA ADDERS

Adder	bit	Cell		Area		Latency
		Count	Ratio	(μm²)	Ratio	
New	4	262	1	0.208	1	7
	8	572	1	0.492	1	11
	16	1336	1	1.292	1	19
	32	3440	1	3.814	1	35
	64	9952	1	12.544	1	67
[8]-BK	4	680	2.59	0.645	3.10	7
	8	1782	3.11	1.49	3.02	10
	16	4350	3.25	3.55	2.74	16
	32	11825	3.43	10.77	2.82	27
	64	30145	3.02	31.20	2.48	46
[8]-RCA	4	339	1.29	0.254	1.22	7
	8	712	1.24	0.745	1.51	11
	16	1602	1.19	1.996	1.54	19
	32	3901	1.13	6.46	1.69	35
	64	10926	1.09	20.916	1.66	67
[28]-CLA	8	1785	3.12	1.456	2.95	9
	16	4114	3.07	3.672	2.84	15
	32	12540	3.64	11.83	3.10	27
	64	33302	3.34	35.62	2.83	49
[28]-CFA	8	1143	1.99	1.018	2.06	9
	16	2817	2.10	2.453	1.89	13
	32	6942	2.01	6.825	1.78	22
	64	17586	1.76	20.45	1.63	38
[6]	4	371	1.41	0.405	1.94	6
	8	789	1.37	0.9487	1.92	10
	16	1769	1.32	2.45	1.89	18
	32	4305	1.25	7.3	1.91	34
	64	11681	1.17	24.196	1.92	66
[29]	8	1606	2.80	1.13	2.29	8
	16	3587	2.68	2.66	2.05	12
	32	7691	2.23	6.65	1.74	20
	64	16667	1.67	18.72	1.49	36

- ***n*-bit QCA adder evaluation via QCA-specific cost function**: A new evaluation metrics, specific to QCA circuits, is recently proposed in [16], which is called QCA-specific cost function. A single, but composite, metric is defined such that different QCA cells (i.e., QM, QI, QX) have their own special share in the composite cost function. Eqn. 5 describes this new metric, where M, I, and C, represent the number of QMs, QIs, and QXs, respectively, and T refers to clocking time. The coefficients k, l, and p, all ≥ 1, can be determined to emphasize the power dissipation, complexity, and latency shares in the composite metric, where the authors of [16] have opted for $k = l = p = 2$, for performance evaluation of six different n-bit adders ($1 \leq n \leq 120$).

$$Cost_{QCA} = (M^k + I + C^l) * T^p \quad (5)$$

Following the same approach, we provide Fig. 12 that depicts the application of this metric on designs of [6], [8], [29], and ours, where the high cost for [29] appears to be mainly due to utilization of ten QMs and thirteen QXs per two bits. The cost function parameter C (see Eqn. 5), for the multi-layer designs of [6] and [8] is three times the cost of our coplanar QFA, which explains the take-off of the corresponding curve, towards the adders with wider bit-width. The higher stand of Brent-Kung parallel prefix adder of [8] can be explained by the extra QX, QMs and QIs. Regarding [28], the information required by the cost function is not available.

VI. CONCLUSION

Most of the QCA full adder designs use double-layer crossover, while there are few coplanar realizations that use 45° rotated cells. Given that more robust coplanar crossover designs, via clock phasing, have been proposed, we used this technique to design robust and efficient QCA full adders, whose cell count and area consumption are superior to all previous designs, while its latency is not more than that of any previous one, except for [6], whose area is 86% more than ours.

Our cell count is 23% less than the least cost previous one and the area of the proposed QFA is 48% less than the most compact previous one. We have used the proposed QFA in realization of 4-, 8-, 16-, 32-, and 64-bit ripple carry QCA adders, where 17-41% improvement in cell count and 22-69% in area consumption have been achieved, with regard to the best previous ripple carry QCA adder. Regarding the QCA-specific cost measurement of [16], cost of the proposed QFA design is far less than all the previous QCA adders including those with alternative carry accelerating techniques.

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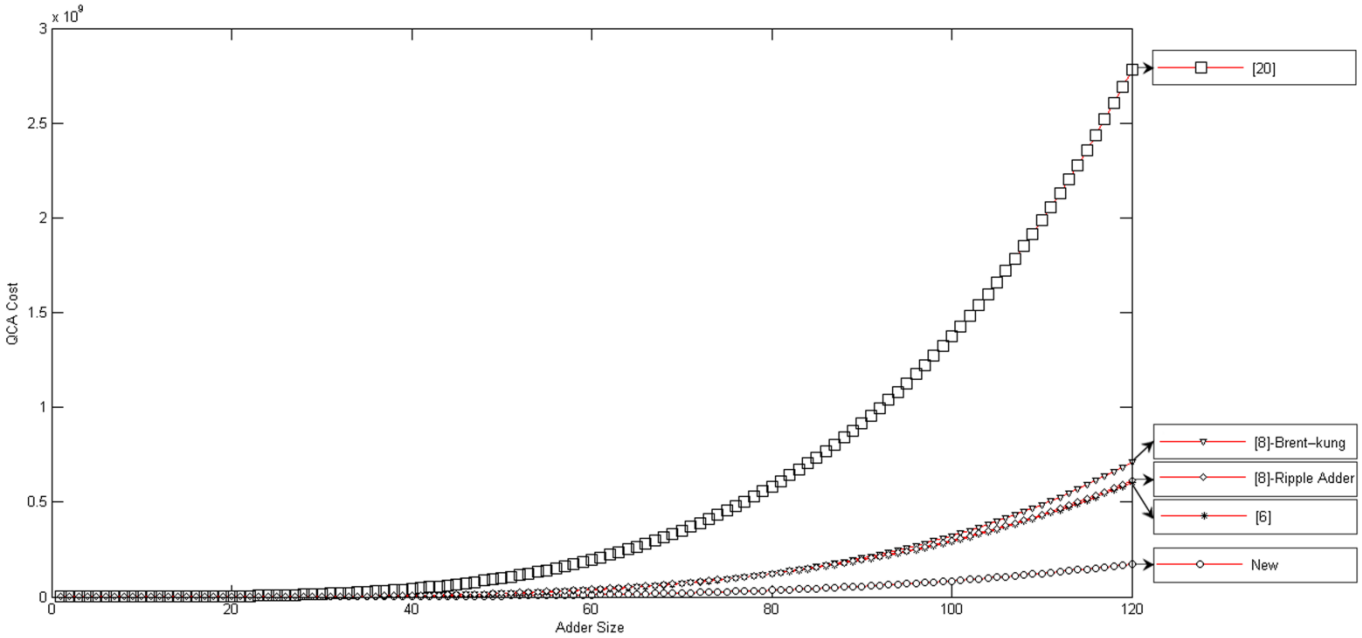

Fig. 12. QCA-specific cost function for five QCA adders.

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