Simulation study on short channel double-gate junctionless field-effect transistors*

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Abstract: We study the characteristics of short channel double-gate (DG) junctionless (JL) FETs by device simulation. Output I–V characteristic degradations such as an extremely reduced channel length induced subthreshold slope increase and the threshold voltage shift due to variations of body doping and channel length have been systematically analyzed. Distributions of electron concentration, electric field and potential in the body channel region are also analyzed. Comparisons with conventional inversion-mode (IM) FETs, which can demonstrate the advantages of JL FETs, have also been performed.

Key words: short channel effect; double-gate; junctionless field-effect transistor; device simulation
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1. Introduction

Currently, as MOSFET dimensions are scaled down to dozens of nanometers, the short channel effect (SCE) seriously affects the behavior of devices. In the nanoscale, the influence of SCE on the characteristics of conventional MOSFETs cannot be ignored. In order to reduce this influence, multi-gate structures such as double-gate (DG), surrounding-gate and FinFETs, which can suppress the SCEs and improve the capacity of control of the current, have been proposed[1−3]. However, to realize an ultrasharp doping profile between (for example) an n-type source/drain (S/D) region and a p-type body region still poses a great challenge for production of multi-gate MOSFETs at the nanoscale[4]. To solve this problem, a novel type of MOSFETs, named junctionless field-effect transistors (JL FETs), has been proposed. Compared to conventional inversion-mode (IM) MOSFETs, JL FETs need no p–n junction to form between the S/D region and the body channel region, which can be seen as n–n–n-type (n-channel) or p–p–p-type (p-channel) JL MOSFET devices. It is easier to achieve a good performance of JL FETs fabricated on an SOI wafer. Take an n–n–n-type JL FET as an example; it is turned off by piping out the electrons from the body region by the gate electric field force to make the body fully depleted at lower gate bias. Thinner silicon films block the channel more easily, and then the channel region achieves complete depletion. From the standpoint of the electric potential distribution, the channel energy band bends due to the reduction of the gate voltage and a strong barrier is formed between the source and drain which makes it difficult for electrons to flow from the source to drain. As the gate bias is increased, the depletion of the body region is eliminated gradually. With the increase of the electron concentration, the resistance also decreases. When the electron concentration reaches body doping concentration N_D, the channel region under the gate becomes electrically neutral. Further increasing gate voltage increases the accumulation of the electrons at the interface between the gate oxide and the silicon film. This makes the device resistance greatly reduced and form a good conductive state under a certain drain-to-source voltage. Then the device is turned on. Therefore, different from traditional n–p–n-type or p–n–p-type IM MOSFETs, junctionless FETs use majority carriers for transport between source and drain. That means it is an accumulation mode MOSFET. From the macroscopic point of view, the gate acts as a good control switch, which turns off the device at low gate bias and turns on at high gate bias on the premise that the silicon film is thin enough. This kind of device will not only assure that the device can work well like a conventional MOSFET, but also avoid the need for sharp doping concentration gradient switching from n-type to p-type. Such kind of MOSFETs greatly reduces the requirements of the fabrication process. At present, some research groups have performed some related studies of JL FETs with a double-gate structure, including investigating the theoretical foundations to better understand the behavior of the device[5], analysis of the turned-on characteristics of the device at different drain voltages and the potential under various operating conditions[6], etc. All these above analyses are performed under the assumption that the channel length is long enough, therefore, SCEs are ignored. Also some other investigations preliminarily studied the performances of silicon junctionless nanowire transistors in terms of SCEs such as turn-on characteristics, output characteristics and room-temperature subthreshold slope as a function of gate voltage[7]. However, it is necessary to provide a more detailed study on its operating characteristics in the situation of SCEs. The main purpose of this work is to investigate the characteristics of short channel DG JL FETs by simulations using SILVACO Atlas[8]. The influence on the devices' characteristics of changes in design parameters such as body doping, thickness of silicon body, and channel length has been performed systematically. Also, we compare the difference between DG

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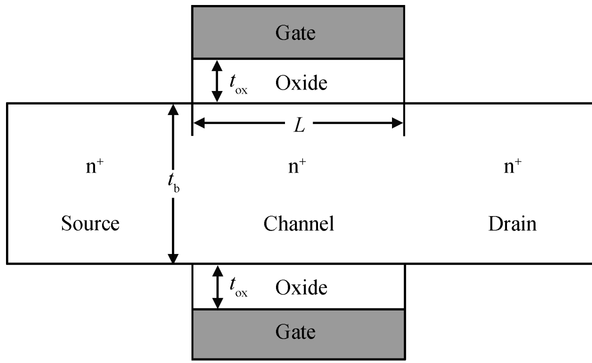

Fig. 1. 2D schematic view of a DG JL FET. The S/D region and body region of the JL FET have the same doping type and concentration. L is the channel length; t_b and t_{ox} are respectively the thicknesses of the silicon body and the gate oxide.

JL FETs with conventional DG MOSFETs, and give a detailed analysis on the principle of DG JL FETs by illustrating the on-state distributions of the electron density, the electric field, and the potential in the silicon body channel region of DG JL FETs. In this paper, the silicon body thickness t_b of each junctionless device is above or equal to 5 nm, so that the quantum effect can be neglected[9].

2. Properties simulation

2.1. Turn-on characteristics and output characteristics

Figure 1 represents the 2-D schematic view of the DG JL FETs. Here, L is the channel length; t_b and t_{ox} are the thicknesses of silicon body and gate oxide, respectively. The channel width is marked as W. N_D and N_A represent the uniform impurity concentration for n-type and p-type FETs. The S/D region and body region of a JL FET have the same doping type and concentration. Both the top and the bottom of the device have a gate electrode to control the device. Take n-type DG JL FETs as an example. We define t_{ox} 1.5 nm of every device and simulate the DG JL FETs by using SILVACO Atlas.

The design parameters of the DG JL FETs are selected as $L = 30$ nm, $W = 10$ nm, $t_b = 10$ nm, $N_D = 1 \times 10^{18}$ cm^{-3}. Figure 2(a) shows the turn-on characteristics of the DG JL FET with drain-to-source voltage $V_{DS} = 1$ V. Figure 2(b) plots the output characteristics of the same DG JL FET for a gate-to-source voltage V_{GS} ranging between 0.5 and 1.3 V in steps of 0.2 V. A comparison of the turn-on characteristics between a DG JL FET and DG IM FETs is shown in Fig. 2(c). Here, both devices' parameters are $L = 50$ nm, $W = 10$ nm, $t_b = 10$ nm, $N_D = N_A = 5 \times 10^{18}$ cm^{-3}. The JL FET's threshold voltage V_T is smaller than the IM FET's with the same V_{DS} ($V_{DS} =$ 1 V). The traditional MOSFETs' threshold voltage is regulated, making it equal to the threshold voltage of DG JL FETs. It can be seen from the figure that the DG JL FET has a very similar property as the DG IM MOSFET. Figure 2(d) shows the comparison of the distribution of electron concentration between the two devices above with the same V_{GS} ($V_{GS} = 0.2$ V) and V_{DS} ($V_{DS} = 0.05$ V) in the perpendicular direction of the channel at the point of L/2. The influence on devices of V_{DS} can be ignored when $V_{DS} = 0.05$ V. Under the same conditions, the

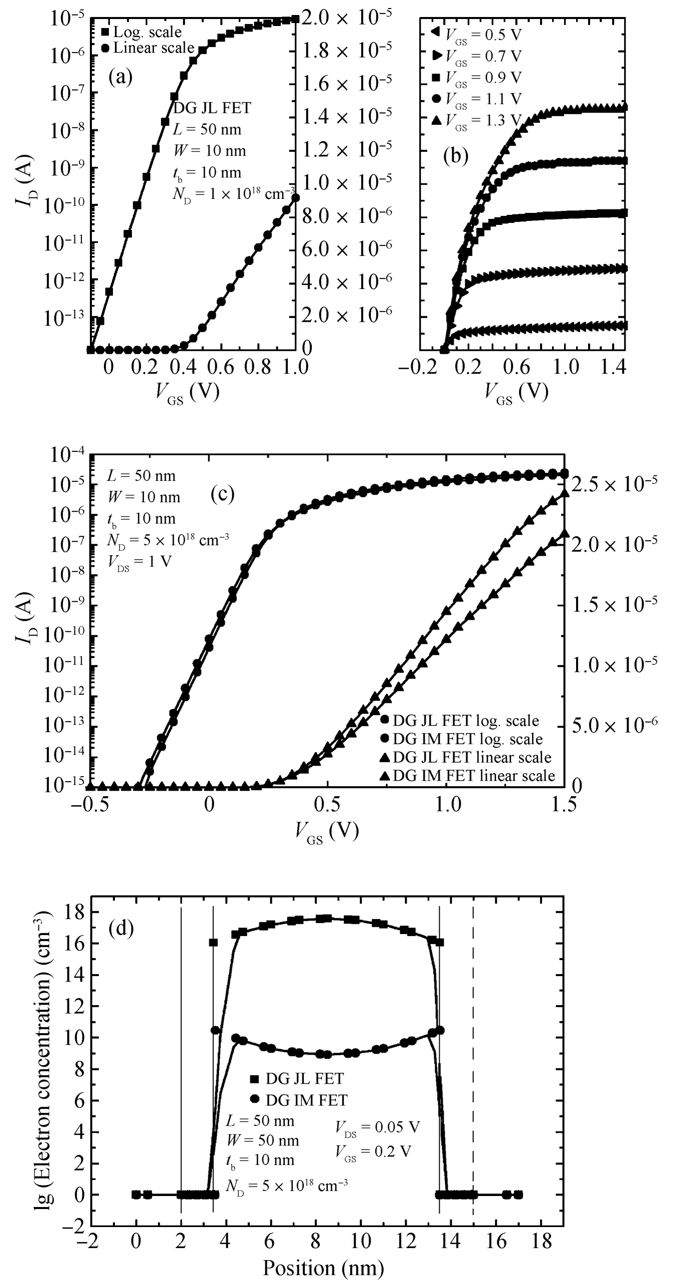

Fig. 2. (a) Turn-on characteristics of the DG JL FET with $V_{DS} = 1$ V. (b) Output characteristics of the DG JL FET for V_{GS} ranging between 0.5 and 1.3 V in steps of 0.2 V. The device parameters are $L = 30$ nm, $W = 10$ nm, $t_b = 10$ nm, $N_D = 1 \times 10^{18}$ cm^{-3}. (c) Comparison of turn-on characteristics between DG JL FET and DG IM FETs. We regulate the conventional MOSFET's threshold voltage, making it equal to the V_T of the DG JL FETs. The two curves are similar. (d) Comparison of the distribution of electron concentration between the two devices above with the same V_{GS} ($V_{GS} = 0.2$ V) and V_{DS} (V_{DS} = 0.05) in the perpendicular direction of channel at the point of L/2. The parameters of both devices are $L = 50$ nm, $W = 10$ nm, $t_b =$ 10 nm and $N_D = N_A = 5 \times 10^{18}$ cm^{-3}.

electron concentration of JL FETs is higher than conventional MOSFETs, which explains that in this case, the JL FET needs a smaller V_{GS} to be turned on, and leads to a lower threshold voltage.

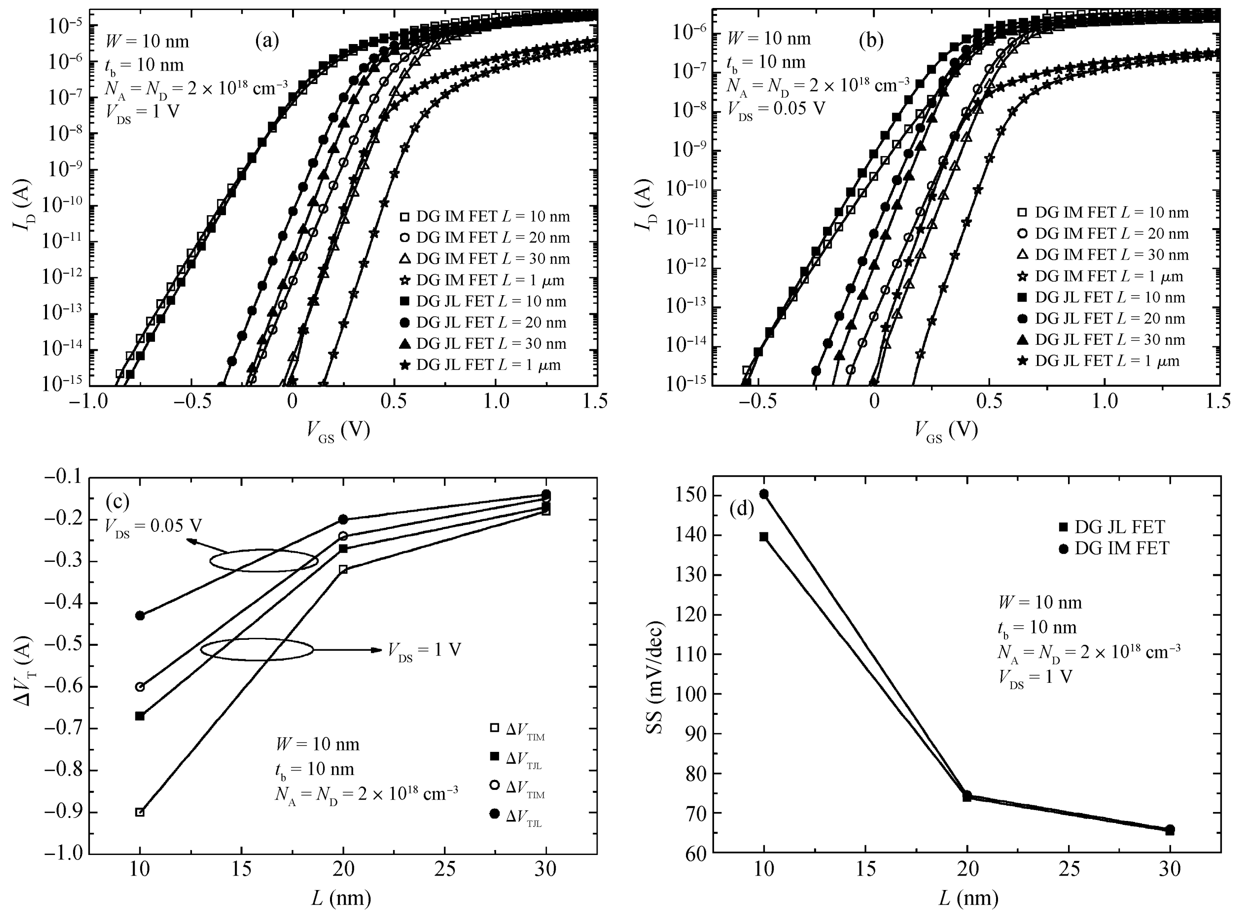

Fig. 3. Impact of channel length of junctionless and conventional devices. (a) Comparison of the turn-on characteristics of junctionless and conventional devices. The two devices parameters are $W = 10$ nm, $t_{\mathrm{b}} = 10$ nm and $N_{\mathrm{D}} = N_{\mathrm{A}} = 2 \times 10^{18}$ cm^{-3}, and the changes of the channel length are both set to 10 nm, 20 nm, 30 nm and 1 μm. The V_{DS} is set to 1 V. (b) Turn-on characteristics of the two devices for $V_{\mathrm{DS}} =$ 0.05 V. In the both of the two situations above, the threshold voltages of the two devices decrease with the diminution of the channel lengths and the change of junctionless DG MOSFETs is smaller than conventional DG MOSFETs. (c) Curve of ΔV_{T}-channel length. Calculate the difference between the threshold voltage with $L = 1$ μm and the threshold voltage with $L = 10$ nm, 20 nm, 30 nm of junctionless and conventional DG MOSFETs, respectively. (d) Influence of channel length on SS. Change the L of the two kinds of devices to 10 nm, 20 nm and 30 nm. SS increases with the decrease of L and the influence on SS of L of DG JL FET is smaller than DG IM FET.

2.2. Influence of channel length

2.2.1. Impact of channel length on threshold voltage

Figure 3(a) shows the comparison of the turn-on characteristics of junctionless and traditional devices. The body doping types of the two kinds of devices are n-type and p-type, and the doping concentrations are both 2×10^{18} cm^{-3}. The thicknesses of the two devices are 10 nm, and the changes of the channel length are both set to 10 nm, 20 nm, 30 nm, and 1 μm. V_{DS} is set to 1 V. As shown, the threshold voltages of the two devices decrease with the diminution of the channel lengths and the change of V_{T} of the DG JL MOSFETs is smaller than for DG IM MOSFETs, which means a shorter channel length has less impact on DG JL MOSFETs than on DG IM MOSFETs. Figure 3(b) shows the turn-on characteristics of devices with $V_{\mathrm{DS}} = 0.05$ V. Then we can ignore the impact of the V_{DS} on devices. Both of the two threshold voltages reduce when the channel length gets shorter, but it also can be observed that the influence of the DG JL MOSFETs on V_{T} is smaller. In the case of $V_{\mathrm{DS}} = 1$ V and $V_{\mathrm{DS}} = 0.05$ V, we calculate the difference between the V_{T} with $L = 1$ μm and the V_{T} with $L = 10$ nm, 20 nm, 30 nm of junctionless and traditional DG MOSFETs, respectively. The curve of the ΔV_{T}-channel length is shown in Fig. 3(c). From the graph, the influence of channel length change on the threshold voltages of both kinds of devices can be seen more intuitively. When the channel length is reduced to 10 nm, even at lower V_{DS} of 0.05 V, the DG IM MOSFET's threshold voltage change is approximately 0.6 V, but the DG JL MOSFET's threshold voltage change is about 0.43 V. The result is the same for higher drain-to-source voltage.

2.2.2. Influence of channel length on the subthreshold slope

The subthreshold slope (SS) affects the quiescent current and converting power consumption, which is defined as the slope of the gate voltage versus the log of the drain current below the threshold (mV/dec).

$$\mathrm{SS} = \frac{\mathrm{d}V_{\mathrm{G}}}{\mathrm{d}\lg I_{\mathrm{D}}}.$$

The value taken as the SS is the most dramatic change in the subthreshold region. SS is also an important physical quantity to measure the conversion speed of the device from the off

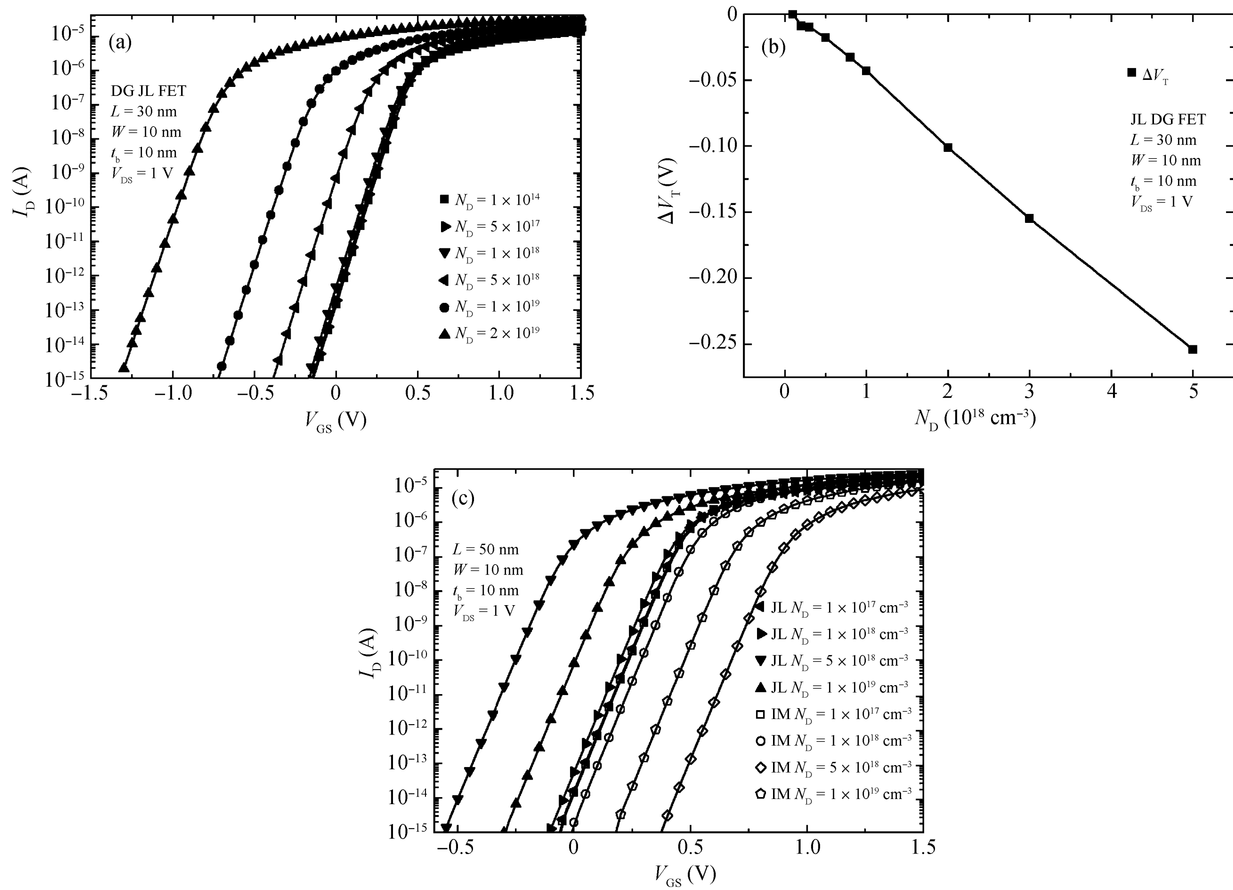

Fig. 4. (a) Influence of the doping concentration on DG JL FETs. The parameters of the DG JL FET are $L = 30$ nm, $W = 10$ nm, $t_b = 10$ nm. Change the doping concentration of nanowire respectively to 1×10^{14} cm^{-3}, 5×10^{17} cm^{-3}, 1×10^{18} cm^{-3}, 5×10^{18} cm^{-3}, 1×10^{19} cm^{-3} and 2×10^{19} cm^{-3}, then compare their turn-on characteristics for $V_{DS} = 0.05$ V. The V_T decreases with the addition of doping concentration of channel. When the doping concentration exceeds a certain value, the device V_T is negative. The change of V_T is not obvious at lower doping concentration. (b) Curve of ΔV_T-channel length of the DG JL FET. Calculate the difference between the threshold voltage with $N_D = 1 \times 10^{17}$ cm^{-3} and the threshold voltage with $N_D = 1 \times 10^{17}$ cm^{-3}, 2×10^{17} cm^{-3}, 3×10^{17} cm^{-3}, 5×10^{17} cm^{-3}, 8×10^{17} cm^{-3}, 1×10^{18} cm^{-3}, 2×10^{18} cm^{-3}, 3×10^{18} cm^{-3} and 5×10^{18} cm^{-3} of DG JL MOSFETs respectively. (c) Changes of V_T with doping concentration of DG JL FETs and traditional DG MOSFETs. The parameters of the both devices are $L = 30$ nm, $W = 10$ nm, $t_b = 10$ nm. Change N_D and N_A to 1×10^{17} cm^{-3}, 1×10^{18} cm^{-3}, 5×10^{18} cm^{-3} and 1×10^{19} cm^{-3}. The JL FET V_T decreases with the augment of nanowire doping concentration of the JL FET, while the traditional MOSFET V_T increases instead.

state to the open state[4], and illustrates the speed of the device to open. The smaller SS a device has, the faster the device opens. We simulate the SSs of the DG JL FET and the DG IM FET above with the same parameters for $L = 10$ nm, 20 nm and 30 nm. Figure 3(d) shows the curve of SS–L of the two devices. It can be seen that the SS increases with the decrease of L. However, the influence on the SS of L of the DG JL FET is smaller than the DG IM FET.

2.3. Influence of the doping concentration

We take the case of the DG JL FET with $L = 30$ nm, $W = 10$ nm, $t_b = 10$ nm. With different doping concentrations of nanowire, 1×10^{14} cm^{-3}, 5×10^{17} cm^{-3}, 1×10^{18} cm^{-3}, 5×10^{18} cm^{-3}, 1×10^{19} cm^{-3}, 2×10^{19} cm^{-3}, we then compare their turn-on characteristics, as shown in Fig. 4(a). We can observe that the V_T decreases with the addition of the doping concentration of the channel. Higher doping concentration induces a higher electron concentration in the body region for the same V_{GS}. In other words, for the higher doping case, more major carriers will be present in the channel and make the body region more difficult to be fully depleted. When the doping concentration is too high to be fully depleted, we need a more negative voltage to realize almost no moving electrons in the channel. The V_T of the device is negative at this time. We calculate the differences between the threshold voltage V_T with different body doping concentrations of DG JL MOSFETs, respectively, and draw the curve shown in Fig. 4(b). We can more clearly observe the change in threshold voltage with channel doping concentration. Because JL FETs use majority carriers to get turned on, the greater the doping concentration of devices are, the more majority carriers the channel contains and the lower V_{GS} we need for device conduction. Therefore, the V_T of JL FETs decreases with the increasing doping concentration. While conventional MOSFETs use minority carriers instead. The greater channel doping concentration makes the body more difficult to form the inversion layer; the higher V_{GS} is needed to turn on the device. Therefore, the threshold voltages of conventional MOSFETs increase with the increase of channel doping concentration. Figure 4(c) makes a compari-

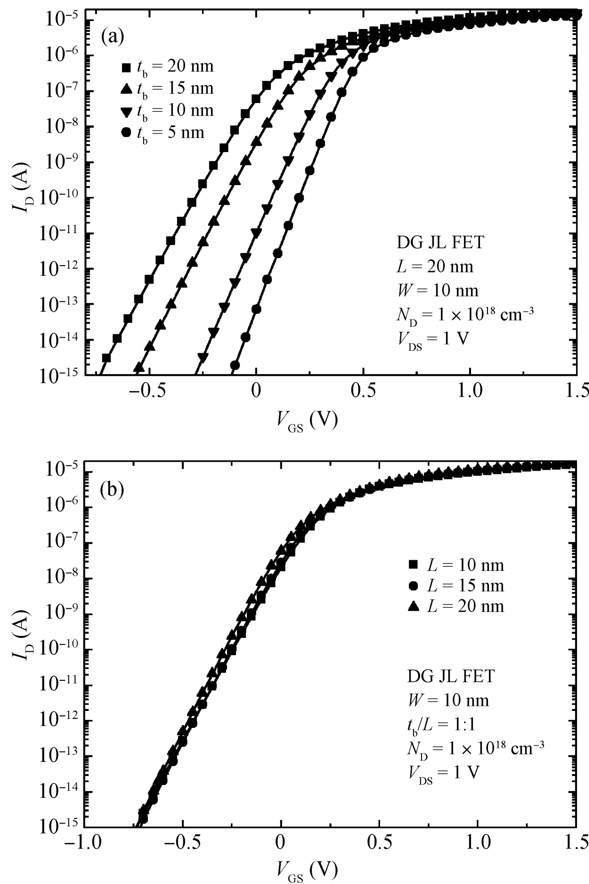

Fig. 5. (a) Influence of body thickness for DG JL FETs. Set the body thickness of the DG JL FET whose parameters are L = 30 nm, W = 10 nm, $N_D = 1 \times 10^{18}$ cm^{-3} to 5, 10, 15 and 20 nm. The V_T decreases with the addition of t_b. The SSs of the above four devices are 63, 72, 94, and 128 mV/dec separately. SS increases gradually with the increase of the body thickness. (b) Comparison of the turn-on characteristics of JL FETs with different channel lengths under the same situation of the ratio of body thickness to channel length. For two DG JL FETs with L = 10 nm, L = 15 nm and L = 20 nm, when their $t_b/L = 1$, their threshold voltages are very similar.

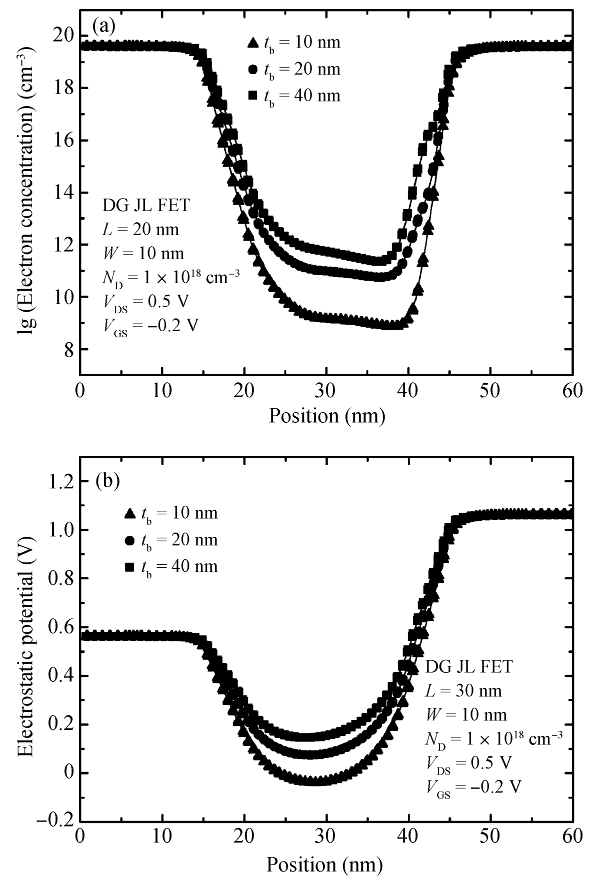

Fig. 6. Distribution of electron concentration and electrostatic potential in the channel direction with different t_b. Set the DG JL FETs' parameters as L = 20 nm, W = 10 nm, $N_D = 1 \times 10^{18}$ cm^{-3}, and different t_b as 10 nm, 20 nm and 40 nm, $V_{GS} = -0.2$ V, $V_{DS} = 0.5$ V. (a) The distribution of electron concentration with different t_b in the direction of channel at the point of 1 nm far from the surface of silicon body. (b) The distribution of electrostatic potential. The electron concentration and the potential increased with the increasing of t_b.

son between JL FETs and conventional MOSFETs with different doping concentrations. Two kinds of the devices have the same parameters which are L = 50 nm, W = 10 nm, t_b = 10 nm, and then different doping concentrations are set as 1×10^{17} cm^{-3}, 1×10^{18} cm^{-3}, 5×10^{18} cm^{-3} and 1×10^{19} cm^{-3} for different doping types. The different situations of threshold voltage change with the doping concentration of JL FETs and conventional MOSFETs can be seen.

2.4. Influence of body thickness

Set the DG JL FET's parameters as L = 20 nm, W = 10 nm, $N_D = 1 \times 10^{18}$ cm^{-3}, and the body thickness shifts from 5 to 20 nm. Figure 5(a) plots the comparison of the simulation results. Due to each device having the same channel length and width, the control area of the gate is the same. When the body thickness is different, the amount of majority carriers controlled by the gate is also different. Under the same lower gate bias in the subthreshold region, the more majority carriers the devices have, the more difficult it is for the depleted body region to form. Hence the threshold voltage decreases with the increasing of body thickness. The SSs of the above four devices are 63, 72, 94, and 128 mV/dec, respectively. SS increases gradually with the increase of the body thickness. In other words, with the decreasing of body thickness, the switching speed from the off state to the open state of the junctionless case is gradually increased and the control ability of gate bias is enhanced, too.

For the DG JL FET whose parameters are L = 20 nm, W = 10 nm, t_b = 20 nm and $N_D = 1 \times 10^{18}$ cm^{-3}, its ratio of body thickness to channel length (t_b/L) is 1. Figure 5(b) shows the comparison of three DG JL FETs with $t_b/L = 1$ but different L = 10 nm, 15 nm and 20 nm. The three curves are very similar.

2.5. Distributions of electron concentration and electrostatic potential in the channel direction with different t_b

Set the DG JL FETs' parameters as L = 20 nm, W = 10 nm, $N_D = 1 \times 10^{18}$ cm^{-3}, and different t_b as 10 nm, 20 nm and 40 nm, respectively. Set the V_{GS} and V_{DS} of the three

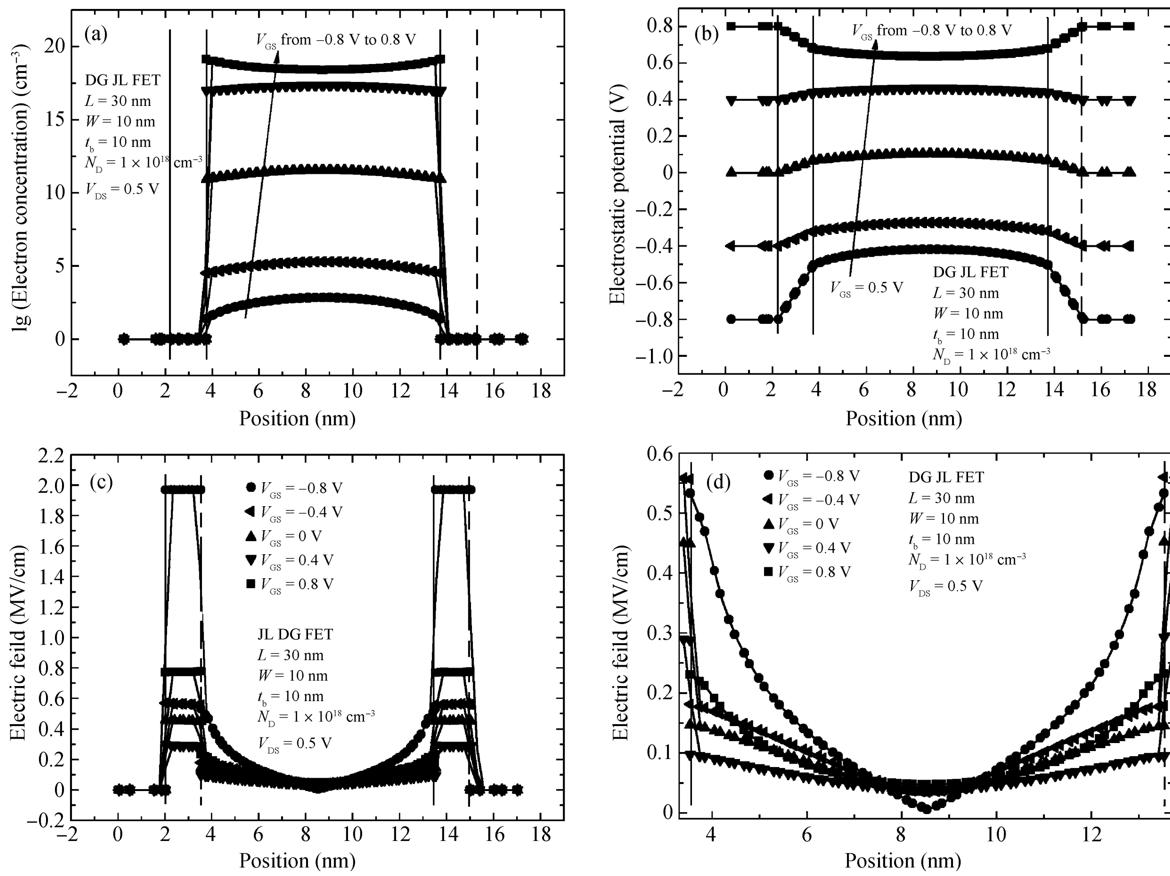

Fig. 7. Distribution of electron concentration, electric field and electric potential in the perpendicular channel direction. Set V_{DS} to 0.5 V and change the gate voltage (−0.8, −0.4, 0, 0.4, 0.8 V). (a) Comparison of the distribution of electron concentration in the perpendicular channel direction in different situations. (b) Distribution of electrostatic potential. (c) Distribution of electric field. (d) Partial enlargement of the electric field.

devices as −0.2 V and 0.5 V. The distribution of electron concentration and electrostatic potential with different t_b in the direction of channel at the point of 1 nm far from the surface of silicon body are shown in Fig. 6. Figures 6(a) and 6(b) report the electron concentration and the electrostatic potential, respectively. It can be seen that, when junctionless devices have the same channel length but different t_bs, in the subthreshold region, under the same biases, for example $V_{GS} = -0.2$ V and $V_{DS} = 0.5$ V, the thicker t_b case can contain more majority carriers in the channel body region, which makes it harder for the gate bias to deplete the channel region. As Figure 6(a) shows, the surface electron concentration for the larger t_b case is also higher. In other words, the surface potential for a larger t_b should be also higher, which can be seen in Fig. 6(b). Thereafter, for devices under the same biases, and with the same channel length but with different t_b, it can be predicted that more subthreshold current will be induced for larger t_b case. This prediction is consistent with the simulation results shown in Fig. 5(a).

2.6. Distribution of electron concentration, electric field and the electric potential in the perpendicular channel direction

Take a DG JL FET with the same parameters as $L = 20$ nm, $W = 10$ nm, $t_b = 10$ nm and $N_D = 1 \times 10^{18}$ cm^{-3} for example. Set V_{DS} to 0.5 V and change the gate voltage (−0.8, −0.4, 0, 0.4, 0.8 V). Figures 7(a), 7(b) and 7(c) report, respectively, the comparison of the distribution of electron concentration, electrostatic potential and electric field in the perpendicular channel direction in different situations. Figure 7(d) shows the partial enlargement of the electric field.

When the applied gate voltage is lower than a certain value, the strong electric force makes almost all of the electrons pipe out of the body region; the electron concentrations of both the body surface and body central region are very low, far lower than the doping concentration of silicon nanowire. It means that the whole body region can be approximately seen as fully depleted. The electron concentration in the surface region is lower than the central region because the control ability of V_{GS} is highest on the surface of body region, as the V_{GS} increase, the depletion is gradually eliminated, after V_{GS} reaches value of the flat band. When the applied gate voltage reaches the device threshold voltage, a certain amount of electrons are accumulated in the channel region to connect the source and drain. These variations also cause the curvature of the potential curve to gradually reduce to zero while both the surface and the central region recover to the neutral region. And as the gate voltage is further raised, the channel potential is continuously increased and the electrons will accumulate on the surface of the body region. In addition, the concentration of electrons near the surface region is higher than that in the central region.

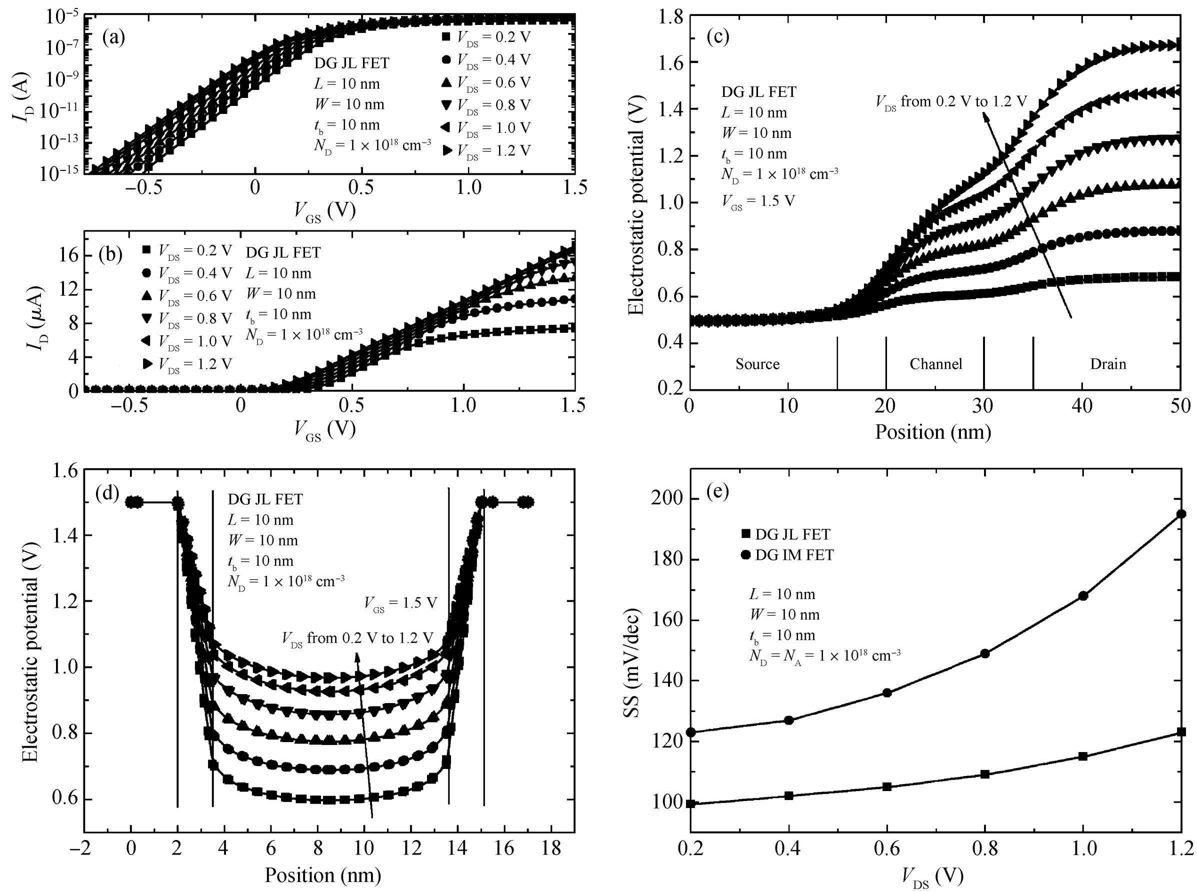

Fig. 8. (a) Turn-on characteristics in log of the DG JL FET for different V_{DS} (0.2, 0.4, 0.6, 0.8, 1.0, 1.2 V). (b) Turn-on characteristics in linear scales. (c) Distribution of electrostatic potential in the channel direction of the DG JL FET for V_{DS} ranging from 0.2 to 1.2 V in steps of 0.2 V and V_{DS} = 1.5 V at the point of $t_b/2$. (d) Distribution of electrostatic potential in the perpendicular channel direction at the point of $L/2$. The electrostatic potential increases with the increasing V_{DS}. (e) Curve of SS–V_{DS} of the two devices. SSs of both kinds of devices increase with the increase of V_{DS}. The influence on SS of DG JL FET of V_{DS} is smaller than that for DG IM FET.

2.7. Influence of drain voltage

Set the DG JL FET's parameters as L = 10 nm, W = 10 nm, t_b = 10 nm, $N_D = 1 \times 10^{18}$ cm^{-3}. Figures 8(a) and 8(b) plot the turn-on characteristics in log and linear scales of the DG JL FET for different V_{DS} (0.2, 0.4, 0.6, 0.8, 1.0, 1.2 V), respectively. It can be seen that the threshold voltage decreases with the increase of V_{DS}. Figure 8(c) shows the distribution of electrostatic potential in the channel direction of the DG JL FET for V_{DS} ranging from 0.2 to 1.2 V in steps of 0.2 V and V_{DS} = 1.5 V at the point of $t_b/2$. Figure 8(d) shows the distribution of electrostatic potential in the perpendicular direction of the channel at the point of $L/2$. The electrostatic potential increases with the increasing of V_{DS} in the two graphs.

Simulate the SSs of the DG JL FET above and DG IM FET with the same parameters for the six V_{DS} values. Figure 8(e) shows the curve of SS–V_{DS} of the two devices. SSs of both kinds of devices increase with the increase of V_{DS}. However, the influence on SS of V_{DS} of DG JL FET is smaller than DG IM FET, which means that JL FETs are more stable in this aspect.

3. Conclusion

We have simulated and analyzed the characteristics of DG JL FETs. From the simulation results, it can be seen that the DG JL FETs have all the properties of conventional DG MOSFETs. This paper analyzed the influence of doping concentration, channel length, and body thickness on the threshold voltages and subthreshold slope of short-channel JL FETs. In the same conditions, the impact of channel length and V_{DS} on JL FETs is smaller than for conventional FETs. Due to these advantages, in terms of SCEs, the JL FET can be a good choice.

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