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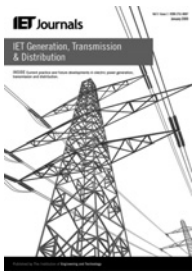

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Solid-state transient limiter for capacitor bank switching transients

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Abstract: Transient overvoltage and inrush current are two major transient phenomena which occur because of capacitor switching. In addition to power quality degradation, these transients lead to shortening the lifetime of the capacitor and switching device. In order to reduce these transients, a solid-state capacitor switching transient limiter (SSCSTL) is proposed in this study. The proposed SSCSTL has two operation modes: limiting mode and bypass mode. During the capacitor energising, a DC reactor and a varistor suppress inrush current and transient overvoltage, respectively. During the steady-state mode, the DC reactor is bypassed by a thyristor, so the SSCSTL acts as short-circuit and has no considerable effect on the circuit. The thyristor is triggered by using a new simple structure auto-triggering technique in normal condition. The proposed SSCSTL with a very simple structure as well as fast and reliable performance is an efficient solution to assure the capacitor switching without any transient overvoltage and inrush current. A prototype single-phase SSCSTL is simulated by electromagnetic transient program and tested. The simulation and experiment results show that the proposed SSCSTL considerably reduces the inrush current and transient overvoltage during switching of the capacitor.

1 Introduction

Power capacitor banks are widely used to improve the power factor in power systems. Closed to unity power factor has several advantages such as loss reduction in the distribution feeders, capacity increase of transmission lines and transformers, as well as the desired voltage profile. Owing to the continuous variation of the inductive loads in the power systems, capacitor banks should be switched on/off frequently by an automatic power factor regulator according to the required power factor in the substations or industrial plants [1]. However, transient overvoltage and inrush current arise in capacitor switching condition [2]. In addition to power quality degradation, such transients lead to a decrease in the lifetime of the capacitor and switching device. So, some standards have been recommended regarding the capacitor bank switching [3, 4]. Furthermore, several approaches have been proposed to restrain the capacitor switching transients, which are generally based on two concepts: increase the line impedance at the switching instant or close the switch contacts when the voltage across the contacts is zero. In [2], a series current limiting reactor is proposed to limit the capacitor switching transients. This method is simple and inexpensive, but a fixed reactor may cause system resonance. Therefore an increased voltage rating of the capacitor bank may be required when this technique is utilised. Pre-insertion resistor/inductor is another approach, suggested in [5, 6]. Zero-voltage switching of the switch contacts [7, 8] and power electronic control-based techniques [9–12] are other alternatives. These approaches require an additional control circuit, which leads to an increase in the cost and complexity. Furthermore, they are less reliable.

In this paper an efficient solid-state capacitor switching transient limiter (SSCSTL) is proposed for restriction of the capacitor switching transients. Upon switching, the SSCSTL goes to transient supersession mode so that a DC reactor limits the switching inrush current, and switching transient overvoltage is clamped by means of a varistor. After energisation of the capacitor bank, the SSCSTL goes to bypass mode and a thyristor (Th) bypasses the DC reactor, so the SSCSTL acts as a short-circuit path. Consequently, the SSCSTL has no effect on the circuit in steady state. The SSCSTL has a fast response time for switching between the limiting and bypass modes, which is <20 ms. It uses a simple and reliable auto-triggering circuit for energising the capacitor bank. As a result of the utilisation of a DC-type reactor, there is no concern about the series resonance. In addition to suppression of the capacitor switching transients, the SSCSTL limits the fault current in case of a fault occurrence in the capacitor bank.

The rest of the paper is organised as follows: in Section 2, configuration of the SSCSTL and its operation principles are presented. Section 3 develops the circuit analysis of the proposed limiter. In Section 4, performance of the SSCSTL is evaluated by using some simulation and experimental results. Finally, in Section 5 the results are concluded.

2 SSCSTL structure and its operation principle

A single-phase topology of the SSCSTL is considered to demonstrate its operation principle. However, it can be straightforwardly extended to a three-phase structure. In this

section, the structure of the proposed capacitor switching transient limiter is presented. Furthermore, duties of different parts of the SSCSTL are introduced. Finally, the SSCSTL operation modes will be discussed.

2.1 SSCSTL structure

The circuit structure of the SSCSTL is shown in Fig. 1. Its structure can be divided into two sections: power section and control section. The power section is composed of a DC reactor (L), an external resistance (R_E), a single-phase bridge rectifier or power rectifier (D_1–D_4), a Th and a high-power varistor (MOV_1). The control section includes a low-power transformer (T), a single-phase rectifier with low-power centre-tap transformer or control rectifier (D_a and D_b), and a voltage regulator (L7805). The DC reactor is connected to the DC side of the power rectifier, connected in parallel with a Th, series resistor-capacitor (RC) snubber components (R_s and C_s) and a varistor (MOV_2). In order to prevent core saturation in the DC reactor and reduce the remnant flux, the inductor core can be designed with an air gap. The inductor limits the inrush current of the capacitor switching. The varistor (MOV_2) and series RC components protect the Th against transient overvoltage switching. Operation voltage of MOV_2 is selected higher than the maximum of the supply voltage. The Th bypasses the inductor and snubber components in steady-state condition. A varistor (MOV_1) is also considered for transient overvoltage suppression of the capacitor switching. Operation voltage of MOV_1 is selected slightly higher than the operation voltage of MOV_2.

In the control section, a low-power 220/9 V transformer is connected in parallel with the capacitor bank. A single-phase rectifier with low-power centre-tap transformer feeds the trigger circuit. The regulator (L7805) is considered to protect the Th against overvoltage in gate cathode.

2.2 SSCSTL operation principle

Essential limiting elements of the proposed SSCSTL are a DC reactor/MOV varistor placed in series/parallel with the capacitor bank, respectively. Transient overvoltage during switching is suppressed by the MOV. Transient overcurrent is limited by the DC reactor. Accordingly, the proposed SSCSTL has two operation modes: limiting mode and bypass mode. In the limiting mode (during initial moments after the capacitor switching), capacitor voltage and secondary voltage of T are less than the required voltage for driving the Th. So, Th remains off and the DC reactor and external resistor limit the inrush current of the capacitor bank. In addition, the switching transient overvoltage is suppressed by the varistor MOV_1. In the bypass mode (after appropriate voltage build-up across the capacitor bank), secondary voltage of transformer T reaches a sufficient level, which turns-on the Th and so the DC reactor will be bypassed. In fact, the capacitor bank current passes through the Th and D_1–D_4, which forms a short-circuit path. The centre-tap rectifier and regulator L7805 are used for driving the Th.

The limiting and bypassing modes of the proposed SSCSTL can be categorised in two states of operation, which are described in the following section.

2.2.1 Energisation transient state: Suppose the capacitor bank has no charge in incipient moments of capacitor switching, so voltage across T is zero and Th is not turned-on by the auto-triggering circuit. Consequently, the DC reactor conducts capacitor bank current. So, the inrush current of capacitor switching will be suppressed by the DC reactor. In addition, the external resistance (R_E) helps to suppress the inrush current, and varistor MOV_1 suppresses transient overvoltage of the capacitor energisation as well.

2.2.2 Steady state: When the capacitor bank is charged and its voltage reaches around nominal voltage, the auto-triggering circuit is supplied by required voltage level. As a result Th can be triggered. So, the inductor is bypassed by Th after the energisation processes. In this condition, the DC reactor discharges in the internal resistance of the inductor (R_{int}), R_E and in the on-state resistance of Th. Owing to the low on-state losses of the Th, this state acts as short-circuit and SSCSTL has no effect on steady-state operation of the circuit.

3 Analysis and design of the SSCSTL

3.1 Circuit analysis

Suppose initial charge of the capacitor bank is zero. Therefore, when the capacitor bank is switched-on, Th is off during the charging process. Equivalent circuit of the SSCSTL in high impedance transient supersession mode is shown in Fig. 2. It is supposed that the energisation started at $t = t_0$.

In the equivalent circuit, L, R and V_{Df} are inductance of the limiter inductor, resistance of the circuit including inductor resistance and external resistance (R_E) and forward voltage of the diodes, respectively. For simplicity, it is supposed that in the capacitor switching only inrush current arises and no voltage transient appears, so the effect of the varistors and snubber can be neglected. Differential

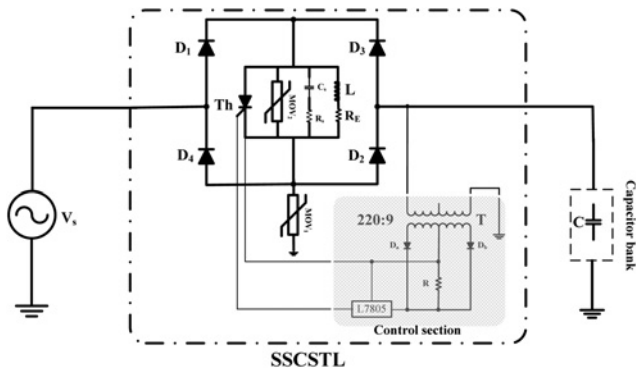

Fig. 1 *Proposed SSCSTL*

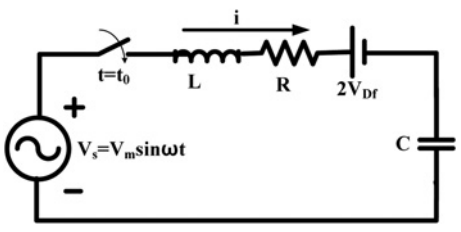

Fig. 2 *Equivalent circuit of the SSCSTL in the limiting mode*

equation of the equivalent circuit can be expressed as follows

$$Ri + L\frac{\mathrm{d}i}{\mathrm{d}t} + \frac{1}{C}\int i\mathrm{d}t = V_m \sin \omega t - 2V_{\mathrm{Df}} \tag{1}$$

Since inductance of the circuit is greater than its resistance in the limiting mode, the circuit response will be under-damped. Initial conditions of the circuit are supposed as: $v_c(t_0) = 0$, $i(t_0) = 0$ and $\mathrm{d}i(t_0)/\mathrm{d}t = (V_m \sin \omega t_0 - 2V_{\mathrm{Df}})/L$, where v_c denotes terminal voltage of the capacitor bank.

Current of this mode can be obtained by solving (1) as follows

$$i(t) = \frac{V_m}{Z}\sin(\omega t - \phi) + \mathrm{e}^{-\alpha(t-t_0)} \times \left[A \sin \omega_d(t - t_0) + B \cos \omega_d(t - t_0)\right] \tag{2}$$

where

$$Z = \sqrt{R^2 + \left(\omega L - \frac{1}{C\omega}\right)^2}, \quad \phi = \tan^{-1}\frac{(\omega L - (1/C\omega))}{R},$$
$$\omega_d = \sqrt{\omega_0^2 - \alpha^2}, \quad \alpha = \frac{R}{2L} \quad \text{and} \quad \omega_0 = \frac{1}{\sqrt{LC}}$$

Constants A and B can be calculated based on initial conditions as follows

$$A = \frac{V_m \sin \omega t_0 - 2V_{\mathrm{Df}}}{\omega_d L} - \frac{V_m}{\omega_d Z}\left[\alpha \sin(\omega t_0 - \phi) + \omega \cos(\omega t_0 - \phi)\right] \tag{3}$$

$$B = -\frac{V_m}{Z}\sin(\omega t_0 - \phi) \tag{4}$$

In the bypass mode, Th is triggered and the DC reactor will be bypassed. So the SSCSTL acts as short-circuit path. In this condition, the inductor discharges in the external resistance (R_E) and other resistance of the bypass circuit. Equivalent circuit of this mode is shown in Fig. 3. The on-state drop voltage of Th is ignored in order to more simplicity. It is supposed that the Th is triggered at $t = t_1$. Equation of the equivalent circuit can be written as follows

$$Ri + L\frac{\mathrm{d}i}{\mathrm{d}t} = 0 \tag{5}$$

where R denotes sum of the R_E and inductor internal resistance (R_{int}).

From (2), $i(t_1) = I$, this is an initial condition for the inductor discharging in the circuit shown in Fig. 3.

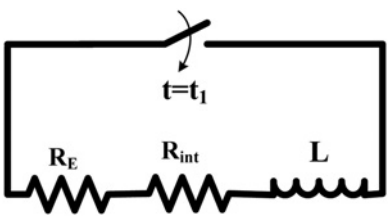

Fig. 3 *Equivalent circuit of the SSCSTL in the bypass mode*

Table 1 Prototype SSCSTL and the circuit parameters

Symbol	Quantity
V_s	220 V
L	1–50 mH
C	120–240 μF
C_s	47 nf
R_s	15 Ω
R	24 Ω
R_E	0.5 Ω
T	220/9, 500 mA
D_a, D_b	1N4001
regulator	L7805CV
D_1–D_4	VPI2560
Th	BTW69
MOV_2	681KD14J
MOV_1	821KD14J

Discharge current of inductor can be obtained by solving (5) as follows

$$i_{\mathrm{discharge}}(t) = I\mathrm{e}^{-(R/L)t} \tag{6}$$

3.2 Design of the SSCSTL

Inductance of the DC reactor can be calculated by using (1), in which a DC voltage is substituted with sinusoidal voltage v_s. For simplicity, it is assumed that the resistance of the DC reactor is negligible and R_E is not considered, so (1) will be rewritten as

$$L\frac{\mathrm{d}i}{\mathrm{d}t} + \frac{1}{C}\int i\mathrm{d}t = V_m - 2V_{\mathrm{Df}} \tag{7}$$

Considering the initial conditions which are: $v_c(t_0) = 0$, $i(t_0) = 0$ and $\mathrm{d}i(t_0)/\mathrm{d}t = (V_m - 2V_{\mathrm{Df}})/L$, by solving (7) and some approximations, the DC reactor value can be calculated from

$$L_d = \left(\frac{V_m - 2V_{\mathrm{Df}}}{I_{\mathrm{inrush}}}\right)^2 \times C \tag{8}$$

where I_{inrush} is magnitude of inrush current, expected to be restricted by the DC reactor.

Operation voltage of varistor MOV_2 is selected as 400 V, which is a little greater than the peak of the supply voltage. Current rating of Th is determined considering average on-state current of the switch and is selected based on the

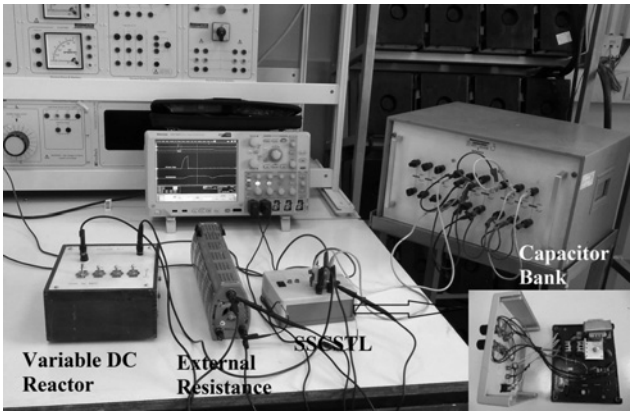

Fig. 4 *Test bench of a laboratory prototype of the SSCSTL*

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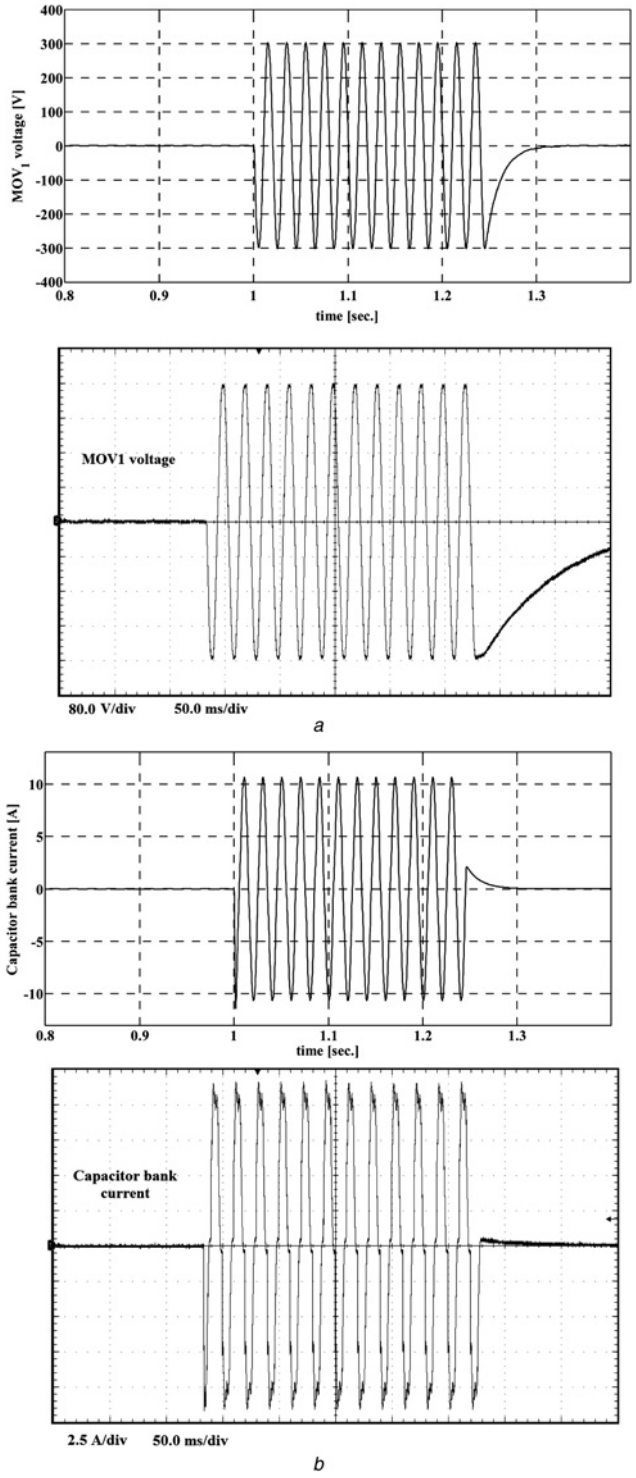

Fig. 5 *Simulation and experimental results of*
a MOV_1 voltage
b Capacitor bank current

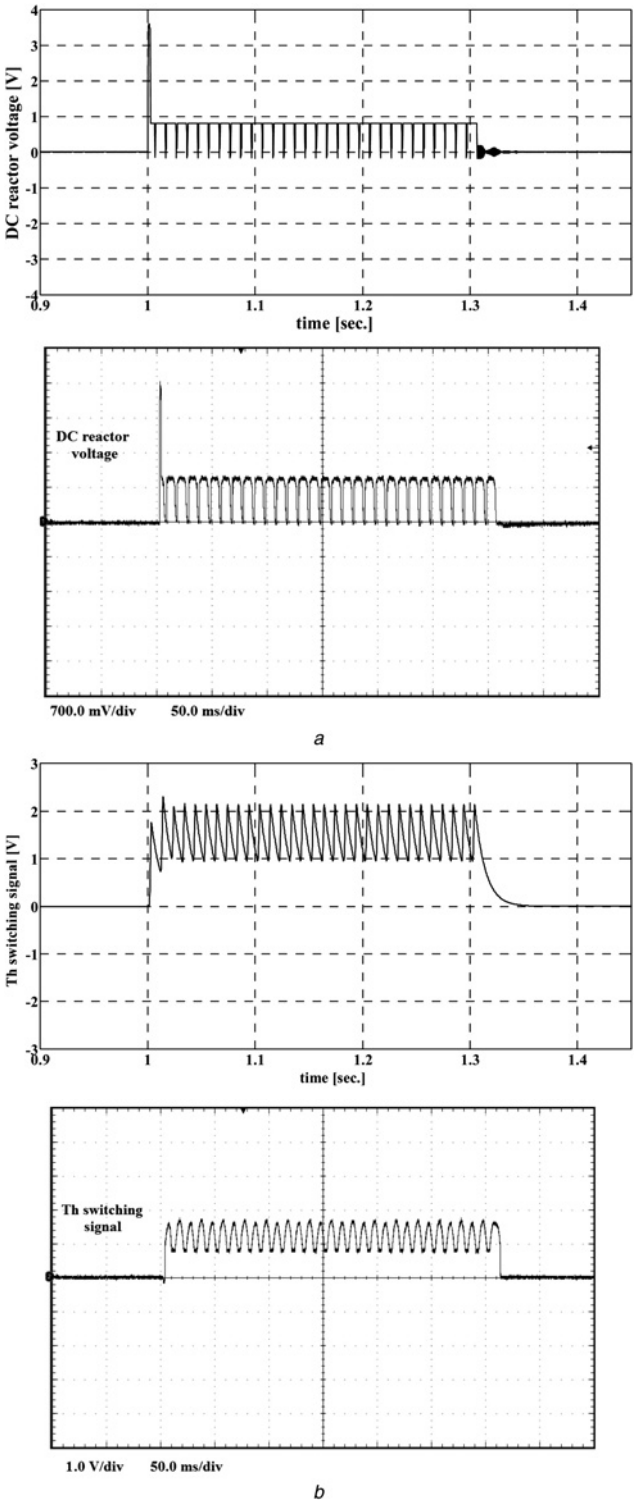

Fig. 6 *Simulation and experimental results of*
a DC reactor voltage
b Th switching signal

full-wave rectified current of the circuit. Operation voltage of MOV_1 is considered as 600 V in order to clamp transient overvoltage of the capacitor switching. Reverse voltage of D_1–D_4 is equal to maximum supply voltage. Average rectified forward current of the diodes is selected considering nominal current of the capacitor bank. Non-repetitive peak forward surge current of the diodes is chosen based on maximum inrush current. All of the components of control section are low-power elements. Turn ratio of the transformer T is selected such that the required triggering voltage in the primary side is achieved in 90% of the capacitor bank nominal voltage.

4 Simulation and experimental results

To verify capability of the proposed SSCSTL a 3 kVAR, 240 μF, 220 V single-phase capacitor bank is considered. The circuit shown in Fig. 1 is simulated in electromagnetic transient program software and its test bench is

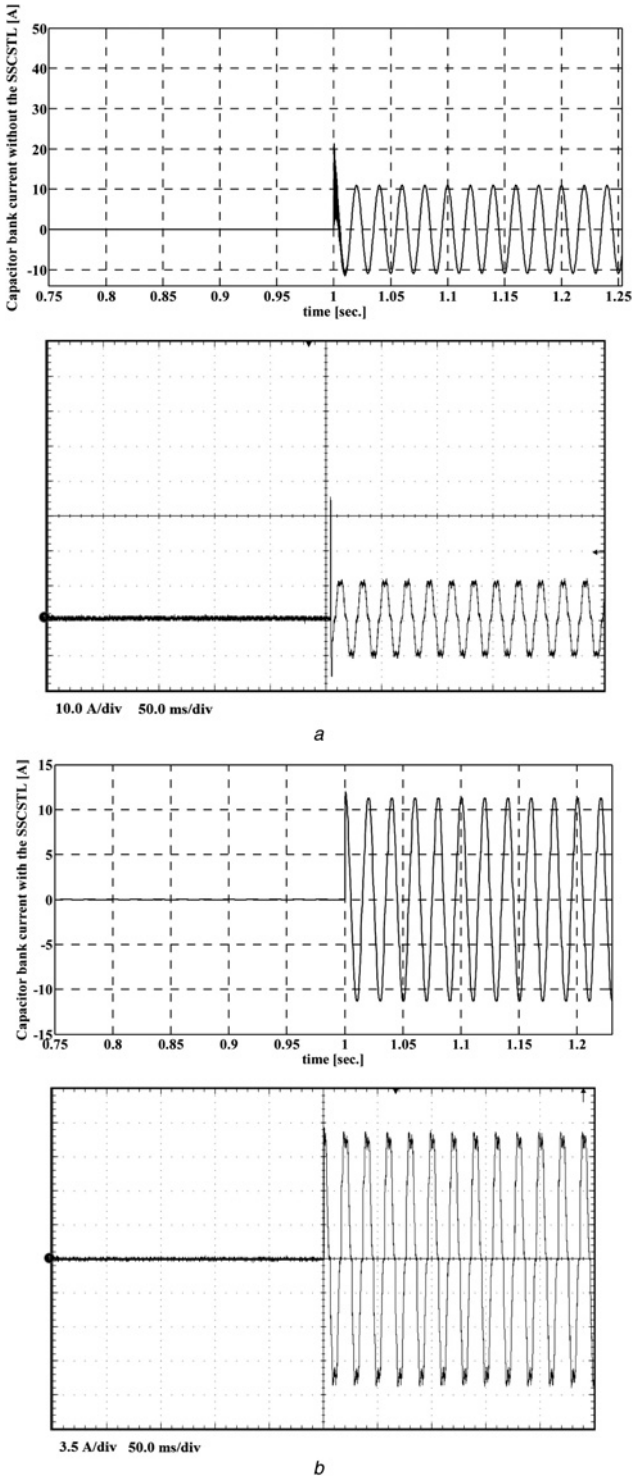

Fig. 7 *Simulation and experimental results of capacitor bank switching for the 120 μF stage*

a Without the SSCSTL
b With the SSCSTL

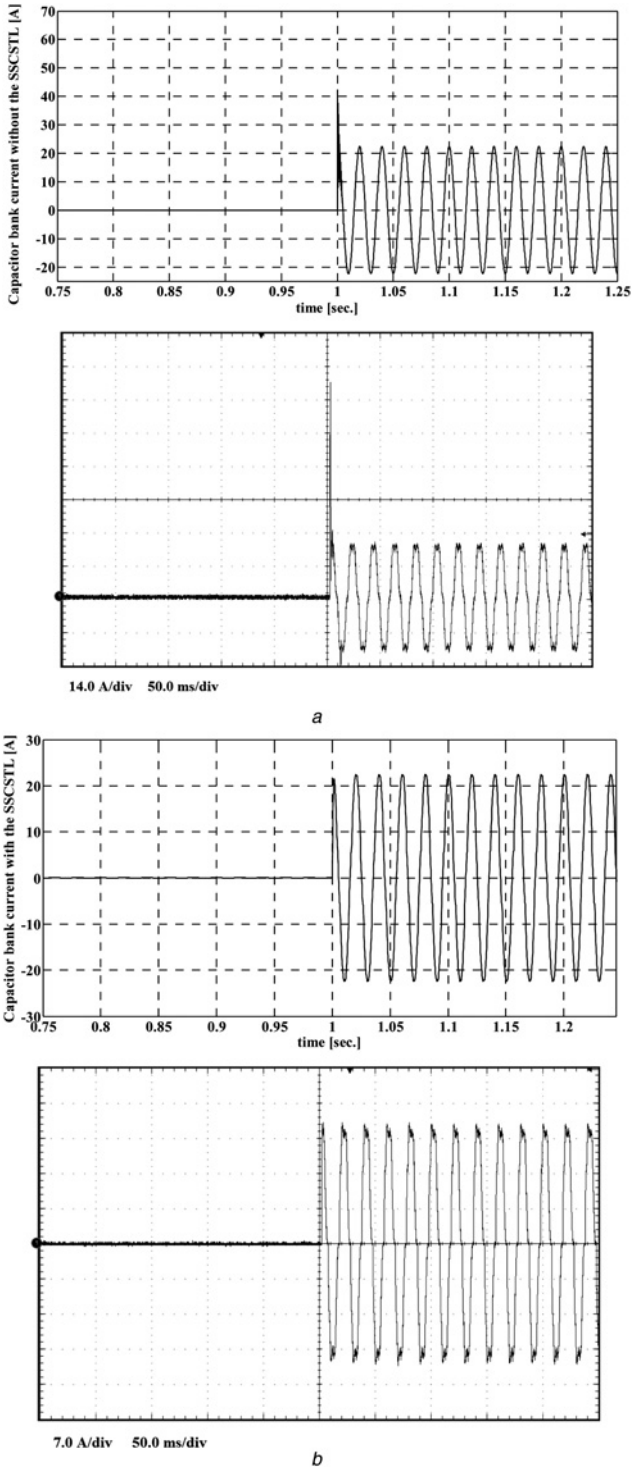

Fig. 8 *Simulation and experimental results of capacitor bank switching for the 240 μF stage*

a Without the SSCSTL
b With the SSCSTL

implemented in the laboratory. The circuit parameters are tabulated in Table 1. The capacitor bank includes two 120 μF stages. Simulation and experiment results show that maximum inrush current in 120 and 240 μF stages is about 35 and 90 A, respectively. It is expected that the inrush currents be suppressed to 12 and 22 A. Based on (8), the required DC inductors for the SSCSTL are about 10 and 3 mH, respectively. Of course, in (8) the circuit's resistances are neglected, although they help to suppress the inrush current. So, the restrictions will be achieved by smaller inductors in practice. Fig. 4 shows a laboratory test bench for a prototype of the SSCSTL. Transient current of the capacitor is measured using a digital oscilloscope (Tektronix MSO5054) in capacitor switching. Components values of the prototype single-phase SSCSTL and the circuit parameters are tabulated in Table 1.

Figs. 5 and 6 show the waveforms related to different parts of the circuit in the mentioned two modes. In Fig. 5,

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simulation and experimental results related to voltage of MOV_1 and current of the capacitor are presented. As shown in this figure, switching transient overvoltage and inrush current are suppressed at switching the capacitor bank.

In Fig. 6, the simulation and experimental results related to voltage of DC reactor voltage and switching signal of Th are presented. It can be seen that the DC reactor conducts the capacitor bank current only in a short moment. After that the switching triggering signal reaches a sufficient level to drive Th and bypasses the DC reactor. It can be observed that the simulation results agree well with the measured ones.

In Fig. 7, simulation and test results of the inrush current related to switching of the 120 μF stage are shown with and without the SSCSTL. The capacitor bank is switched-on with and without the SSCSTL at identical incipient angles in different cases. Without the SSCSTL, peak of the inrush current in the experiment is 35 A, which is suppressed by the SSCSTL to 12 A. It is observed that inrush current is considerably limited by the proposed limiter.

Similar results shown in Fig. 7 are also presented in Fig. 8 for 240 μF stage. In this case, without the SSCSTL inrush current in the experiment is 90 A, which is perfectly limited by the SSCSTL.

As the DC limiting reactor and MOV are present in the circuit prior to capacitor switching, the limiting process is actually instantaneous. The time necessary to transfer the current from DC reactor to Th depends on the L and R values in (6) and regarding their values presented in Table 1, the bypassing mode lasts 1–20 ms.

5 Conclusion

An SSCSTL is proposed to suppress inrush current and transient overvoltage related to capacitor bank switching. A DC reactor and MOV varistor are utilised in order to limit the inrush current and suppress the overvoltage of the capacitor bank switching, respectively. In steady-state condition, the SSCSTL acts as short-circuit path and has no negative impact on the circuit.

Simple structure, minimum power loss in steady state, fast response and reliable operation are the main advantages of the SSCSTL. Experiments and simulations confirm that the proposed SSCSTL is an efficient transient limiter for switching of the capacitor banks.

6 References

1 Miller, T.J.E.: 'Reactive power control in electric system' (John Wiley and Sons, Inc. Press, 1982), pp. 204–214
2 Das, J.C.: 'Analysis and control of large-shunt-capacitor-bank switching transients', *IEEE Trans. Ind. Appl.*, 2005, **41**, (6), pp. 1444–1451
3 IEEE Standard 18–1992: 'IEEE standard for shunt power capacitors', 2002
4 IEEE Standard 1036–1992: 'IEEE guide for application of shunt power capacitors', 1993
5 Bhargava, B., Khan, A.H., Imece, A.F., DiPietro, J.: 'Effectiveness of pre-insertion inductors for mitigating remote overvoltages due to shunt capacitor energization', *IEEE Trans. Power Deliv.*, 1993, **8**, (3), pp. 1226–1238
6 Abdulsalam, S.G., Xu, W.: 'Sequential phase energisation technique for capacitor switching transient reduction', *IET Gener. Transm. Distrib.*, 2007, **1**, (4), pp. 596–602
7 Alexander, R.W.: 'Synchronous closing control for shunt capacitors', *IEEE Trans. Power Appl. Syst.*, 1985, **PAS-104**, (9), pp. 2619–2626
8 Liu, K.C., Chen, N.: 'Voltage-peak synchronous closing control for shunt capacitors', *IEE Proc. Gener. Transm. Distrib.*, 1998, **145**, (3), pp. 233–238
9 Tseng, S.-T., Chen Hagh, J.-F.: 'Capacitor energising transient limiter for mitigating capacitor switch-on transients', *IET Electr. Power Appl.*, 2011, **1**, (3), pp. 260–266
10 Tseng, S.-T., Chen Hagh, J.-F., Liang, T.-J.: 'Symmetrical structure transient limiter for suppression of capacitor switching transients', *IEEE Trans. Power Deliv.*, 2011, **26**, (4), pp. 2821–2828
11 Tseng, H.-T., Chen, J.-F.: 'Single-DC reactor-type transient limiter for reducing three-phase power capacitor switching transients', *IEEE Trans. Power Electron.*, 2012, **27**, (4), pp. 1745–1757
12 Wu, J.C., Jou, H.L., Wu, K.D., Shen, N.T.: 'Hybrid switch to suppress the inrush current of AC power capacitor', *IEEE Trans. Power Deliv.*, 2005, **20**, (1), pp. 506–511