A 12-bit 210-MS/s 5.3-mW Pipelined-SAR ADC with a Passive Residue Transfer Technique

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Abstract

A 210 MS/s dual-channel 12-bit analog-to-digital converter (ADC) employing a pipelined successive approximation (SAR) architecture is presented. The ADC is partitioned into 3 stages with passive residue transferring between the 1st and the 2nd stages and active residue amplification between the 2nd and the 3rd stages. The ADC consumes 5.3 mW from a 1-V supply and achieves an SNDR of 63.48 dB at a 5-MHz input and 60.1 dB near Nyquist-rate.

Introduction

The demand on low-power, high-speed, and high-resolution ADCs has increased as many applications require wider signal bandwidth recently. To satisfy the specifications, pipelined ADCs [1] are typically used for their superior speed. On the other hand, with the scaling down of CMOS technologies, SAR ADCs have been replacing pipelined ADCs because of their excellent power efficiency. But the performance of SAR ADCs is limited due to comparator noise and the serial bit-cycling conversion.

This work employs a pipelined-SAR [2]-[4] architecture to enhance the throughput as well as to relax the design requirement of the comparator. To minimize the number of the power-hunger op amps along the signal path, conventional pipelined-SAR ADCs usually adopt a 2-stage scheme which requires only one op amp for residue amplification. A passive residue transferring method is proposed in this work to extend the pipelined operation from 2 to 3 stages while retaining the power efficiency. Besides, three comparators are rotated among the stages to ease the offset design constrain.

Architecture and Circuit Implementation

Fig. 1 shows the proposed ADC architecture. The ADC is configured as 3 stages and each stage resolves 4 bits, 5 bits, and 6 bits respectively to generate a 12-bit output. The extra one bit resolved by the last stage is used for the gain calibration.

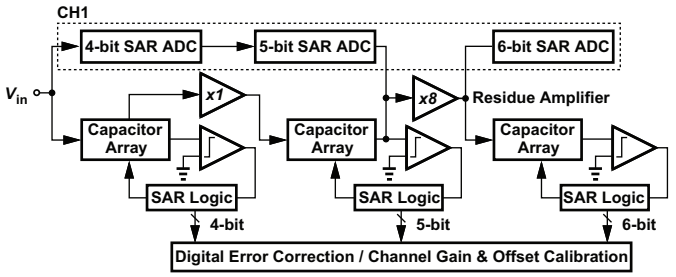

Fig. 1 ADC architecture

At the end of 1st stage A/D conversion, the DAC generates the corresponding residue which then be transferred to the 2nd stage passively. An 8x residue amplifier (RA) shared between channels is placed between the 2nd and the 3rd stages to alleviate backend noise and offset requirements.

For a conventional SAR ADC, the capacitor-DAC (CDAC) is always reset when it finishes conversion. If the charge stored on the CDAC could be reused, considerable power for residue generation can be saved. The idea of passive residue transferring is illustrated in Fig. 2.

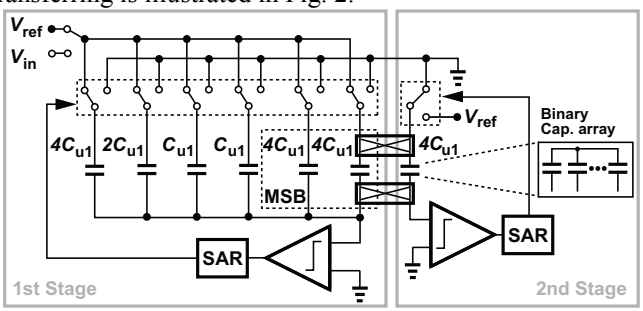

Fig. 2 Passive residue transferring

Considering a conventional bottom-plate sampling 4-bit SAR ADC as the 1st stage, the capacitor ratio for the binary D/A is 8:4:2:1:1 as shown. Once the conversion is done, the residue is stored on these capacitors. Thus, one of the capacitors could be moved to the 2nd stage for the following SAR process. On the other hand, the rest of capacitors are kept in the 1st stage for the next incoming sample. In this design, two half of the MSB capacitors, $4C_{u1}$, are served for the residue transferring to meet the kT/C noise requirement. When one $4C_{u1}$ moves the residue from the 1st to the 2nd stage, the other one is switched back to the 1st stage correspondingly. This ping-pong operation enables the residue transferring without any active components. Together with the switches via the proposed method, the ADC with the gain error induced by nonlinear parasitic capacitance still achieves about a 13-bit accuracy according to simulation. In addition, DAC settling time becomes the main speed bottleneck in the 1st stage because of the relatively large capacitance. A simple solution [5] employs redundant capacitors and decision cycles to tolerate DAC settling error with the penalty of the extra input capacitance and dynamic range overhead. To resolve the design issues, as shown in the Fig. 3, the first three MSB capacitors are split and an extra cycle is added for 2.8-bit implementation during the 4-bit conversion in the 1st stage, where large settling errors typically occur in the first and the second DAC switching. Similar to a 2.8-bit stage of a pipelined ADC, the error tolerance is $\pm V_{ref}/8$. In this work, the scheme accommodates the incomplete DAC settling and the comparator noise.

The offset of comparators in different stages also imposes potential linearity issue. Traditionally, the offset problem is simply solved by adding redundancy between stages. Despite of the one-bit redundancy, the tolerance is not enough because

the input of the 2nd and 3rd stages is not amplified to the full scale for power saving. A comparator rotation scheme is proposed in Fig. 4. Utilizing the same comparator from the 1st to the 3rd stages makes the signal experience the equal offset through every comparison. Because this rotation technique translates the comparator offset to the sample-to-sample offset that could be cancelled by channel offset calibration, the offset requirement of the comparators can greatly be relaxed from 3 mV to 100 mV.

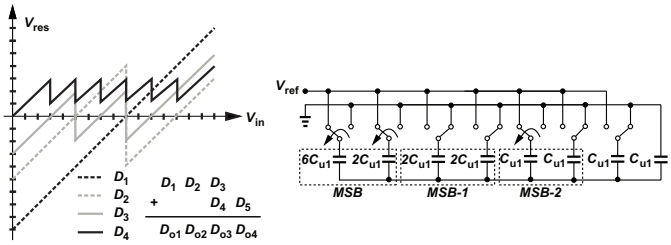

Fig. 3 Embedded 2.8-bit conversion

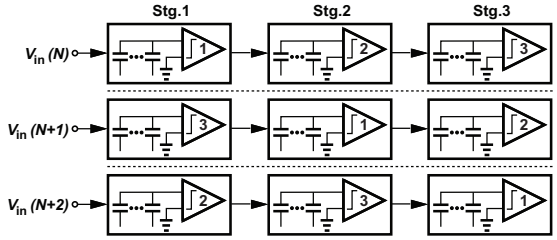

Fig. 4 Comparator rotation scheme

In order not to be noise-limited in the 3rd stage, the residue generated by the 2nd stage is amplified through an 8x RA. The op amp is implemented as a gain-boosted telescopic structure with an NMOS input and has a minimum gain of 65 dB to suppress the memory effect caused by channel sharing. The 3rd stage ADC is designed as a top-plate sampling, set-and-down architecture [5].

Experimental Results

The proposed ADC has been fabricated in a 65-nm CMOS technology which occupies 0.48 mm^2. The ADC accepts a full-scale differential signal of 1.6-Vpp with a 2-pF input capacitance. The digital calibration is performed off-chip for both gain error and offset. The chip micrograph is shown in Fig. 5. As shown in Fig. 6, the measured DNL and INL are within +0.66/-0.57 LSB and +1.45/-0.68 LSB.

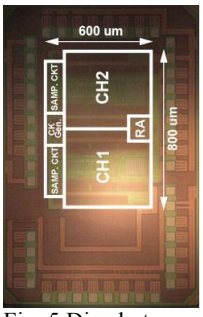

Fig. 5 Die photo

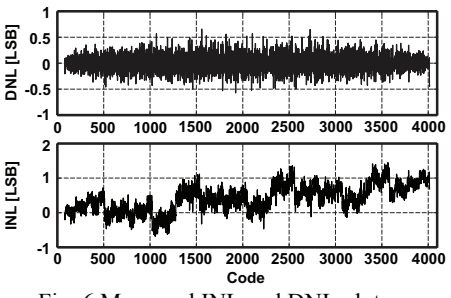

Fig. 6 Measured INL and DNL plots

Fig. 7 shows the measured dynamic performance at 210 MS/s. The results indicate an SNDR of 63.48 dB and an SFDR of 77.5 dB with a 5-MHz input. With a Nyquist-rate input, the SNDR is 60.1 dB and SFDR is 74.8 dB. Fig. 8 summarized the dynamic performance versus input frequency. Table 1 summarizes the performance of the proposed ADC and shows the comparison with the other 12-bit, high-speed ADCs. This work achieves a low FoM of 30.3 fJ/Conversion-step while operating at 210 MS/s.

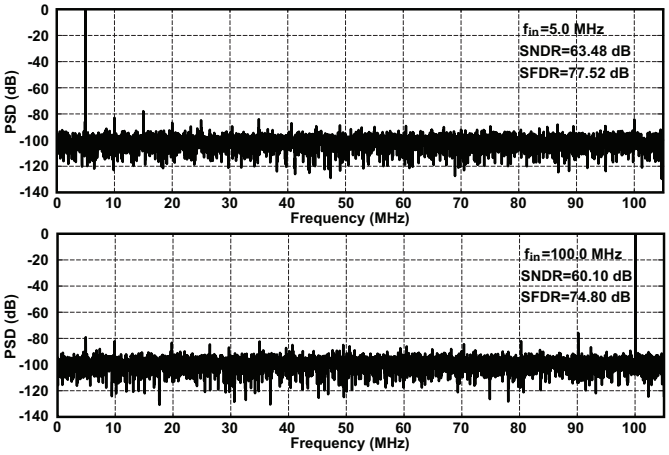

Fig. 7 Measured FFT plots

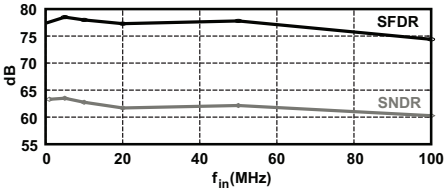

Fig. 8 Dynamic performance versus input frequency

Table 1. Performance summary and comparision table

	This work	[1]	[2]	[3]
Architecture	Pipelined-SAR	Pipelined	Pipelined-SAR	Pipelined-SAR
Technology	65-nm CMOS	65-nm CMOS	65-nm CMOS	65-nm CMOS
VDD	1.0 V	1.0 V	1.3 V	1.2 V
Resolution	12-bit	12-bit	12-bit	12-bit
Speed	210 MS/s	200 MS/s	50 MS/s	110 MS/s
SNDR	63.48 dB	65.0 dB	65.5 dB	63.0 dB
DNL / INL	0.66/1.45 LSB	1.0/1.25 LSB	0.75/1.5 LSB	0.42/1.63 LSB
Power	5.3 mW	11.5 mW	3.5 mW	13.3 mW
FoM	30.3 fJ/Conv.	93.1 fJ/Conv.	52.0 fJ/Conv.	131 fJ/Conv.

Acknowledgement

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References

[1] N. Dolev, M. Kramer, and B. Murmann "A 12-bit, 200-MS/s, 11.5-mW Pipeline ADC using Pulsed Bucket Brigade Front-End," in *Proc. VLSI Circuits Symp.*, Jun. 2013, pp. 98-99.

[2] C. C. Lee and M. Flynn, "A 12b 50MS/s 3.5mW SAR Assisted 2-Stage Pipeline ADC," in *Proc. VLSI Circuits Symp.*, Jun. 2010, pp. 239-240.

[3] R. Wang, U.-F. Chio, S.-W. Sin, S.-P. U, Z.-H. Wang, and R. P. Martins "A 12-bit 110MS/s 4-stage Single-Opamp Pipelined SAR ADC with Ratio-Based GEC Technique," in *Proc. IEEE ESSCIRC*, Sep. 2012, pp. 265-268.

[4] Y.-D. Jeon, Y.-K. Cho, J.-W. Nam, K.-D. Kim, W.-Y. Lee, K.-T. Hong, and J.-K. Kwon, "A 9.15mW 0.22mm^2 10b 204MS/s Pipelined SAR ADC in 65nm CMOS," in *IEEE CICC Dig. Tech. Papers*, Oct. 2010, pp. 1-4.

[5] C.-C. Liu, *et al*. "A 10b 100MS/s 1.13mW SAR ADC with binary scaled error compensation," in *IEEE ISSCC Dig. Tech. Papers*, pp.386-387, Feb. 2010.