Split ADC Based Fully Deterministic Multistage Calibration for High Speed Pipeline ADCs

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***Abstract*—A fully deterministic digital background calibration for pipeline ADCs is presented. The proposed approach is based on split ADC concept to give the shortest background calibration time with high accuracy. A slope mismatch averaging technique is employed in a multistage calibration scheme to deterministically detect the circuit errors without any iterative operations or feedback loops, which render it fast and accurate. Analysis and behavioral simulations for the developed multistage calibration demonstrate the efficiency of this technique and its merit over the LMS-based techniques. Practical considerations have been considered and the proposed calibration has been applied on a 200 MS/s 40 nm CMOS split pipeline ADC to correct for the capacitor mismatch and the amplifier finite gain. The post-layout simulation results show a very fast calibration cycle, where the ADC achieves more than 11 ENOB in less than 1600 clock cycles.**

***Index Terms*—Analog digital conversion, calibration time, CMOS, digital calibration, digitally assisted analog, pipeline converter, split ADC.**

I. Introduction

HIGH performance analog-to-digital converters are needed to push the digital processing as close as possible to the RF input in wideband communication systems. This enables higher flexibility and higher integration level with better power efficiency [1]. For high resolution and high speed applications, the pipeline ADC represents the most suitable architecture, and it is shown in Fig. 1 for a 12-bit ADC. It is a multi-step amplitude quantizer in which digitization is performed by pipelining a number of similar or identical stages of low-resolution analog-to-digital encoders called the analog-to-digital sub-converter (ADSC). The ADSC output of each pipelined stage is processed with its input signal by the multiplying digital to analog converter (MDAC), which combines the digital-to-analog sub-converter (DASC), signal subtraction and amplification in a single switched capacitor (SC) circuit. The precision of the MDAC depends on a high gain amplifier at the ADC required speed. Designing a fast settling high gain amplifier is becoming more complex and power inefficient with the technology advances, which reduce the transistor feature length for higher speed on the expense of lower analog performance and use lower supply voltages.

An efficient method to leverage the effective analog resolution at high speed using low gain amplifiers is to use digital calibration to correct for the analog circuit limitations [2]. This method conforms well with technology trend in which digital processing is becoming faster and more power efficient. Digital calibration can be done by interrupting the ADC normal operation in the foreground, or it can be run in the background during the normal conversion of the ADC. Background calibration ensures a seamless ADC operation and tracks performance deviation across temperature variations, which render the calibration robust and effective. Among different background calibration techniques, split ADC calibration has been introduced in [3] and evolved as a promising and practical technique to calibrate high speed ADCs. Unlike other techniques [4]–[6], split ADC calibration preserves the dynamic range of the input signal, provides robust error measurement and correction, and performs the calibration cycle in a much less time. An interesting split ADC technique is presented in [7], which performs a rapid calibration of MDAC errors. This technique is further developed in [8], which gives more accurate and faster calibration using slope mismatch averaging (*SMA*) to correct for amplifier finite gain and sampling capacitor mismatch.

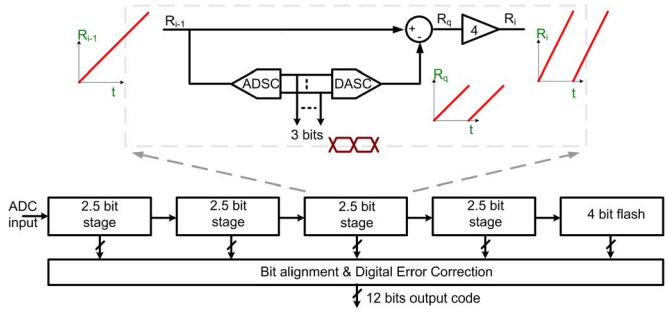

Fig. 1. 12-bit pipeline ADC.

This work aims at extending the *SMA* technique in split ADC for multistage calibration, and considering its practical limits by analysis, simulations and applying it on a 40 nm pipeline ADC. Section II presents an overview on the split ADC calibration. Section III discusses and analyses the split ADC deterministic digital calibration. Section IV introduces the developed background calibration scheme. Section V presents the practical considerations of the proposed technique and finally Section VI concludes the achieved results.

II. Split ADC Calibration: Concept and Overview

The split ADC calibration provides a reference for error detection by splitting the single channel ADC into two halves as shown in Fig. 2. Each one of the two halves uses half the sampling capacitances C_s and half the amplifier transconductance g_m of the original single channel ADC, thus the split ADC preserves nearly the same power and area. The background calibration is then performed in the digital domain using the digital outputs of both split ADC channels D_{oa} and D_{ob}. The difference between the two channel outputs is used for error detection which feeds the error correction block for each ADC channel with the corresponding correction parameters. The calibrated

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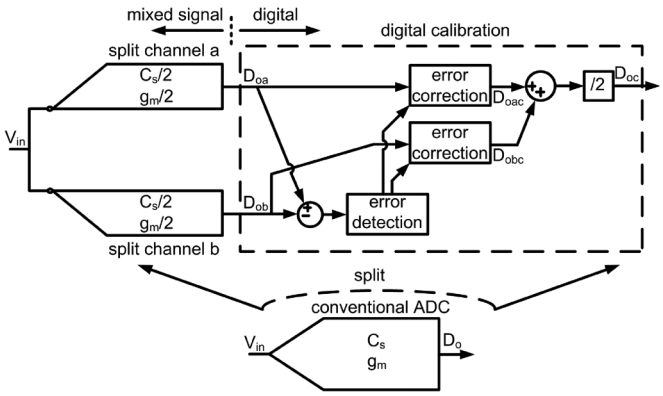

Fig. 2. Split ADC background calibration concept.

outputs of both channels D_{oac} and D_{obc} are then averaged to recover the final calibrated output of the ADC D_{oc}.

In [9] and [10], non-deterministic split ADC calibration approaches are used with multiple residue modes in the calibrated split ADC stage to provide a robust error detection. The multiple residue modes used in these techniques imply the use of lower gain in the pipelined stage to account for over-range due to comparator threshold offsets. This lower gain stage means that more stages will be needed to provide the required ADC accuracy. Also, the correction is performed by updating certain calibration parameters through an adaptive loop using LMS (Least Mean Square algorithm), which necessitates extra time for loop convergence. In [7], the split ADC calibration is considered for a pipeline ADC by shifting the residue characteristics of each calibrated split ADC half with respect to the other one, and direct error estimation for finite amplifier gain and capacitor mismatch is done by taking the difference of the two split channel outputs. However, in order to do this, a LMS loop has been used to correct the gain error mismatch between the two split ADC halves, which affects the accuracy of error estimation and increases the calibration time. The LMS loop should converge at a much slower rate than the calibration algorithm for correct operation, which adds constraints when using this technique. Also this technique as presented in [7] is not suitable for multistage calibration, which implies the use of higher resolution first stage to decrease the input-referred errors of the uncalibrated backend ADC (BE ADC). The use of higher resolution pipelined stage limits the maximum speed of the converter and puts stringent requirement on the comparator offsets of the ADSC.

III. Multistage Split ADC Calibration: Operation and Analysis

To alleviate the limitations of previous split ADC work mentioned in Section II, we propose the extension of (*SMA*) technique to multistage calibration. By analyzing the split ADC operation for multistage, a fully deterministic approach has been considered. This deterministic approach means that the error detection and correction have been done without any approximate calculations or estimators, and thus makes the calibration very accurate and fast, depending on the ADC noise-level and digital post-processing optimization requirements. The analysis and its conclusion is presented in this section, and the following section will discuss the proposed multistage calibration scheme.

Circuit error detection in split pipeline ADC can be performed directly by using shifted residues in the calibrated stage [7]. This circuit error, which is caused by amplifier finite gain and capacitor mismatch, appears at the decision thresholds of each residue where the references are subtracted or added. This

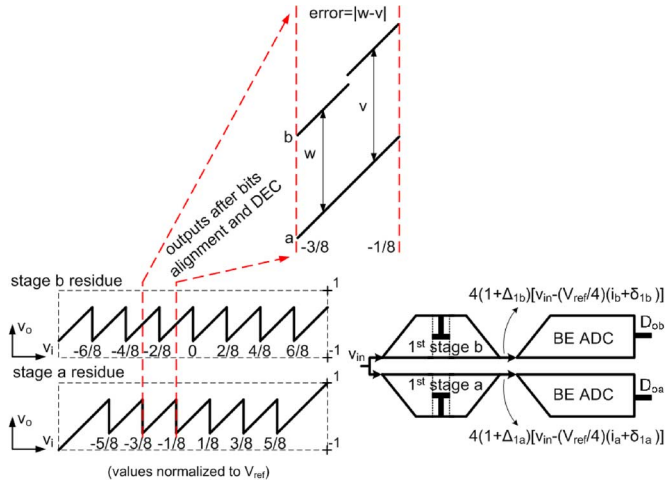

Fig. 3. Error detection concept in split ADC calibration for 2.5-bit stages (Δ is the gain error due to the finite DC gain of the amplifier, and δ_i is the error due to the unit sampling capacitor mismatch).

is illustrated in Fig. 3 for 2.5-bit split stage. The shift in the residue characteristics between the two split channels allows using each channel as a reference to the other. The transition in the residue of the calibrated stage in one channel from certain segment to the following one can be referred to the same linear residue segment in the other channel. The corresponding error to this segment transition can be directly detected by performing a difference of the difference operation between the two split channel outputs $|w - v|$, as shown in the figure. The output raw bits of each split pipelined stage are used as an index to the corresponding segment of the stage output residue to perform error detection and correction in the background.

Fig. 4 shows the SC MDACs with shifted residue characteristics for the 2.5-bit pipelined stages. The outputs of the 2.5-bit SC MDAC and its shifted version can be given by these equations respectively:

$$v_o = \left(v_{in}\frac{C_1+C_2+C_3+C_{4f}}{C_{4f}} - \left(i+\frac{\Delta C_i}{C_{4f}}\right)V_{ref}\right) \times \frac{1}{1+\frac{1}{A_{dc}}\frac{C_1+C_2+C_3+C_{4f}}{C_{4f}}} \quad (1)$$

and

$$v_o = \left(v_{in}\frac{C_1+C_2+C_3+C_{4f}}{C_{4f}} - \left(i+\frac{\Delta C_i}{C_{4f}}\right)V_{ref}\right) \times \frac{1}{1+\frac{1}{A_{dc}}\frac{C_1+C_2+C_3+C_{4f}+\frac{C_0}{2}}{C_{4f}}} \quad (2)$$

where $C_{0,1,2,3,4f} = C_u$ are the unit sampling capacitors, ΔC_i is the mismatch of the unit sampling capacitor, A_{dc} is the finite DC gain of the amplifier, $i \in \{[-3,3],[-3.5,3.5]\}$ determines the output residue segment and depends on the input signal level, and V_{ref} is the reference voltage of the ADC. Both (1) and (2) can be put as:

$$v_o = 4(1+\Delta)\left[v_{in} - \frac{V_{ref}}{4}(i+\delta_i)\right] \quad (3)$$

where Δ is the gain error mainly due to the finite DC gain of the amplifier, and δ_i is the error mainly due to the unit sampling capacitor mismatch. The gain error Δ is the same for all the residue segments, while the unit capacitor mismatch error δ_i varies from one segment to another in the residue characteristics. The error corresponding to each segment transition in the

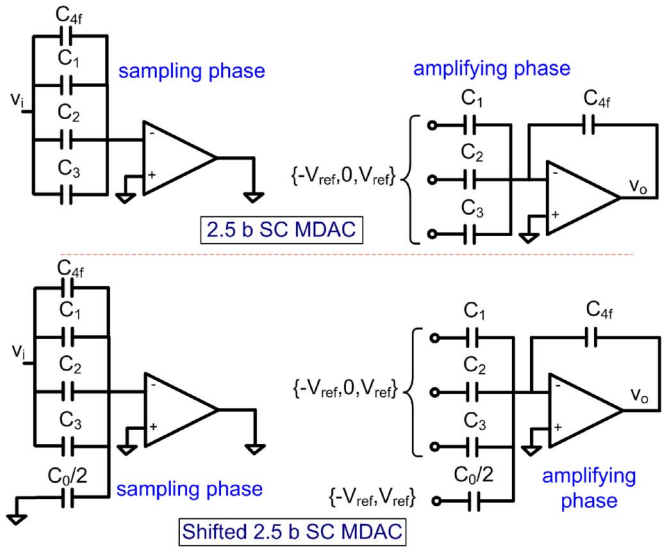

Fig. 4. SC implementations for two residue modes.

residue of a certain ADC channel can be computed using (3) to represent the split stage residues, and will be calculated hereafter for the transition from the 3rd segment to the 4th segment for the residue of the first 2.5-bit split stage of channel b, as depicted in Fig. 3. The digital representation of (3) can be given by:

$$D = 4(1+\Delta)\left[\frac{v_{in}}{V_{ref}} - \frac{1}{4}(i+\delta_i)\right] \tag{4}$$

Consider channel b BE ADC digital output for an input signal level v_{in1} corresponding to the 3rd segment of the stage residue:

$$D_{1b,1} = 4(1+\Delta_{1b})\left[\frac{v_{in1}}{V_{ref}} + \frac{\frac{3}{2}+\delta_{1b,-1.5}}{4}\right] \tag{5}$$

and the corresponding channel a BE ADC digital output for the same input:

$$D_{1a,1} = 4(1+\Delta_{1a})\left[\frac{v_{in1}}{V_{ref}} + \frac{1+\delta_{1a,-1}}{4}\right] \tag{6}$$

where $\delta_{1b,-1.5}$ is the unit sampling capacitor mismatch error for the residue segment -1.5 of the first stage in channel b, and $\delta_{1a,-1}$ is that for the residue segment -1 of the first stage in channel a. The digital output of the BE ADC of channel b for an input signal level v_{in2} corresponding to the 4th segment of the stage residue is:

$$D_{1b,2} = 4(1+\Delta_{1b})\left[\frac{v_{in2}}{V_{ref}} + \frac{\frac{1}{2}+\delta_{1b,-0.5}}{4}\right] \tag{7}$$

and the corresponding digital output of the *BE ADC* of channel a is:

$$D_{1a,2} = 4(1+\Delta_{1a})\left[\frac{v_{in2}}{V_{ref}} + \frac{1+\delta_{1a,-1}}{4}\right] \tag{8}$$

The digital difference of the difference $|w-v|$ should be ideally equal to 1, which corresponds to adding V_{ref} when the input signal level changes to correspond to the 4th segment from the 3rd segment in the residue characteristics in channel b. Due to gain error and capacitor mismatch, this difference deviates from the ideal value as shown in Fig. 3, and the error corresponding to the 4th segment of the channel b stage residue is given by:

$$e_{b3} = 1 - [(D_{1b,1} - D_{1a,1}) - (D_{1b,2} - D_{1a,2})] \tag{9}$$

Substituting (5), (6), (7), and (8) into (9):

$$\begin{aligned} e_{b3} =& 1 - 4(1+\Delta_{1b})\frac{v_{in1}}{V_{ref}} - (1+\Delta_{1b})\left(\frac{3}{2}+\delta_{1b,-1.5}\right) \\ &+ 4(1+\Delta_{1a})\frac{v_{in1}}{V_{ref}} + (1+\Delta_{1a})(1+\delta_{1a,-1}) \\ &+ 4(1+\Delta_{1b})\frac{v_{in2}}{V_{ref}} + (1+\Delta_{1b})\left(\frac{1}{2}+\delta_{1b,-0.5}\right) \\ &- 4(1+\Delta_{1a})\frac{v_{in2}}{V_{ref}} - (1+\Delta_{1a})(1+\delta_{1a,-1}) \end{aligned} \tag{10}$$

Equation (10) shows that the gain error mismatch between the two split ADC channels should be zero to completely cancel the input signal from the error calculations, i.e., $\Delta_{1b} = \Delta_{1a}$. The gain error mismatch between the channels is minimized in [7] by using a LMS adaptive algorithm. Once the gains are matched, the error corresponding to the 4th segment of the stage residue in channel b will be input-independent and (10) becomes:

$$e_{b3} = 1 - (1+\Delta_{1b})(1+\delta_{1b,-1.5} - \delta_{1b,-0.5}) \tag{11}$$

For deterministic *multistage* calibration, the errors of the first stage will affect the error detection process of the subsequent calibrated stages, and thus analysis and modified procedures are needed to perform accurate multistage calibration. Considering the calibration of the second pipelined stage in the ADC, and due to the difference in the output residues of the 1st split stages, inputs to both 2nd split stages are not the same as shown in Fig. 3. Output residues of the 1st split stages a and b are respectively given by:

$$res_{1a} = 4(1+\Delta_{1a})\left[v_{in} - \frac{V_{ref}}{4}(i_{1a}+\delta_{1a})\right] \tag{12}$$

and

$$res_{1b} = 4(1+\Delta_{1b})\left[v_{in} - \frac{V_{ref}}{4}(i_{1b}+\delta_{1b})\right] \tag{13}$$

Using (12) and (13), and following the same procedure as in the calculation of the error for the first split stages, the error corresponding to the 4th segment of the 2nd stage residue in channel b is given by:

$$\begin{aligned} e_{b3,2} =& 1 - 4(1+\Delta_{2b})\frac{4(1+\Delta_{1b})\left[v_{in1} - \frac{V_{ref}}{4}(i_{1b,1}+\delta_{1b,1})\right]}{V_{ref}} \\ &- (1+\Delta_{2b})\left(\frac{3}{2}+\delta_{2b,-1.5}\right) \\ &+ 4(1+\Delta_{2a})\frac{4(1+\Delta_{1a})\left[v_{in1} - \frac{V_{ref}}{4}(i_{1a,1}+\delta_{1a,1})\right]}{V_{ref}} \\ &+ (1+\Delta_{2a})(1+\delta_{2a,-1}) \\ &+ 4(1+\Delta_{2b})\frac{4(1+\Delta_{1b})\left[v_{in2} - \frac{V_{ref}}{4}(i_{1b,2}+\delta_{1b,2})\right]}{V_{ref}} \\ &+ (1+\Delta_{2b})\left(\frac{1}{2}+\delta_{2b,-0.5}\right) \\ &- 4(1+\Delta_{2a})\frac{4(1+\Delta_{1a})\left[v_{in2} - \frac{V_{ref}}{4}(i_{1a,2}+\delta_{1a,2})\right]}{V_{ref}} \\ &- (1+\Delta_{2a})(1+\delta_{2a,-1}) \end{aligned} \tag{14}$$

from (14), we can deduce the following for the 2nd stage calibration:

- *LMS accuracy issue*: Gain error mismatch due to the 1st and 2nd split stages should be zero to cancel the input

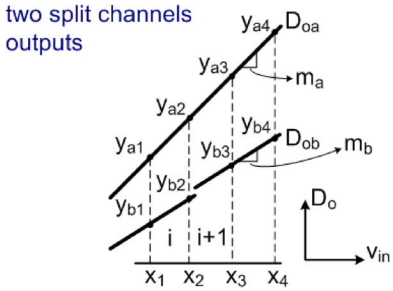

Fig. 5. SMA concept (illustrated for residue segments i and $i+1$).

signal from error calculations, i.e., $(1+\Delta_{1b})(1+\Delta_{2b}) = (1+\Delta_{1a})(1+\Delta_{2a})$. As we infer from (10) for 1st stage calibration, the condition $(1+\Delta_{1b}) = (1+\Delta_{1a})$ should be realized for the same reason. Using LMS adaptive algorithm as in [7] will settle the correction parameter of the gain error mismatch on *average* between the two conditions. This translates to an accuracy issue when directly estimating the errors.

- *Multistage calibration issue*: The calibration outputs needed to estimate the error which corresponds to a certain residue segment for the 2nd stage calibration should lie on the same segment of the 1st split stage residues, to cancel out any errors from these stages in 2nd stage error calculations, i.e., $(i_{1b,1}+\delta_{1b,1}) = (i_{1b,2}+\delta_{1b,2})$ and $(i_{1a,1}+\delta_{1a,1}) = (i_{1a,2}+\delta_{1a,2})$.

When the conditions mentioned above are achieved, the error corresponding to the 4th segment of the 2nd stage residue in channel b is given by:

$$e_{b3,2} = 1-(1+\Delta_{2b})(1+\delta_{2b,-1.5}-\delta_{2b,-0.5}) \tag{15}$$

which is similar to the 1st stage error for the corresponding segment. The error calculations for other segments transitions and for both channels can be derived using the same approach.

IV. Fully Deterministic Split ADC Calibration

Based on the analysis and conclusions of Section III, a fully deterministic multistage calibration is proposed. This calibration scheme depends on an algorithm that uses the *SMA* technique with a programmable two-mode residue in the first pipelined stage. The elements and procedures of the calibration are discussed hereafter.

A. Slope Mismatch Averaging

SMA technique takes the gain error mismatch between the two split channels into account in the residue segment error estimation. It provides accurate error estimation by detecting the *local* gain error mismatch between the residue segments of the split stage, and accounts for it in the circuit error correction of the pipelined stage, without physically correcting this gain error mismatch between the two split channels in the hardware. This alleviates the limitation of LMS discussed in Section III. The slope mismatch averaging (*SMA*) concept is illustrated in Fig. 5, where the digital outputs $y_{a1}\cdots y_{a4}$ and $y_{b1}\cdots y_{b4}$ of the two split ADC channels D_{oa} and D_{ob} are shown for the calibration of a specific segment $i+1$ in the MDAC residue of ADC channel b.

Using the raw bits of the 1st split stages, two calibration outputs are detected in the background for each segment of the calibrated stage residue of ADC channel b, along with the corresponding outputs of ADC channel a as illustrated in the figure. The slopes of the residue segments of both split ADC channels, m_a and m_b, are then calculated and the gain error mismatch correction parameter for all segments of the residue is given by the average [8]:

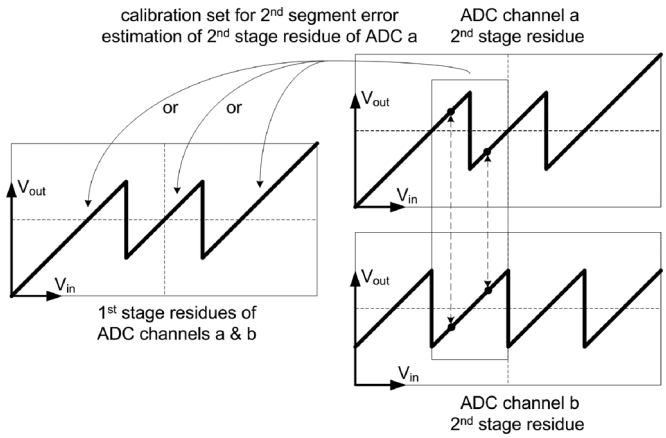

Fig. 6. The concept of the error detection algorithm for 2nd stage calibration.

$$m_{\frac{b}{a}} = \overline{\left\{\frac{m_{b,i}}{m_{a,i}}, \frac{m_{b,i+1}}{m_{a,i+1}}\right\}} \tag{16}$$

The error estimate corresponding to residue segment $i+1$ of channel b can be accurately given by the average:

$$e_{b,i+1} = \overline{\left\{\left(y_{b1}-y_{a1}\times m_{\frac{b}{a}}\right)-\left(y_{b3}-y_{a3}\times m_{\frac{b}{a}}\right), \left(y_{b2}-y_{a2}\times m_{\frac{b}{a}}\right)-\left(y_{b4}-y_{a4}\times m_{\frac{b}{a}}\right)\right\}} \tag{17}$$

As the error of segment $i+1$ is calculated, it can be subtracted from the ADC output to align this residue segment to the preceding segment i using the stage raw bits, which restores back the linearity of the ADC.

B. Deterministic Multistage Calibration

For a fully deterministic multistage calibration, a programmable two-mode residue is employed in the first split pipelined stage. This programmable residue alternates between the 2.5-bit residue and the shifted version of it shown in Fig. 3, depending on the mode control signal. These residue modes use the nominal pipelined stage gain, and thus avoid the need of extra quantization if lower gain stage is considered. These modes are used in a specific algorithm to exercise the decision thresholds of the 2nd pipelined stages, where the finite gain of the amplifier and capacitor mismatch errors appear, and to avoid the addition of the 1st stage imperfections in estimating the 2nd stage errors.

The concept of error detection algorithm in the 2nd stage is illustrated in Fig. 6 for the split ADC channel a. Both split channels in the first pipelined stage are configured in a 2.5-bit residue mode during the calibration of the 2nd split stage. To calibrate the 2nd pipelined stage, and by using the stages' raw bits, the calibrating digital outputs are detected in the background to estimate the error of a certain residue segment as presented in Section IV-A. These calibrating outputs are stored in a certain calibration set corresponding to the calibrated residue segment. To avoid the circuit errors in the 1st pipelined stages, the outputs stored in this calibration set are detected for the same linear residue segment in the 1st stage residues. This algorithm is repeated to all the residue segments of the 2nd stages of both split ADC channels a and b.

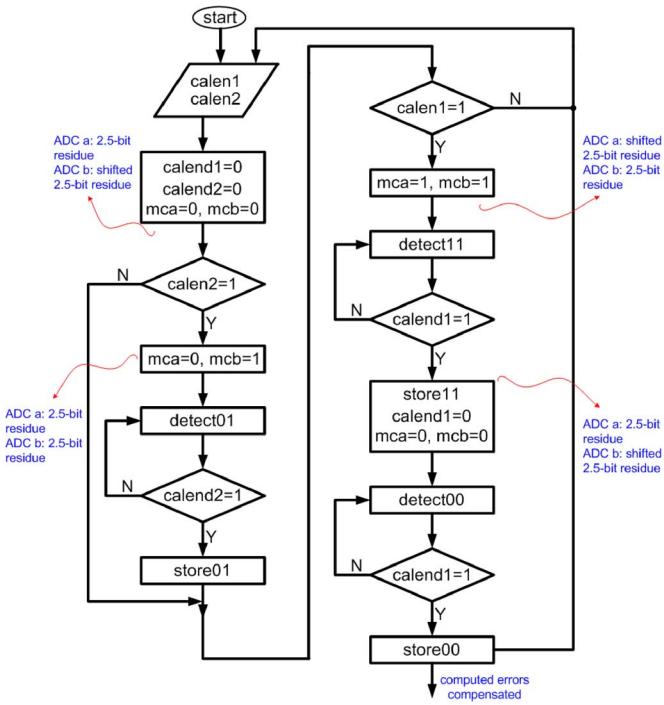

Fig. 7. Calibration procedure for two stage split ADC calibration.

C. Background Calibration Procedure

The calibration procedure can be summarized in the flowchart of Fig. 7. First the stage calibration enable flags, *calen1* for the 1st stages and *calen2* for the 2nd stages, are checked. The residue mode controls, *mca* and *mcb*, and the end-of-calibration cycle flags, *calend1* and *calend2*, are reset before the multistage calibration cycle. Second stage calibration can be skipped to the 1st stage calibration using the enable flag *calen2*. The calibration cycle for 2nd stage starts by setting the residue modes for the 1st stages to the 2.5-bit mode, using the mode controls *mca* and *mcb* for channels *a* and *b* respectively. The error detection algorithm for the 2nd stages *detect01* is performed till the calibration set containing the detected calibration outputs is completed and the end-of-calibration cycle flag *calend2* rises. Second stage errors are then stored for correction *store01* and the calibration enable flag for the 1st stages *calen1* is checked. Similarly, the 1st stage errors detection is performed for the residue modes when the mode control signals *mca* and *mcb* are both set to 1 and then set to 0, and the corresponding errors is stored for correction *store11* and *store00* respectively. These procedures are then repeated for a continuous background calibration.

In this work, two stage calibration has been considered, however the technique can be extended to more stages if required. This can be done by introducing a programmable two-mode residue in the stage preceding the one under calibration, and the same concept of calibration algorithm can be applied.

V. Practical Considerations and Simulation Results

A. Noise Effect on Calibration Accuracy

Usually digital calibration requires averaging certain number of samples to achieve certain calibration accuracy. A behavioral 13-bit split pipeline ADC is developed in MATLAB to examine the number of averaging required in the proposed calibration. The behavioral ADC is using low gain amplifiers in the first two stages, and the random comparator offsets are modelled in the ADSC. Thermal noise equivalent to 74 dB is inserted in the ADC. The SNDR before calibration is 48.3 dB.

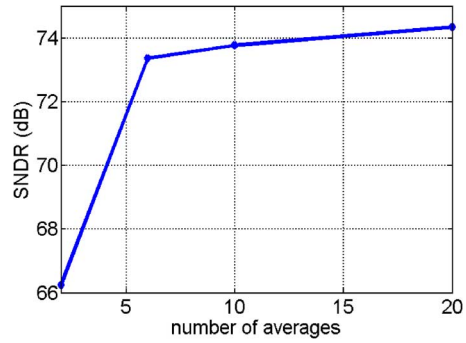

Fig. 8. Thermal noise effect on the calibration accuracy.

The SNDR after calibration is plotted in Fig. 8 with the number of samples averaged. With the aforementioned ADC noise-level, six averages are enough to restore the ADC SNDR to be almost as the SNR of ADC, limited by the thermal noise. The low number of averaging attributes to the fully deterministic approach of the proposed calibration, where the ADC linearity errors, represented by missing codes at the comparator decision levels, are being detected and corrected without any estimation or approximate methods.

The accuracy of deterministic detection and compensation of missing codes can be verified experimentally using the foreground equivalent to the proposed background technique. Lab. measurements were done on a 65 nm 11-bit pipeline ADC prototype, where the ADC is calibrated in the foreground by detecting and compensating the missing codes at the comparator decision levels, which is the same method of calibration that our proposed split ADC follows in the background. To do this, a slow clipped sine wave input that exercises all the ADC codes is used as the calibrating signal, which exercises the full scale of the ADC 6 times, and thus the calibration is done by averaging the detected errors 6 times.

Fig. 9 shows the ADC performance before and after calibration of the first two stages. Six averages were enough to restore the ADC total harmonic distortion (THD) from 58.2 dB to 72.7 dB, despite the imperfection of the backend ADC (appeared as spurs in the ADC output spectrum after calibration, mainly caused by capacitor mismatch in the backend stages). As the proposed split ADC calibration implements the same method of detecting and compensating the missing codes through a fully deterministic manner in the background, the number of required averages is very low to restore the linearity of the ADC, depending on the ADC noise-level.

B. Effect of Input Signal Characteristics on the Background Calibration

The background calibration depends on exercising the decision levels of the ADSC by the input signal, as shown in Fig. 10. Initially, a sufficiently busy input should be considered to exercise all the decision levels to rapidly calculate all the calibration parameters. The initial very fast calibration cycle would lessen the time spent in the automated tester for high volume production, and thus significantly decreases the overall cost. During normal background operation, the calibration parameter equivalent to a certain decision level could be updated so that linearity is restored rapidly even if the input is only exercising one decision level. If the input is small enough to exercise no decision level as shown in Fig. 10, no calibration is needed as the input

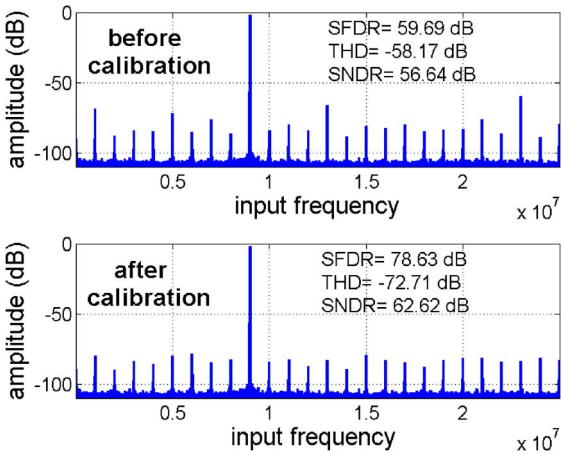

Fig. 9. 65 nm ADC measurements before and after the foreground calibration.

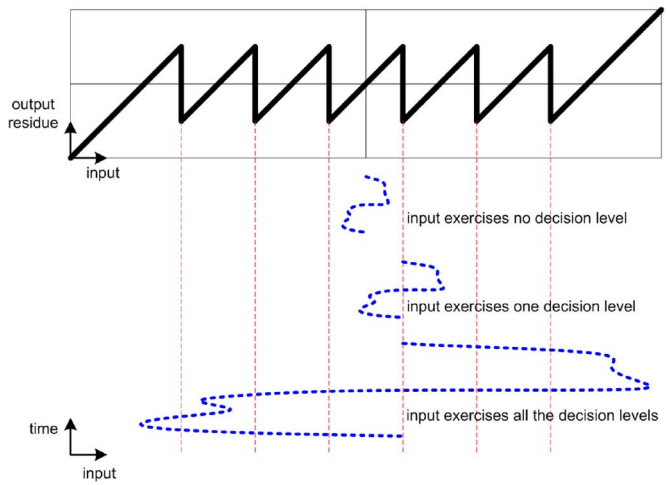

Fig. 10. Pipelined stage characteristics with inputs of different amplitudes.

is in the linear region of the ADC and doesn't experience the places of errors. To ensure a very fast calibration cycle to compensate the errors for all the decision levels independently of the input amplitude, the unit sampling capacitors can be rotated exchangeably in a non-correlated sequence with the input signal, as suggested in [7] (not implemented in this prototype).

The split ADC calibration for the first two pipelined stages is done in the behavioral MATLAB model with different input characteristics, and the calibration parameters update for the second and first stages are shown in Fig. 11 and Fig. 12, respectively. In each case, averaging is done 10 times, and the THD of the ADC is preserved above 80 dB after calibration. While the 16 QAM signal shows a significantly longer 2nd stage calibration cycle than the sine wave and uniformly distributed random input counterpart, the input statistics do not affect the calibration robustness and accuracy.

C. Application on Split Pipeline ADC in 40 nm CMOS

A 1.1-V 200 MS/s split pipeline ADC has been implemented in 40 nm CMOS and the split ADC calibration is applied. Fig. 13 shows the architecture of the 12-bit split pipeline ADC to calibrate the first two stages. Each channel consists of four pipelined stages, with 2.5-bit (*2.5*) and shifted 2.5-bit (*2.5s*) residue characteristics, and a final 4-bit flash ADC stage. The digital outputs of the backend ADC of each split channel and the raw bits of the first two calibrated stages in both channels (*rb1a*, *rb2a*, *rb1b*,

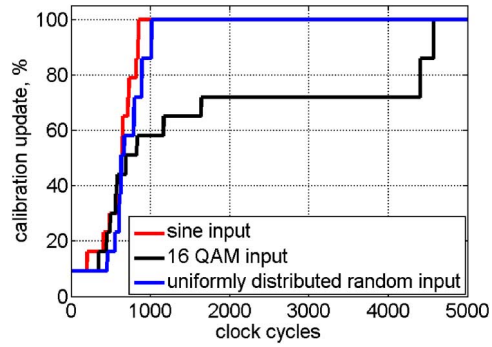

Fig. 11. 2nd stage calibration for different inputs.

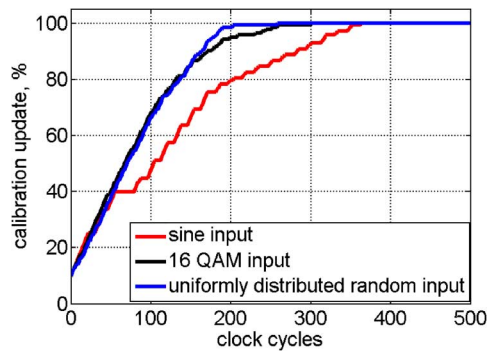

Fig. 12. 1st stage calibration for different inputs.

and *rb2b*) are used in the digital calibration algorithm to give the final calibrated ADC output D_{oc}. The digital calibration algorithm provides two output signals, *calend1* and *calend2*, which control the mode control logic block to change the residue characteristics of the split ADC channel a (*res1a*) and channel b (*res1b*), using the corresponding mode control signals *mca* and *mcb* respectively. The uncalibrated backend ADCs in both split channels are identical 2.5-bit stages and have been designed for a 12-bit accurate 200 MS/s ADC. The ADSC in the calibrated split pipelined stage needs to be accurate by two bits more than the stage resolution $(n+2)$ to ensure residue shift between the two split ADC Channels. This is one bit more accurate than the ADSC in the uncalibrated pipelined stage. The Monte Carlo transient simulations for the designed comparator give an offset standard deviation of $V_{ref}/2^7$, where V_{ref} is the ADC reference voltage. The split ADC is designed for approximately 75 dB signal-to-thermal noise ratio (SNR) to reduce the number of averaging required in the calibration calculations. The ADC linear errors, stemming from low gain amplifiers and unit sampling capacitor mismatches in the MDAC, are calibrated using the proposed technique, while the distortion in the MDAC due to amplifier non-linearity is not considered in the calibration, and thus the ADC THD will be limited by that of the MDAC. The amplifiers are designed for THD better than 78 dB, input-referred in the MDAC closed loop.

The designed circuits are verified in the transistor and post-layout levels to validate the proposed digital calibration performance. The very short calibration cycle eases the verification of the calibrated ADC and enables the simulation of the whole ADC in circuits and post-layout levels with a relatively affordable simulation time. To provide more flexibility in the test setup, the digital calibration engine is implemented off-chip, where the digital outputs of the split ADC channels are extracted from the circuit simulations, and then imported into MATLAB to perform the digital post-processing. As the proposed digital

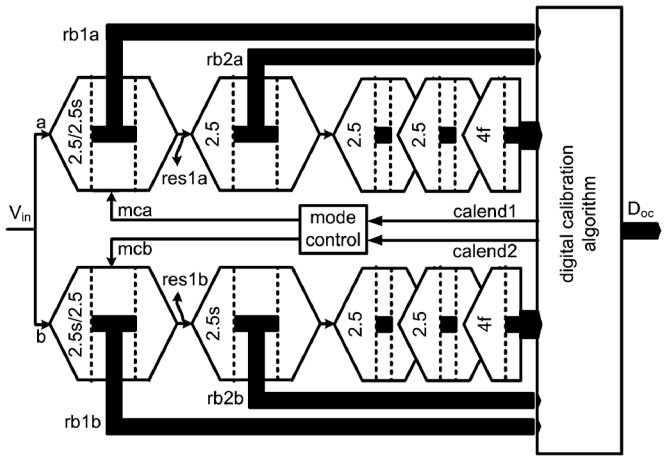

Fig. 13. Digitally calibrated ADC architecture.

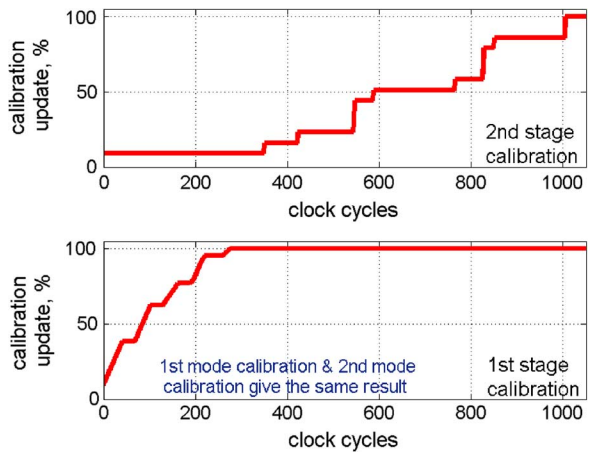

Fig. 14. Calibration cycle for the 1st and 2nd pipelined stages after parasitic extraction (post-layout simulation at $f_{in} = 1$ MHz and $f_s = 200$ MHz).

calibration technique requires no feedback from the analog circuits and merely processes the ADC digital outputs, operating on the off-chip digital outputs of the split ADC verifies the calibration without any loss of generality.

Post-layout transient simulations have been performed for the split pipeline ADC, with extracted parasitic capacitances. The calibration cycles for the first and the second stages are shown in Fig. 14, where 10 samples are averaged to have the results. 1555 clock cycles are needed to calibrate both stages with the two residue modes in the background, and only 275 clock cycles are needed to calibrate the first pipelined stage in the background. The ADC performance before and after calibration is shown in Fig. 15, where the calibration enhances the ADC THD from 49 dB to 78 dB, limited by the MDAC non-linear distortion. The 78 dB THD of the calibrated ADC is achieved without using extra quantization bits in the ADC, which confirm the accuracy of our developed fully deterministic calibration approach. Thermal noise is not included in these transient simulations, but averaging the calibration parameters 10 times should account for the targeted 75 dB SNR, as discussed in Section V-A.

Table I compares the calibration time of the proposed technique with that of prior art in terms of the number of clock cycles needed to complete the calibration, and the achieved spurious free dynamic range (SFDR). Digital calibration techniques are numerous, intermingled and widely vary, and here we compare to the main themes of calibration approaches, considering the least reported calibration time in each approach. By using

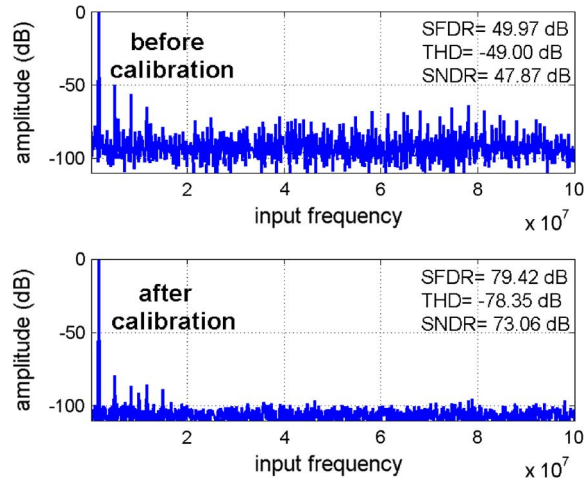

Fig. 15. ADC performance before and after calibration with C parasitic extraction (Post-layout simulation at $f_{in} = 1$ MHz and $f_s = 200$ MHz).

TABLE I
CALIBRATION TIME COMPARISON WITH PRIOR ART

Reference	Calibration technique	required cycles	SFDR
[4]	Correlation based on PRS insertion	2^{32}	94.9 dB
[5]	Statistical based on data histograms	$200\times\ 10^3$	90.9 dB
[6]	Skip and fill method	$15\times\ 10^3$	70 dB
[7]	Split ADC using LMS	$10\times\ 10^3$	70 dB
This Work	Split ADC using SMA	$1.555\times\ 10^3$	79.4 dB

SMA in split ADC, calibrating the two pipelined stages in the background requires more than 6x less time than the least calibration time reported for other techniques. Practically, as the deviation in the calibrated ADC performance with temperature in the second pipelined stage is scaled down by the gain of the first stage, background calibration can be considered only for the first stage, and thereby only 275 clock cycles are needed to complete the calibration cycle in the background.

The digital calibration performance is affected by the variation in the amplifier gain due to temperature or supply variations. These variations can be tracked and compensated for in the background by the proposed calibration scheme with its very fast calibration cycle. In addition of the rapid calibration tracking, and to ensure minimum linearity degradation due to gain variation, the amplifier gain is made 44 dB to preserve the ADC SNDR above 68 dB with 10% gain variation, as discussed in [11].

A limitation in the proposed calibration could arise when the pipeline ADC don't use a front-end sample and hold. This is particularly important for high frequency inputs, when a potential mismatch in the input sampling between the two channels of the split ADC causes a degradation in the overall calibration performance, as the concept of calibration depends on processing the same input between the two channels. This issue can be treated by using a common bottom plate sampling switch between the split ADC channels, as discussed in [12], and the results for input frequencies up to 160 MHz shows a THD of more than 75 dB.

D. Area and Power Overhead of Splitting the ADC

As mentioned in Section II, splitting the ADC into two channels should results in a minimum overhead in area and power, which is especially true in thermal noise-limited high resolution designs. The added area and power will be mainly due to

doubling the number of ADSCs, clock buffers, and the accompanying digital logic. Considering these in the split ADC after layout, these circuits represent an approximate addition of 10% in area and power. In an absolute basis, the area and power of the implemented 40 nm 200 MS/s 12-bit split ADC after parasitic extraction are 0.42 mm^2 and 54 mW respectively. Comparing these to a similar 90 nm ADC, the 200 MS/s 12-bit ADC in [6] consumes area and power of 1.36 mm^2 and 186 mW respectively. These suggest that splitting the ADC for calibration in a high resolution design is an efficient approach.

VI. Conclusion

In this paper, a fast digital multistage calibration based on split ADC for pipeline converter is presented. The proposed background calibration follows a fully deterministic approach, which significantly reduces the calibration time and increases the accuracy of calibration. Compared to other techniques which use blind error estimation or feedback loops like LMS, the proposed technique based on SMA gives better accuracy in a much less time without the need of extra ADC quantization, thereby saving area and power. Practical considerations have been considered and the calibration technique shows a sufficient robustness. The area and power overhead of splitting the ADC is minimal in high resolution designs, and the post-layout simulation results of a 12-bit 200 MS/s split pipeline ADC in 40 nm CMOS demonstrate the efficiency and the accuracy of the proposed technique.

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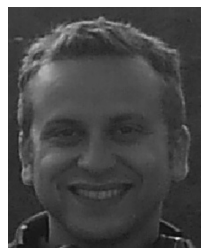

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