Analog Integr Circ Sig Process (2016) 87:353–368
DOI 10.1007/s10470-016-0736-y

Pipelining method for low-power and high-speed SAR ADC design

Ziba Fazel[1] · **Saeed Saeedi**[2] · **Mojtaba Atarodi**[1]

Received: 30 December 2015 / Revised: 22 March 2016 / Accepted: 31 March 2016 / Published online: 8 April 2016

Abstract A low power analog to digital converter (ADC), based on a pipelining method employed in successive approximation register (SAR) architecture is presented. This structure is a two-stage pipeline SAR ADC with asymmetrical time interleaved (TI) channels, aimed to reach sampling rate as high as about threefold of a conventional SAR ADC while benefiting from its low power consumption and small area. Passive residue conversion without inter-stage amplifier and symphonic collaboration of stages are employed to design a low power, high speed, and accurate converter. In the proposed architecture, every signal sample experiences equal comparator offset during its conversion due to the applied novel operation sequence, without adding redundancy or comparator rotation scheme. A 7-bit ADC with sampling rate of 83 MS/s based on the proposed architecture is designed and its performance is verified by post layout simulation results in a 180-nm CMOS Technology. Both system level analysis and simulation verifications support proposed architecture superiority over similar reported SAR architectures.

✉ Mojtaba Atarodi
atarodi@sharif.edu

Ziba Fazel
ziba_fazel@ee.sharif.edu

Saeed Saeedi
saeed.saeedi@modares.ac.ir

[1] Electrical Engineering Department, Sharif University of Technology, P.O. Box 14115-111, Tehran, Iran

[2] Faculty of Electrical and Computer Engineering, Tarbiat Modares University, Tehran, Iran

Keywords SAR ADC · Pipelining · Passive residue conversion · Asymmetrical time interleaving · Low power · High sampling rate

1 Introduction

Analog to digital converter (ADC) is one of the key functional blocks of any mixed signal system. It should be optimally designed concerning both performance and power consumption. Various ADC architectures such as pipeline, flash, folding and successive approximation register (SAR) have been employed to meet different requirements of sampling speed, power consumption and resolution. SAR ADC is known as a low-power, low-speed and low-complexity architecture, as it employs only a comparator over N clock cycles to determine N bits of the sampled analog input [1, 2]. This feature makes SAR ADC one of the most popular architectures for biomedical, modern portable and wireless applications. In addition, scaling of CMOS technology increases the sampling rate and reduces power consumption of SAR ADCs which are replacing pipelined ADCs due to their wider input signal bandwidth [3, 4].

To achieve the desired ADC performance, efforts are usually focused on improvement of circuit techniques or introduction of novel architectures. Advantages of the SAR ADC have made it attractive for introducing novel combinational architectures [5–18]. These architectures employ different techniques to increase sampling rate or resolution of SAR ADC while benefiting from its low power consumption. Pipelined and time interleaved (TI) ADCs based on SAR, supported by many improving systematic techniques, are the most common architectures.

A conventional pipelined SAR employs a multiplying digital-to-analog converter (MDAC) with a residue

amplifier between stages [5, 6]. Designing high gain MDAC is needed for high resolution and high speed ADCs; however, it increases power consumption for wide input bandwidth and becomes more difficult as technology scales down due to the lower intrinsic gain of transistors and lower supply voltages. To overcome these issues, some reported pipelined SAR structures have tried to share, replace or omit the inter-stage MDAC [7–12]. Sharing a unique MDAC between stages improves power efficiency; however due to the use of a single MDAC in different stages, there are probable gain errors and also a rigid limitation on allowed time for residue amplification. To overcome this limitation, different timing-derived techniques have been employed to maximize the speed of implemented ADC [7–9], but they consumes extra power. Replacing MDAC with a simple bucket-brigade circuit, in which charge is moved from a large capacitor to a small capacitor to realize voltage gain, reduces power consumption especially in its Op-Amp-less realization [10, 11]; but it results in inaccurate settling besides signal dependent and temperature-variant linear and nonlinear errors [11]. Another method of pipelining in SAR topology is transferring the residue from the first stage to the second stage in a passive way to eliminate the power consumption of inter-stage amplifiers [12]. In this method, the residue charge stored on the first stage capacitors is transferred to the second stage by moving a part of the most significant bit (MSB) capacitor to the second stage. The comparators are also moved among stages to reduce the nonlinearity due to the unequal offset of comparators in different stages [12]. The disadvantage of this architecture is accuracy degradation due to the moving the first stage capacitor, which holds the residue, to the second stage. In this moving, the residue charge may be changed by more than one LSB because of circuit imperfections such as charge sharing and non-idealities of the switches. In addition, the employed comparator rotation increases the switching activity significantly.

In TI SAR ADCs, power consumption is increased linearly with the number of interleaved channels and accuracy degrades due to the mismatches between the channels, such as offset, gain error and timing skew. Therefore, calibration is necessary in these architectures [13]. Various circuit or system techniques have been utilized to minimize power consumption in TI SARs [14–17]. For example, pipelining a Flash ADC, as the first stage, and a TI of SAR ADCs, as the second stage, reduces the number of conversion cycles and eliminates the MDAC [17]. However, this topology does not benefit from the intrinsic track and hold (T/H) operation implemented in the SAR topology, due to the employed flash ADC in the first stage and a separate T/H circuit is required in the ADC front-end. The extra T/H circuit consumes excessive area and also requires an additional clock scheme for its operation [17, 18]. In addition, increasing available number of bits from the flash topology to raise the sampling rate increases the number of comparators and results in power increment and linearity degradation [18].

This paper presents a pipelining method for enhancing throughput of the SAR ADC while trying to retain its power efficiency. The ADC is a two stage pipelined SAR with an asymmetrical TI method applied to each stage for increasing the sampling rate. The proposed SAR architecture benefits from passive residue conversion without inter-stage amplifier. Optimal arrangement of operating stages and channels is proposed to reduce area, enhance power efficiency and increase sampling speed compared to the previous works. These advantages are achieved due to the attempts made in this work to minimize the number of comparators, eliminate the inter-stage amplifier, reduce the effect of comparators' input parasitic capacitance, reduce the effect of switches and minimize the number of TI channels. Resolutions and hence the capacitance of the two stages are adjusted to minimize the amount of first stage capacitance and balance settling time of the two stages. In contrast to [12], the capacitor holding the residue is not moved between stages in the proposed method, so the residue is not impacted by circuit imperfections. Instead, an auxiliary capacitive array is employed and connected to the idle port of the comparator for residue conversion. In addition, the comparator rotation scheme with high switching activity, as used in [12], is not utilized in the proposed circuit, however, the signal experiences the same comparator offset in every comparison.

The rest of the paper is organized as follows: Sect. 2 explains the proposed ADC architecture and its operation details. Systematic comparison of the proposed SAR ADC topology with some other ADC structures is presented in Sect. 3. Section 4 covers linearity analysis of the proposed architecture and its design considerations. Section 5 describes circuit design, followed by post-layout simulation results in Sect. 6 and conclusions in Sect. 7.

2 Proposed ADC architecture

Figure 1 shows the overall architecture of the proposed ADC. The ADC is a two-stage pipelined SAR with TI method applied to each stage. N1 most significant bits (MSBs) and N2 least significant bits (LSBs) for $N = N1 + N2$ bits conversion are produced by the first and the second stage, respectively. The ADC consists of two stages, a main controller, a reference voltage generator and a bit concatenator. The 1st-stage has three channels, named "Ch1, Ch2, and Ch3" in Fig. 1, each consists of an N1 bit capacitor array, a SAR logic, an analog multiplexer,

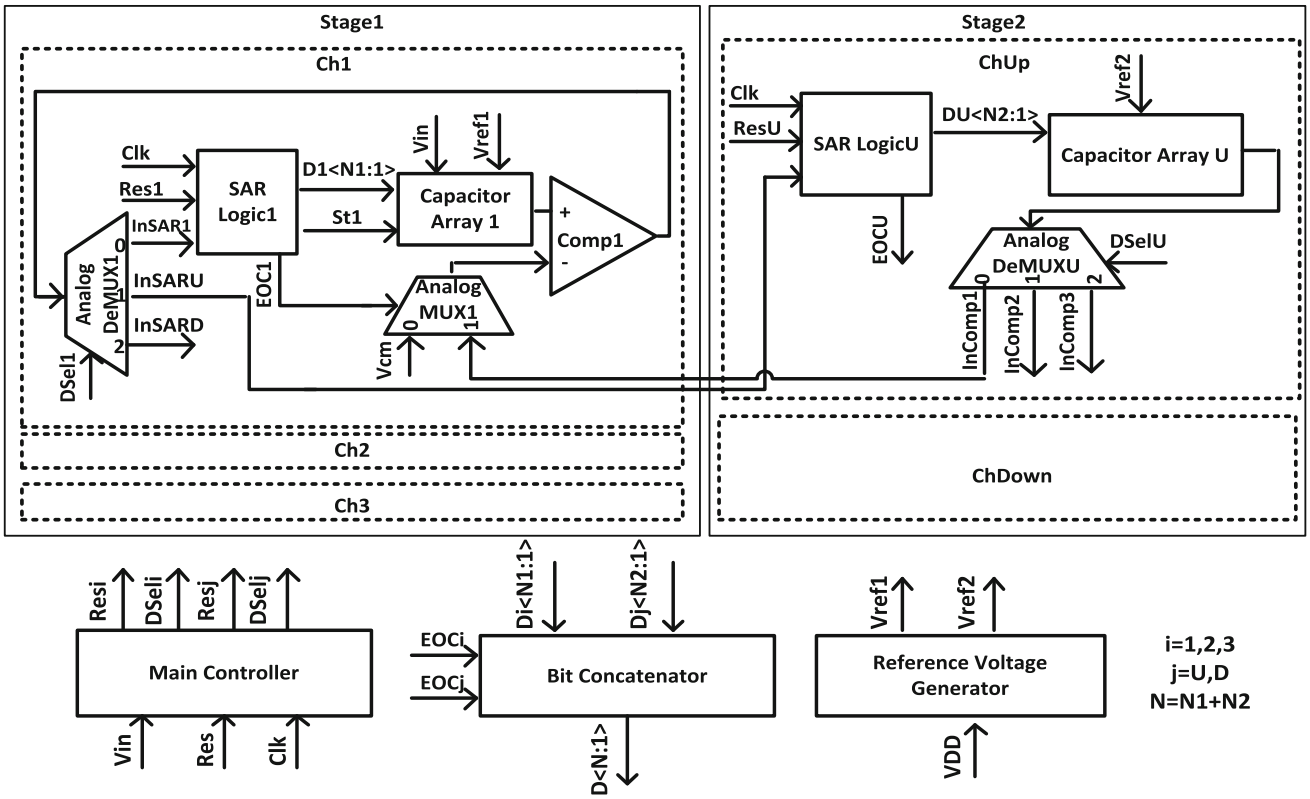


Fig. 1 Proposed pipelined SAR ADC with asymmetrical TI stages

and an analog de-multiplexer. The 2nd-stage has two channels, named "ChUp and ChDown" in Fig. 1, each consists of an N2 bit capacitor array, a SAR logic, and an analog de-multiplexer. The channels of the stage have no comparators. They employ each of the first stage comparators in different conversion intervals. The analog de-multiplexers of the 2nd-stage, named "Analog Demux U (D)" in Fig. 1, connects the output of each capacitor array of the 2nd-stage to the appropriate comparator of the 1st-stage during the LSB generation by the second stage. Analog multiplexers and de-multiplexers of the 1st-stage, named "Analog Demux1 (2or3)" and "Analog Mux1 (2or3)", are employed for completing this connection. Analog Demux connects output of each comparator to the appropriate SAR logic and Analog Mux connects the common mode voltage (Vcm) or output of the capacitor array of the 2nd-stage channels to the comparator. The main controller in Fig. 1 organizes the operation sequence of each SAR block and provides the required selection signals for the analog de-multiplexers.

Figure 2 shows timing diagram of the proposed SAR ADC for N = 7 and N1 = 2. As shown in this figure, the first SAR channel of 1st-stage ("Ch1" in Fig. 1) samples the input on the capacitors when its start signal ("St1" in Fig. 1) is activated by the main controller, and in the following clock cycles employs the sampled input, S1, to generate the corresponding MSBs, D1 ⟨2:1⟩ . These bits are generated by the SAR algorithm, i.e. they become high and based on the comparator result, remain high or become low. The second and third channels ("Ch1" and "Ch2" in Fig. 1) also generate the MSBs, D2 ⟨2:1⟩ and D3 ⟨2:1⟩, from the samples S2 and S3, after activation of their start signals ("St2" and "St3" in Fig. 1) by the main controller, respectively. For each SAR channel of 1st-stage, it takes (N1 + 1) clock cycles to sample the input voltage and convert it to the proper N1-bit.

After converting N1 MSBs, the charge stored on the capacitor array of each SAR channel of 1st-stage equals the residue voltage, ($V_{cm} - V_{in} + V_{out,\ DAC,\ stage1}$). At this time, the end-of-conversion (EOC) signal of each SAR block is activated, showing that the proper residue is ready on the top plate of the capacitor array. Instead of transferring the residue to the 2nd-stage channels, one of the idle up or down capacitor array is connected to the other input of comparator through the analog de-multiplexers and multiplexers to convert the residue voltage and produce the N2 LSBs in the following N2 clock cycles. By employing this technique for passive residue conversion, the inter-stage amplifier in the pipeline architecture is omitted. In addition, conversion of each sample and generation of MSBs and LSBs in the first and second stage are performed by a specific comparator and the signal

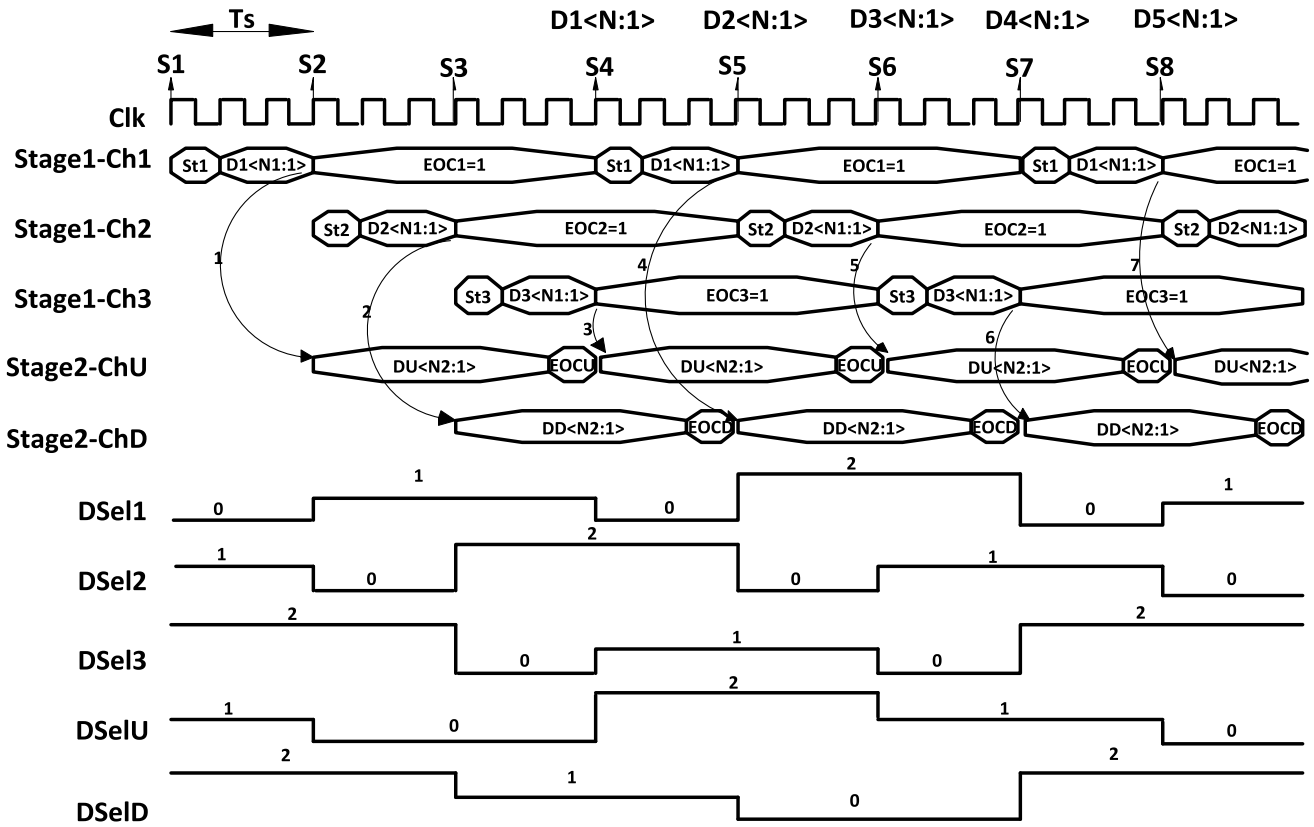


Fig. 2 Timing diagram of a conversion in the proposed ADC

experiences the same comparator offset in every comparison. Therefore, the nonlinearity due to the different offset of comparators in the conventional two stage implementation is reduced and the advantage of a single stage SAR ADC is retained to a great extent.

As shown in Fig. 1, the required selection signals in the analog de-multiplexers and multiplexers, namely Dseli, Dselj, and EOCi are provided by the main controller and the three SAR logic controllers, respectively. Due to the passive residue conversion in this design, reference voltages of N1-bit SAR blocks (Vref1 in Fig. 1) and N2-bit blocks (Vref2 in Fig. 1) are different, in other words, the former is equal to the input full scale range while the latter is equal to $\frac{1}{2^{N1}}$ of the full scale range.

As illustrated in Fig. 2, the residue voltage of the sample S1 is employed by the up SAR block after generation of D1 $\langle 1 \rangle$ to produce the five LSBs of this sample, DU $\langle 5:1 \rangle$, successively. Activation of the up SAR block for conversion of five LSBs of S1 and activation of "St2" for sampling and generation of two MSBs of S2 take place simultaneously. According to Fig. 2, as the up SAR block is busy when the two MSBs of S2 is ready, i.e. activation of EOC2, generation of S2 LSBs is performed by the down SAR block (DD $\langle 5:1 \rangle$ in Fig. 2). Activation of the down SAR block for conversion of five LSBs of S2 takes place at the same time as activation of the "St3", when the sample S3 is taken by the third N1-bit SAR block to determine its MSBs (D3 $\langle 2:1 \rangle$). After generation of D3 $\langle 2:1 \rangle$, the up SAR block becomes idle such that it produces the LSBs of the sample S3 while the down SAR block is still busy generating LSBs of the sample S2. The conversion continues with sampling the input for the fourth time by the first channel of 1st-stage and so on. As shown in Fig. 1, the control signals EOC1, EOC2, EOC3, EOCU, and EOCD which are generated by the five SAR controllers, are employed in the bit concatenator block to concatenate N1 MSB bits of each sample to its corresponding N2 LSBs.

The key point in the proposed architecture is employing the residue as soon as it is produced by the N1-bit SAR blocks of 1st-stage by the just idled N2-bit SAR block of 2nd-stage in a passive way such that the throughput of the system, i.e. the number of converted analog samples to digital data per unit time, is maximized. For this purpose, N1 and N2 should be chosen carefully. According to Fig. 2, if N2 is equal to $2 \times N1 + 1$, the ADC is able to sample the analog input and produce the corresponding N-bit data every $N1 + 1 = \frac{N+2}{3}$ clock cycles with a latency of $N + 2$ clock cycles. Compared to a conventional N-bit

SAR ADC, which produces N-bit data every N + 1 clock cycles, throughput of the proposed architecture is enhanced by $\frac{3(N+1)}{N+2}$.

The proposed ADC can also be implemented in a differential architecture. For this purpose, a comparator with two differential inputs, i.e. a four input comparator as illustrated in [19], should be employed. In this structure, in the second conversion phase, a differential input pair of the comparator is connected to the second stage capacitive DAC, while the other differential pair holds the residue from the first conversion phase. Thus, the differential version of the proposed technique becomes similar to the single-ended topology in Fig. 1 in terms of capacitive attenuation.

3 Systematic comparison

A popular way to compare a new architecture with others is considering power consumption, conversion speed or throughput, resolution, silicon area and ability to tolerate non-idealities. In this section, for comparison of the proposed architecture with some other ones, it is assumed that all architectures have the same resolution and conversion rate and the aim is comparing energy per conversion, silicon area and latency. As circuit implementations also affect these parameters, conventional structure of a SAR ADC with binary weighted capacitor array is assumed to be used in all architectures.

For a conventional N-bit SAR ADC, which produces N-bit data every N + 1 clock cycles, power consumption is given by

$$P_{ConvADC} = P_{Comp} + P_{DAC} + P_{Logic} \quad (1)$$

where P_{comp}, P_{DAC} and P_{logic} are power consumption due to the comparator, DAC and control logic, respectively. For the comparison, regardless of the employed circuits, only the DAC power is considered. This is because power consumption of the capacitive DAC circuit is increased by 2^N while the power consumption of the comparator and the control logic is increased by a smaller extent compared to 2^N. Therefore, the DAC power consumption is dominant in SAR ADCs and the power consumption of the comparators and control logic is not critical, even for higher resolution, as indicated in the ten-bit design in [20]. For an N-bit binary weighted capacitor array DAC with a unit capacitor of C_u and full scale range of V_{ref}, required energy in a clock cycle equals [20]

$$E_{conventional} = P_{ConvADC}T_{clk} \approx \frac{P_{DAC}}{f_{clk}} \approx 0.66 \times \left(\frac{2^N \times V_{ref}^2}{N+1}\right) \times C_u \quad (2)$$

As discussed in the previous section, for a conversion rate of f_S samples/second, an N-bit conventional SAR ADC requires a clock with a frequency of $f_{clk} = (N + 1) \times f_S$. Therefore, from (2), power consumption of the conventional SAR ADC normalized to the conversion rate f_S, i.e. energy per conversion, is given by

$$\frac{P_{ConvADC}}{f_s} \approx 0.66 \times 2^N \times V_{ref}^2 \times C_u \quad (3)$$

For the proposed N-bit SAR ADC architecture, with N = N1 + N2, power consumption is given by

$$P_{propADC} = 3P_{Comp} + P_{DAC,Stage1} + 2P_{DAC,Stage2} + P_{Logic} \quad (4)$$

where $P_{DAC,\ Stage1}$ and $P_{DAC,\ Stage2}$ are power consumption due to the one of N1-bit DACs in 1st-stage and one of the N2-bit DACs in the 2nd-stage, respectively. As only one of the N1-bit DACs works at a given time and the other two only holds the residue at that time, $P_{DAC\text{-}Stage1}$ appears with a factor of 1 while $P_{DAC\text{-}Stage2}$ has a coefficient of 2 because both of the N2-bit DACs are busy in all times. Although the number of comparators is three in this TI design and it appears as *3Pcomp* in (4), the throughput is also increased by three times compared to a conventional SAR with one comparator. Thus, only considering the comparator power consumption, it does not degrade the energy per conversion of the proposed ADC, with due attention to the energy per conversion formula. Hence neglecting power consumption of the comparators and control logic, required energy of the proposed ADC in a clock cycle equals

$$E_{proposed} = P_{propADC}T_{clk} \approx \frac{P_{DAC,Stage1} + 2P_{DAC,Stage2}}{f_{clk}} \approx 0.66 \times \left(\frac{2^{N1}V_{ref_1}^2}{N1+1} + \frac{2 \times 2^{N2}V_{ref_2}^2}{N2+1}\right) \times C_u \quad (5)$$

where $V_{ref_1} = V_{ref}$ and V_{ref_2} is the reference voltage of the N2-bit SAR blocks and is equal to $V_{ref_1}/2^{N1}$. As discussed in the previous section, the proposed N-bit SAR ADC requires a clock with a frequency of $f_{clk} = \frac{N+2}{3} \times f_S$. Therefore, power consumption of the proposed SAR ADC normalized to the conversion rate, f_S, is given by

$$\frac{P_{propADC}}{f_s} \approx 0.66 \times \frac{N+2}{3} \times \left(\frac{2^{N1}}{N1+1} + \frac{2 \times 2^{N2}}{2^{2N1} \times (N2+1)}\right) \times V_{ref}^2 \times C_u \quad (6)$$

To compare the silicon area of the conventional N-bit SAR ADC with the proposed SAR ADC, it can be assumed that the DAC area is dominant. Therefore the area of these architectures are expressed as

$$A_{Si,prop} = 3 \times 2^{N1} \times A_{Cu} + 2 \times 2^{N2} \times A_{Cu} \quad (7)$$

$$A_{Si,conv} = 2^{N} \times A_{Cu} \quad (8)$$

where A_{Cu} is the area of a unit capacitor element.

Table 1 summarizes comparison results of the proposed ADC with similar architectures in terms of throughput, latency, energy per conversion and silicon area. For generating the column of "Energy/conversion" in Table 1, as indicated above, all architectures are assumed to have the same resolution, N = 7, and the same conversion rate, fs. Then the dominant energy consumption of the capacitive DAC, which is assumed binary weighted with unit capacitor equals C_u in all architectures, has been normalized to the conversion rate. The full scale range of the ADCs, V_{ref}, is also assumed to be equal to the supply voltage V_{DD}. It should be mentioned that the power consumption of the circuits like: comparators, complex logic circuits and opamps in all architectures is neglected because the power of the capacitive DAC in SAR ADCs is almost dominant regardless of the employed architecture and resolution [20].

Due to the proposed technique for separating the MSB's DAC from LSB's DAC in this design, the power consumption of the ADC has been reduced significantly. Hence, the energy/conversion of the proposed ADC is lower than other similar architectures at the same sampling rate and resolution, in Table 1. Estimated silicon area of proposed ADC seems to be more than that of a few reported structures. This is due to neglecting complexity of other blocks in those architectures such as Op-Amps and sharing networks. In addition, implementing the 2nd-stage DACs by binary weighted capacitor array with one series capacitor as attenuator, according to [20], reduces the area of the proposed ADC to $20 \times A_{Cu}$. Considering the layout area of the proposed topology, as shown in Table 2 in Sect. 6, reveals its area efficiency more significantly.

Compared to the conventional TI SAR in [16], the main advantage of the proposed topology in this paper is implementing a TI scheme, which benefits from SAR power efficiency and compact design. For implementing the conventional TI in SAR ADCs, the number of channels should be equal to the number of the bits in each SAR because each channel will not be idle to receive the new input sample until it completes its conversion. This limitation on minimum number of channels in conventional TI SARs leads to an inefficient TI design in terms of area and power consumption [16]; Moreover, it results in complex clock distribution in the chip and increases mismatches and timing skew among channels. The proposed specific TI architecture mitigates this issue such that a TI SAR ADC with seven-bit resolution and with three times higher throughput compared to a single-stage SAR can be realized. The applied asymmetrical TI method in this paper leads to smaller and more compact ADC compared to a conventional SAR TI and hence would less suffer from timing skew. It should be mentioned that, to implement a seven-bit TI ADC with three times higher throughput, other ADC topologies such as flash can also be utilized but the resulting architecture will not take the low-power and compact-design advantages of the SAR.

4 Design considerations and non-ideality tolerance

In a conventional SAR ADC, the comparator offset voltage does not affect the overall linearity of the conversion. It is represented as a voltage source in series with sample and

Table 1 System level comparison of 7-bit ADC architectures based on SAR with the same sampling rate (f_S)

Ref	SAR architectures (7 bit ADCs)	Throughput $\left(\frac{Conversion}{\#ofclkcycles}\right)$	Latency # of clks	f_{clk}	Energy per conversion	Area
–	This work	$\frac{1}{3}$	9	3 f_S	$3.96 \times C_u \times V_{DD}^2$	$76 \times A_{C_u}$
[20]	Conventional	$\frac{1}{8}$	8	8 f_S	$84.48 \times C_u \times V_{DD}^2$	$128 \times A_{C_u}$
[5]	Two stage pipeline (conventional)	$\frac{1}{5}$	5	5 f_S	$17.15 \times C_u \times V_{DD}^2$	$32 \times A_{C_u}$
[11]	Pipeline with MDAC replacement	$\frac{1}{4.5}$	9	4.5 f_S	$17.02 \times C_u \times V_{DD}^2$	$28.8 \times A_{C_u} + A_{Capacitorofbucketbrigade}$
[8]	Pipeline with inter-stage shared MDAC	$\frac{1}{3.75}$	15	3.75 f_S	$13.52 \times C_u \times V_{DD}^2$	$16.82 \times A_{C_u}$
[9]	Pipeline with inter-channel shared MDAC	$\frac{1}{4.5}$	10	4.5 f_S	$17.02 \times C_u \times V_{DD}^2$	$56.6 \times A_{C_u}$
[12]	Pipeline with passive residue transferring	$\frac{1}{3.7}$	12	3.7f_S	$13.9 \times C_u \times V_{DD}^2$	$20.91 \times A_{C_u}$
[18]	Assisted pipeline with flash	$\frac{1}{7}$	7	7f_S	$14.78 \times C_u \times V_{DD}^2$	$128 \times A_{C_u}$
[16]	TI of SARs	1	8	f_S	$84.48 \times C_u \times V_{DD}^2$	$1024 \times A_{C_u}$
[17]	TI of SARs-assisted with flash	1	5.5	f_S	$7.467 \times C_u \times V_{DD}^2$	$576 \times A_{C_u}$

hold output, indicating that offset voltage simply adds to analog input and hence appears as an offset in the overall characteristics. In the proposed ADC architecture, without residue amplification, nonlinearity errors due to the offset mismatches of the comparators in different stages can become larger [12]. This issue is mitigated by employing the same comparator for each sample conversion. As discussed in the Sect. 2, despite of utilizing three different comparators, each signal sample is converted by the same comparator and hence experiences equal comparator offset during the conversion. The timing arrangement of comparators is shown in Fig. 3 for more clarification. Each row in Fig. 3 shows the busy parts of the proposed ADC structure in sampling and conversion of every input signal sample (S_i) to a seven-bit output data (Di $\langle N:1 \rangle$). Figure 3 shows that for conversion of sample 1 to its MSBs, ch1 is employed and then to convert the produced residue to the LSBs, the auxiliary capacitive array of Ch-Up from the 2nd-stage is connected to the idle port of comparator1 already used in its MSBs' conversion. Then for conversion of sample 2 to its MSBs, Ch2 is employed and to convert the produced residue to the LSBs, capacitive array of Ch.-Down from the 2nd-stage is connected to the idle port of comparator2 already used in its MSBs' conversion. Good to mention that for conversion of sample 4 to its MSBs, ch1 is again used and for its LSBs conversion, this time, Ch. Down capacitive array is used. The rotation of capacitive DACs of the 2nd-stage instead of the comparators rotation, translates the offset of the comparators to the sample-to-sample or channel-to-channel offset which could be easily cancelled by channel-offset calibration [12].

Another non-ideality effect in the SAR ADC topology is the nonlinearity due to the errors in the DAC capacitors. This effect is estimated, in the rest of this section, for the proposed and conventional SAR architectures. To analyze the effect of the error in the capacitor value on the linearity of the SAR with conventional switching, each of the capacitors in the binary weighted DAC is modeled as the sum of a nominal capacitance value and an error term [22]

$$C_i = 2^{i-1}C_u + \delta_i \tag{9}$$

where C_i, C_u and δ_i refer to ith capacitor of the DAC array, capacitance value of a unit capacitor, and the error of the ith capacitor, respectively. Considering the values of the unit capacitors as independent identically distributed Gaussian random variables, variance of δ_i equals [22]

$$E\left(\delta_i^2\right) = 2^{i-1}\sigma^2 \tag{10}$$

where σ is the standard deviation of unit capacitor. To calculate DAC output ($V_{out}(X)$) to its corresponding digital input X, the array is considered initially discharged; i.e. $V_{in} = 0$. Then the analog output of the N bit capacitive DAC can be stated as [22]

$$V_{out}(X) = \frac{\sum_{i=1}^{N}(2^{i-1}C_u + \delta_i)S_i + (C_u + \delta_0)S_0}{2^N C_u + \sum_{i=0}^{N}\delta_i} \cdot V_{ref} \tag{11}$$

where S_i shows the connection of each capacitor to V_{ref}, or ground and is equal to 1, or 0, in each case, respectively. Excluding gain error effect, integral nonlinearity (INL) and differential nonlinearity (DNL) are [22]

$$\begin{aligned} INL &= \frac{V_{out}(X) - V_{idl}(X)}{V_{LSB}} \\ DNL &= \frac{(V_{out}(X) - V_{out}(X-1)) - V_{LSB}}{V_{LSB}} \end{aligned} \tag{12}$$

where $V_{idl}(X)$ and V_{LSB} are the ideal DAC output at the code X and LSB voltage of ADC, respectively. The maximum DNL for the conventional switching occurs at the step below the MSB transition. The difference between two corresponding codes is defined by [22]

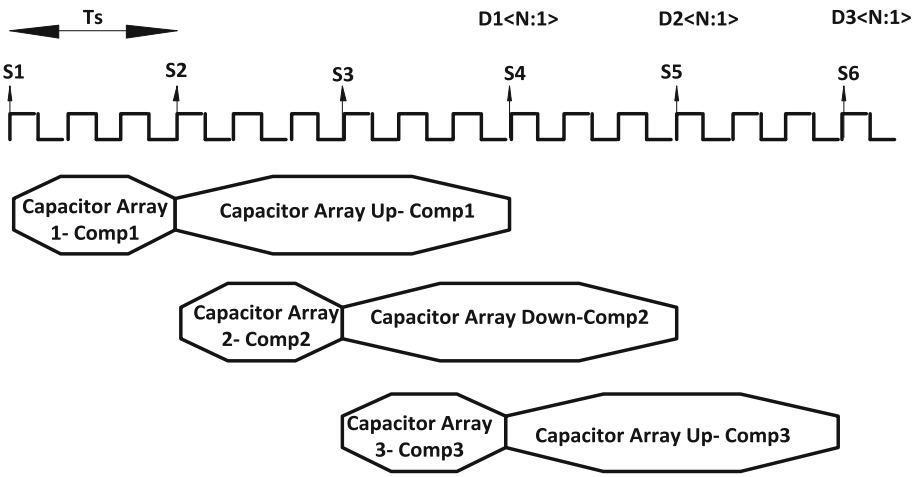


Fig. 3 Eliminating the comparators' offset effect on the linearity of the proposed ADC

$$V_{out}(X) - V_{out}(X-1) = \frac{C_u + \delta_N - \sum_{i=1}^{N-1}\delta_i}{2^N C_u}.V_{ref} = LSB.\left(1 + \frac{\delta_N - \sum_{i=1}^{N-1}\delta_i}{C_u}\right) \quad (13)$$

The DNL of conventional N bit SAR ADC can be calculated as [22]

$$DNL_{conventional} = \frac{\delta_N - \sum_{i=1}^{N-1}\delta_i}{C_u} \quad (14)$$

Therefore, its variance equals [22]

$$E\left[\delta^2_{DNL-conventioanl}\right] = \frac{(2^N-1)\sigma^2}{C_u^2} \quad (15)$$

The worst INL in the conventional switching happens at the MSB transition, where only the MSB capacitor is precharged to V_{ref}, leaving the other capacitors to the ground; Its corresponding output is defined by [22]

$$V_{out}(X) = \frac{2^{N-1}C_u + \delta_N + C_u + \delta_0}{2^N C_u}.V_{ref} \quad (16)$$

Then the INL of conventional N bit SAR ADC can be calculated as [22]

$$INL_{conventional} = \frac{\delta_N + \delta_0}{2^N C_u}.\frac{V_{ref}}{LSB} = \frac{\delta_N + \delta_0}{C_u} \quad (17)$$

Therefore, its variance equals [22]

$$E\left[\delta^2_{INL-conventioanl}\right] = \frac{2^{N-1}\sigma^2}{C_u^2} \quad (18)$$

In the same way, the effect of the error in the capacitor value on the linearity of the proposed ADC architecture is analyzed. For comparability, it is assumed that the conventional binary weighted array DAC with equal unit capacitor (C_u) is employed in both stages. As the MSBs are defined by the capacitor array of the 1st-stage, it is expected to observe its dominant role in the overall linearity.

For DNL estimation, like Eq. 13, the difference between two determinant codes of the 2nd-stage equals:

$$V_{DAC,Stage2}(X) - V_{DAC,Stage2}(X-1) = \frac{C_u + \delta_{N_2} - \sum_{i=1}^{N_2-1}\delta_i}{2^{N_2}C_u}.V_{ref2} \quad (19)$$

where $V_{DAC,Stage2}(X)$, N_2, and V_{ref2} are output voltage of capacitor array for input code X, resolution and reference voltage of 2nd-stage, respectively. V_{ref2} equals $V_{LSB,stage1}$ due to the determination of MSBs in the1st-stage.As the linearity is being analyzed, $V_{LSB,Stage1}$ must be replaced with the difference between two determinant codes of 1st-stage, which equals

$$V_{LSB,Stage1} = \frac{V_{ref1}}{2^{N_1}}.\left(1 + \frac{\delta_{N_1} - \sum_{i=1}^{N_1-1}\delta_i}{C_u}\right) \quad (20)$$

where N_1, and V_{ref1} are resolution and reference voltage of 1st-stage, respectively. So from Eqs. 19 and 20 and after some simplifications, DNL of the proposed ADC architecture will be defined by

$$DNL_{propADC} = \frac{\delta_{N_1} - \sum_{i=1}^{N_1-1}\delta_i}{C_u} + \frac{\delta_{N_2} - \sum_{i=1}^{N_2-1}\delta_i}{C_u} + \frac{\delta_{N_1} - \sum_{i=1}^{N_1-1}\delta_i}{C_u}.\frac{\delta_{N_2} - \sum_{i=1}^{N_2-1}\delta_i}{C_u} \quad (21)$$

Neglecting the third term, its variance will equal

$$E\left[\delta^2_{DNL,propADC}\right] = \frac{(2^{N1} + 2^{N2} - 2)\sigma^2}{C_u^2} \quad (22)$$

Applying the same approach, the overall INL equals

$$INL_{propADC} = \frac{\frac{2^{N_2-1}C_u + \delta_{N_2}}{2^{N2}C_u}.V_{LSB-Stage1} - \frac{2^{N_2-1}C_u}{2^{N_2}C_u}.\frac{V_{ref1}}{2^{N_1}}}{\frac{V_{ref1}}{2^{N_1+N_2}}} \quad (23)$$

where $V_{LSB,stage1}$ is being replaced by Eq. 10

$$INL_{propADC} = \frac{2^{N_2-1}C_u + \delta_{N_2}}{C_u}.\left(1 + \frac{\delta_{N_1} - \sum_{i=1}^{N_1-1}\delta_i}{C_u}\right) - \frac{2^{N_2-1}C_u}{C_u} \approx \frac{\delta_{N_2}}{C_u} \quad (24)$$

So its variance will equal

$$E\left[\delta^2_{INL,propADC}\right] = \frac{2^{N_2-1}\sigma^2}{C_u^2} \quad (25)$$

As N_1 and N_2 are always less than N, the DNL and INL in (22) and (25) show better linearity of the proposed ADC architecture with N bit resolution compared to a conventional N bits SAR ADC. For generating nonlinearity histogram from Matlab, each capacitor, in the code, is defined as a number of unit capacitors in parallel and the unit capacitor, C0, is defined to be exactly like the capacitor in technology file. The standard deviation is also extracted from the data of the technology documents. The nonlinearity histograms from MATLAB simulations for a sven-bit realization of a conventional SAR ADC and the proposed ADC and with Cu = 50f and the standard deviation of $\sigma = 0.0032$ for 200 samples per code are depicted in Figs. 4 and 5, respectively, confirming superiority of the proposed ADC linearity. As shown in Fig. 5, DNL and INL of the proposed topology have relatively large values when the MSBs changes. As the 1st-stage, which has low number of bits, determines the MSBs, its capacitor array can be

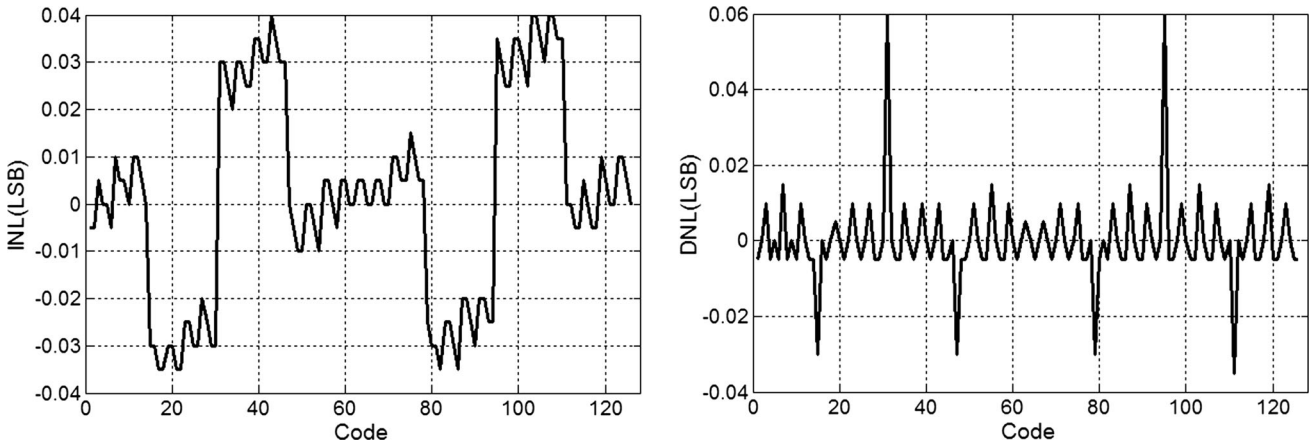


Fig. 4 Nonlinearity histogram of a 7-bit conventional SAR ADC

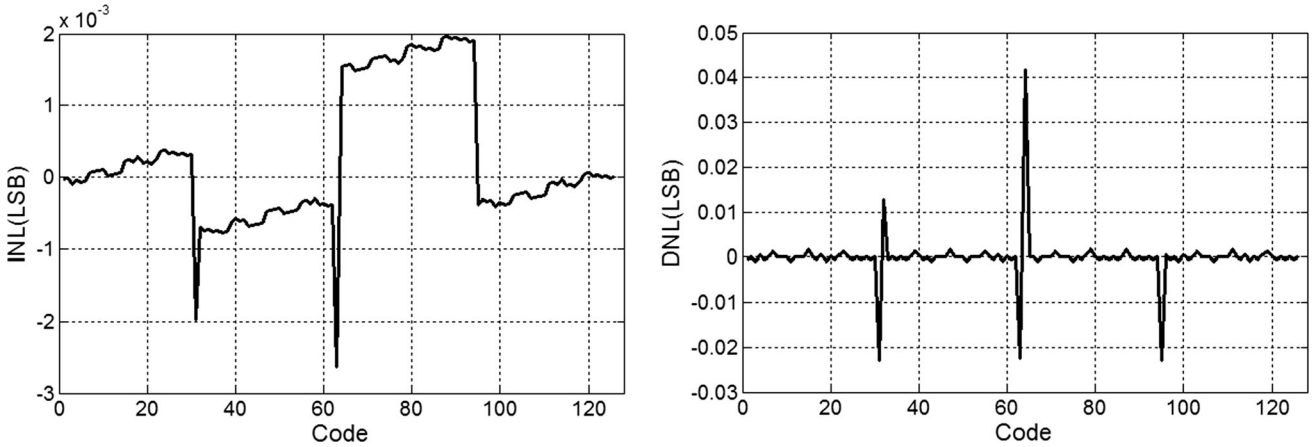


Fig. 5 Nonlinearity histogram of a 7-bit proposed ADC

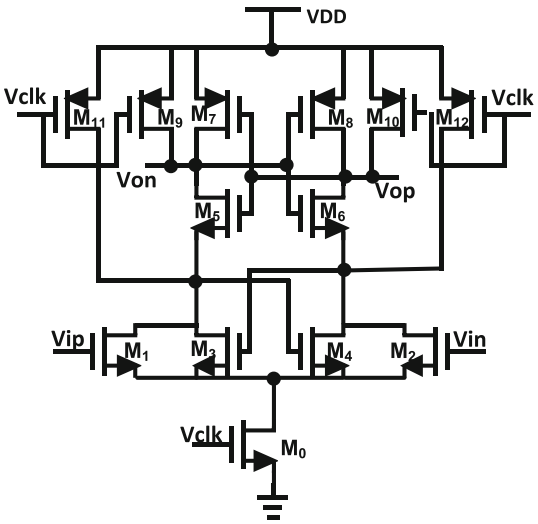


Fig. 6 Schematic of comparator [23]

implemented in binary weighted configuration, while the non-dominant capacitor array in the 2nd-stage can be implemented by binary weighted array with series capacitor to save area and reduce power consumption.

5 Circuit implementation

To evaluate performance of the proposed pipelining method, the ADC circuit have been designed and simulated in a 0.18-μm CMOS technology. As shown in Fig. 1, proposed ADC consists of different blocks being categorized as: comparators, capacitor arrays, SAR logics, main controller, analog de-multiplexers and multiplexers. Three latter blocks are used to control timing and operation of the overall proposed ADC; hence, their implementations are brought up together in this section as the controller.

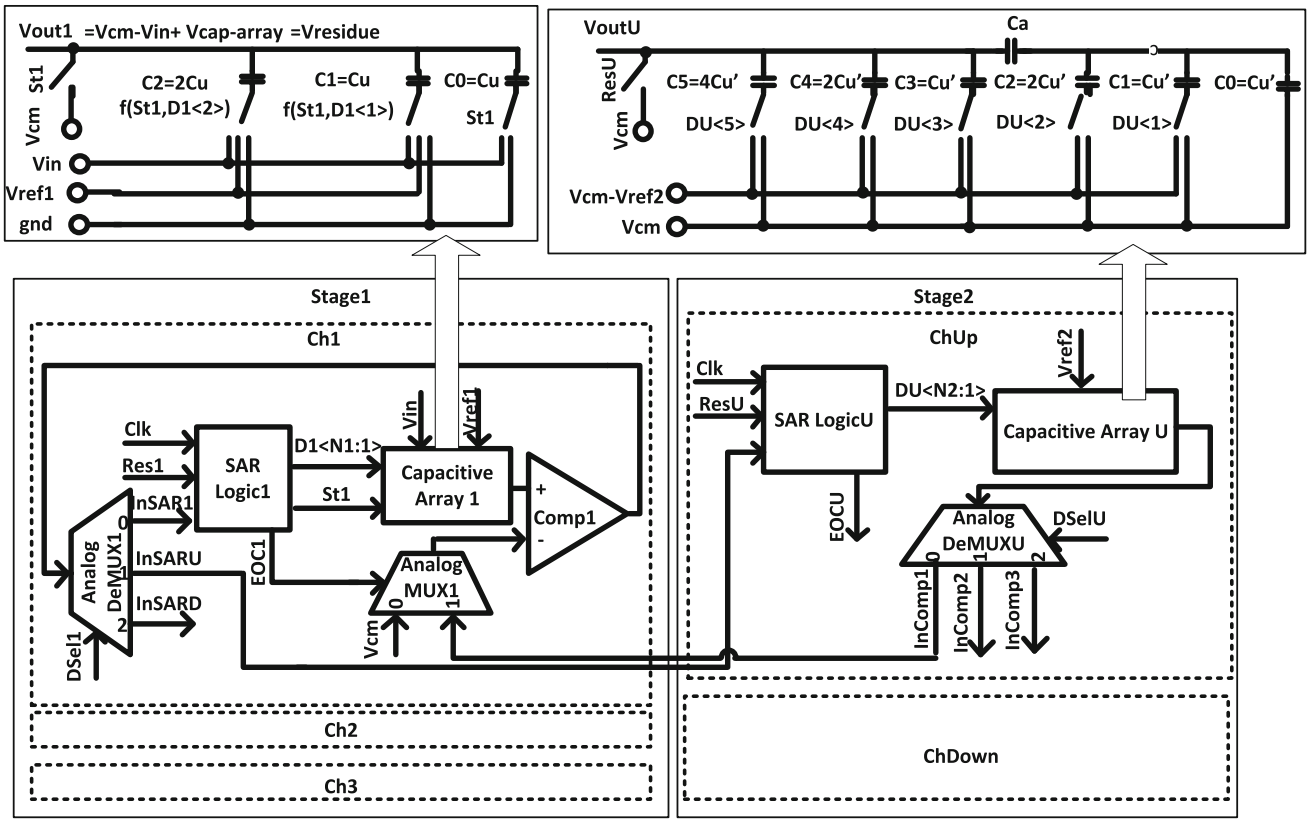


Fig. 7 Schematic of 1st-stage and 2nd-stagecapacitor arrays

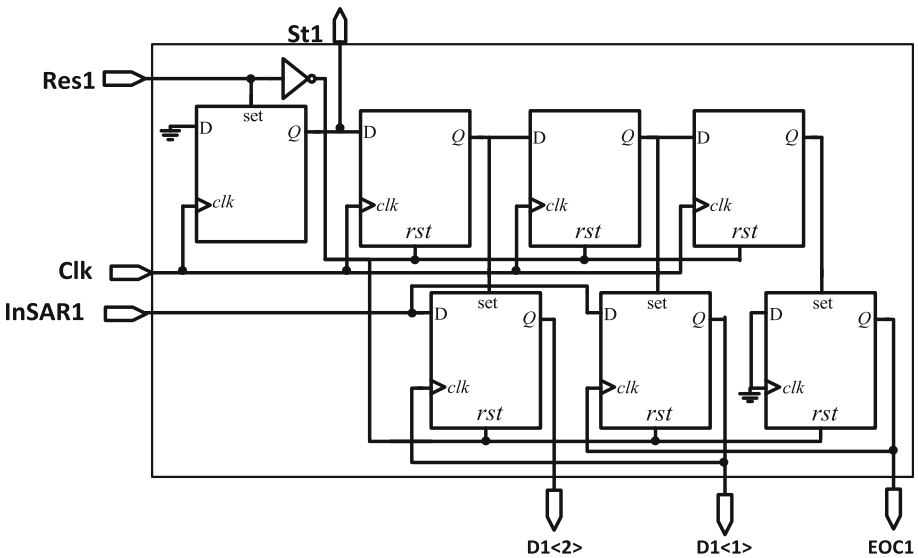


Fig. 8 Schematic of the SAR logic1

5.1 Comparators

Circuit schematic of the comparators is shown in Fig. 6 [23]. "Vip/Vin" and "Vop/Von" in Fig. 6 are the input and output nodes, respectively. It is a dynamic latch-comparator based on differential pair input stage along with one cross-coupled stage, inspired by "Lewis-Gray" dynamic comparator. Adjusting the transistor sizing resulted in a comparator with 2.1 mV offset, 456.92 ps delay at the frequency of 83.3 MHz while dissipating 125 μW from 1.2 V supply.

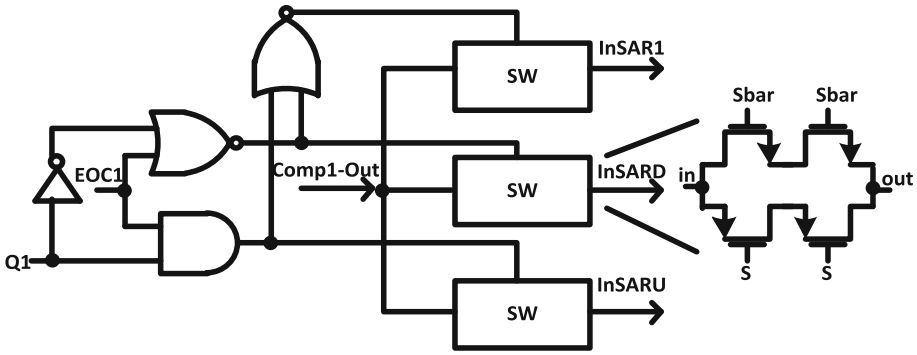


Fig. 9 Analog De-multiplexor of the channel 1

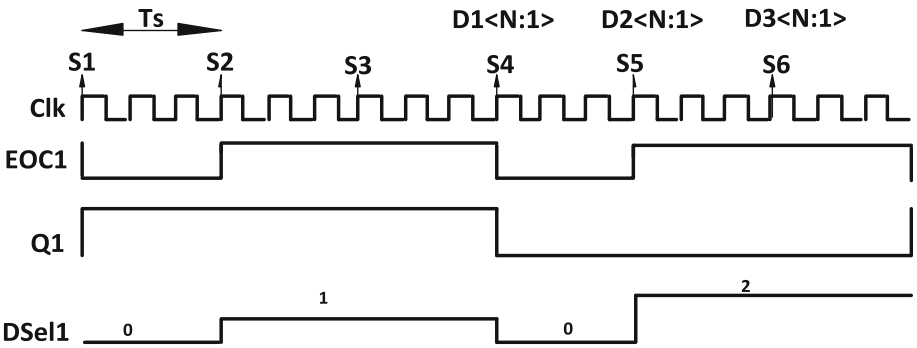


Fig. 10 Controlling signals of the Analog DeMUX1

5.2 Capacitor arrays

Capacitor arrays of the 1st-stage are employed for bottom plate sampling of input voltage, MSBs decision and storing residue voltage on their top plates for the rest of conversion cycle, while capacitor arrays of the 2nd-stage are utilized for conversion of the residue voltage to LSBs. As shown in Fig. 7, in a seven-bit ADC, digital to analog converter (DAC) of each channel at the 1st-stage and the 2nd-stage are two-bit conventional binary weighted capacitor array and 5-bit binary weighted capacitor array with an attenuator capacitor, respectively. With this arrangement, the total capacitance at the input of the comparator during the MSB conversion and the LSB conversion become equal. This reduces the error due to the parasitic capacitance at the input of the comparator. It also results in the same settling time at the two-bit and five-bit DACs in both stages and maximizes clock frequency. According the linearity analysis in Sect. 4, this implementation also saves area and improves power efficiency without degrading the linearity performance.

Size of the unit capacitor is chosen considering kT/C noise, capacitor matching [24], timing, area and power. To decrease period of the clock, area and power, the unit capacitor value should be as small as possible; while for improving noise and matching, it should be enlarged. To satisfy $\sqrt{\frac{kT}{C}} \leq \frac{V_{ref}}{2\times 2^7}$, for $V_{ref} = 1V$, and also considering capacitor matching limitation of 180 nm CMOS technology, unit capacitor of each stage must be greater than 40 fF; so the unit capacitor of the 2nd-stage is chosen to be Cu' = 50 fF to minimize the settling time and silicon area of the DAC. Both stages can have equal unit capacitors due to their same accuracy requirements; however for minimizing the effect of comparator's input parasitic capacitor, the total capacitance amount seen by each port of comparator, in the LSBs conversion phase, must be equal resulting in the unit capacitor of the 1st-stage to be Cu = 100 fF. Finally, total capacitance of each channel in both stages is equal to 400 fF.

5.3 SAR logics

Proposed ADC architecture with a resolution of seven-bit includes three two-bit and two five-bit SAR logics for the 1st-stage and the 2nd-stage channels, respectively. The SAR logic, which is commonly used in SAR ADCs, consists of ring counter and code registers [25]. Figure 8 shows the 2-bit SAR logic, "SAR Logic 1" in Fig. 1. The 5-bit SAR logic has similar architecture. The logic decides

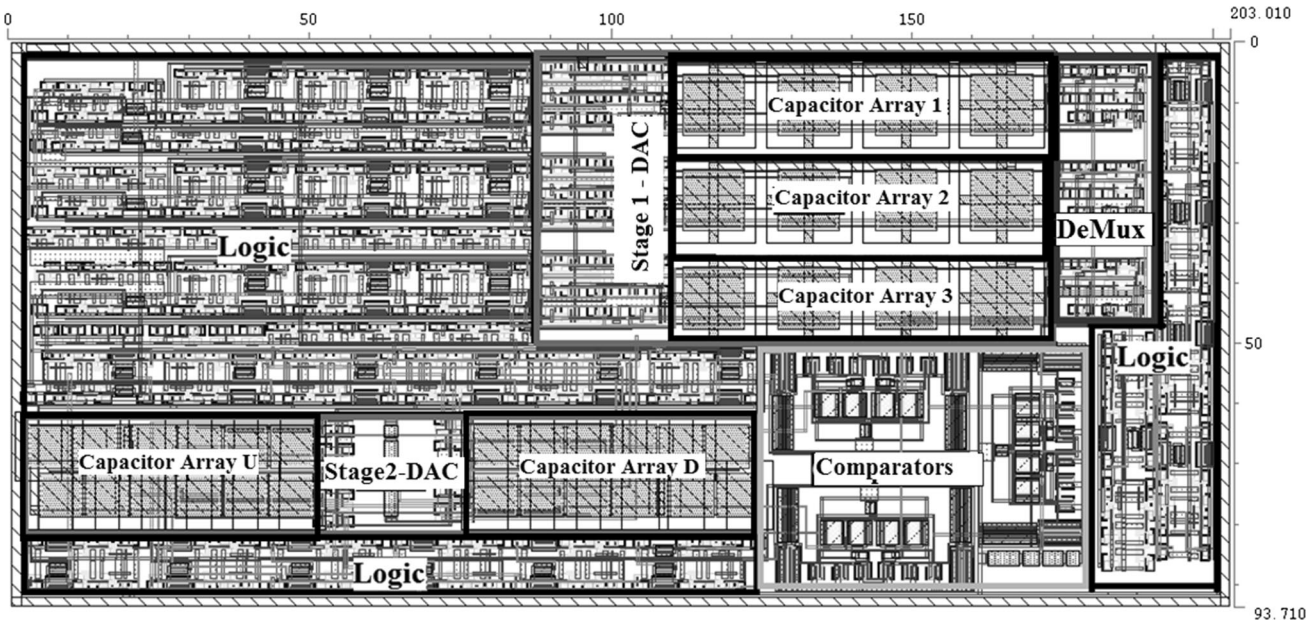


Fig. 11 Layout of the proposed ADC

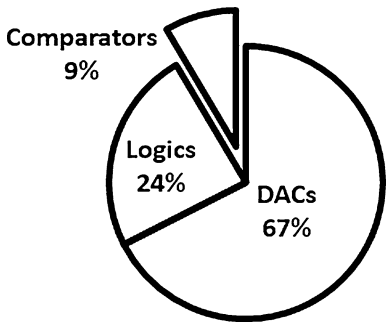


Fig. 12 Power dissipation of different blocks

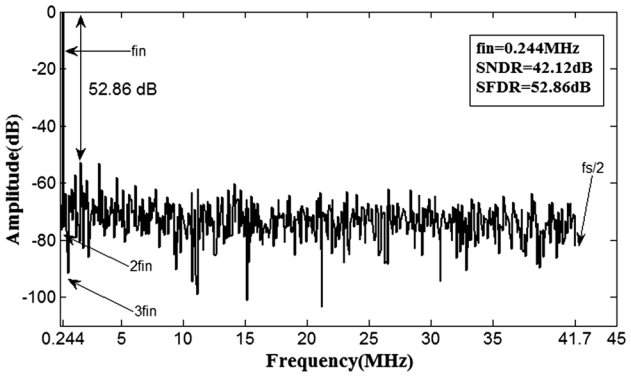
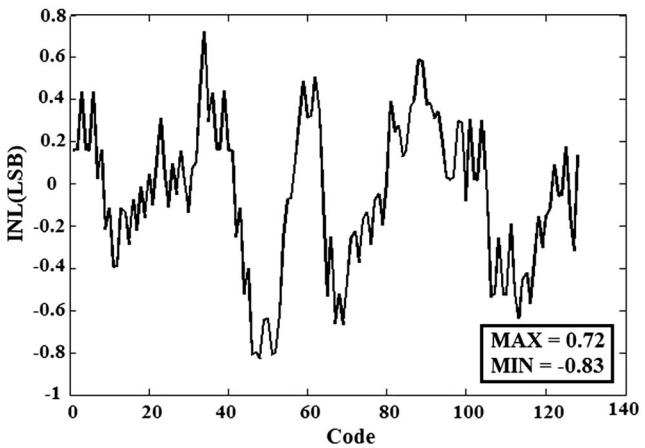


Fig. 14 ADC output spectrum at $f_{in} = \frac{f_s}{300}$



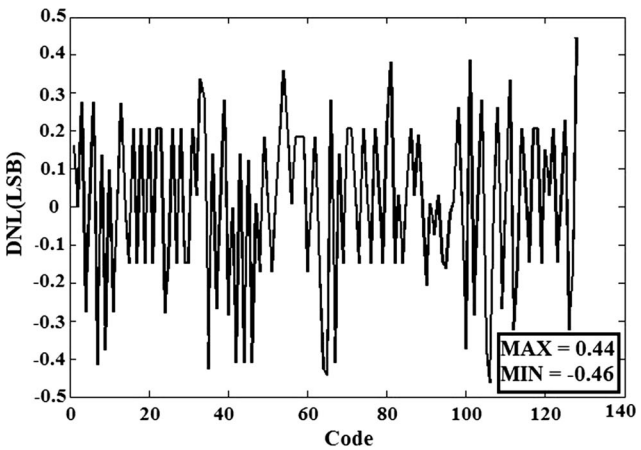


Fig. 13 INL and DNL of the proposed ADC

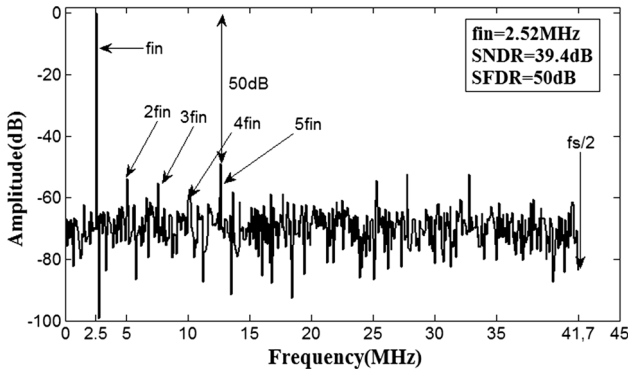


Fig. 15 ADC output spectrum at $f_{in} = \frac{f_s}{30}$

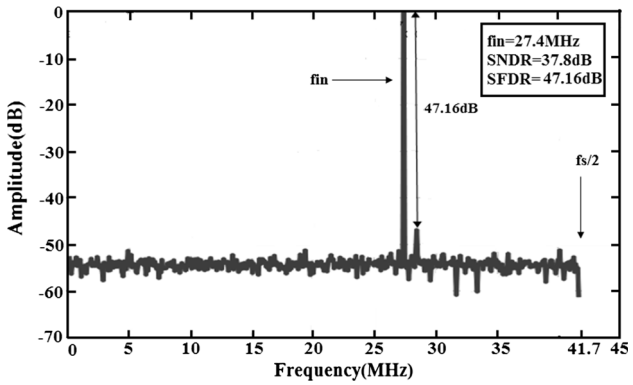


Fig. 16 ADC output spectrum at $f_{in} = \frac{f_s}{3}$

and saves the value of each bit, named "D1 ⟨2⟩" and "D1 ⟨1⟩" in Fig. 8, according to its input signals. The input signals include reset (Res1), clock (Clk) and the comparator output (InSAR1). EOC signal (EOC1) is also generated to show completion of the logic function.

5.4 Controller

Every block utilized to arrange operations of the channels is considered as a part of controller. Analog de-multiplexers of the 1st-stage channels, named "Analog Demuxi" in Fig. 1, are utilized for connecting the output of the ith channel comparator to the input of the SAR logic of either that channel or one of the second stage channels, according to the "Dseli" signal in Fig. 1. Similarly, analog de-multiplexers of second stage's channels, named "Analog Demuxj" in Fig. 1, are utilized for connecting the capacitor array of the corresponding channel to the positive input of one of the comparators of the 1st-stage through its analog multiplexer according to "Dselj" and "EOCi" signals. Both "Dseli" and "Dselj" are three-phase controlling signals, while "EOCi" is a two-phase signal

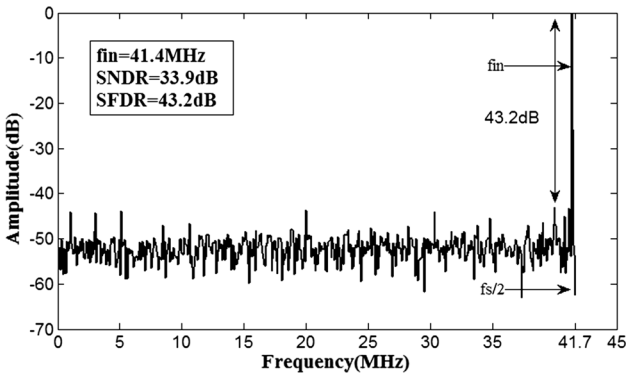


Fig. 17 ADC output spectrum at $f_{in} = \frac{f_s}{2}$

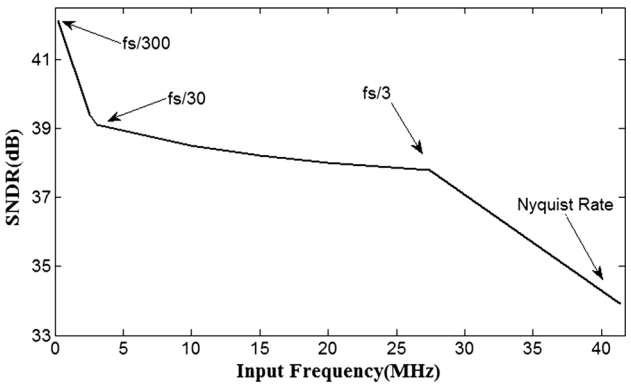


Fig. 18 SNDR versus input frequency at 83.3 MHz sampling frequency

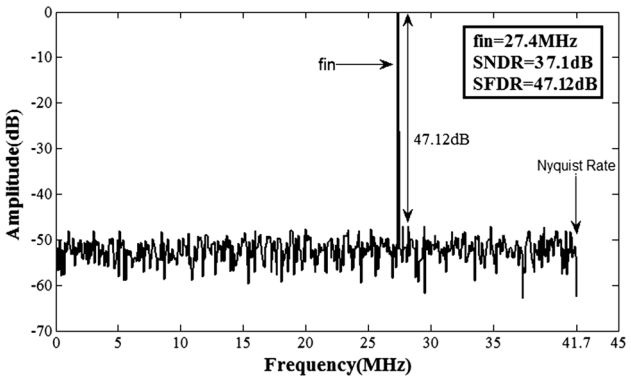


Fig. 19 ADC output spectrum at $f_{in} = \frac{f_s}{3}$ in presence of voltage supply noise

generated by the SAR logics. Instead of creating three-phase signals, all above blocks are implemented by switches that are controlled by a function of EOC signals and the main controller two-phase signals. Main controller also generates reset signals by some delay gates from main reset signal of the ADC.

For more clarification, schematic of analog de-multiplexer of channel one, named "Analog Demux1" in Fig. 1,

is shown in Fig. 9. It consists of three switches and some logic gates to create the select signals of the switches from the input signals, i.e. Q1 and EOC_1. Utilizing analog de-multiplexer for connecting the capacitive array of the 2nd-stage to the comparator of the 1st-stage can cause charge sharing between the auxiliary capacitive array and the parasitic capacitors of the analog de-multiplexer switches, resulting in gain error in the LSBs conversion phase. To reduce its impact, switches of the analog de-multiplexer are realized by transmission gate with lowered charge sharing and stack transistors with minimized leak currents during off phases [25]. As shown in Fig. 10, Q1 has a frequency of eighteen times slower than main clock signal and can be produced by common frequency dividers.

6 Post layout simulation results

A 7-bit model of the proposed ADC is designed in 180 nm CMOS process, and the layout is as shown in Fig. 11. Layout has occupied an area of about 0.0227 mm^2. To reduce channel mismatches, analog blocks are placed adjacent to each other. For reducing mismatch among capacitors, the binary weighted capacitors are placed in a common centroid configuration based on the proposed method in [26]. Capacitors would occupy half of the ADC area if capacitor arrays of the 2nd-stage were implemented by binary weighted configuration without series capacitor. Capacitors of TI channels are marked in Fig. 11.

Considering settling and delay time of all blocks, period of the clock signal equals 4 ns. This makes a sampling rate of $\frac{1}{12\text{ns}}$ for a seven-bit implementation possible. ADC dissipates total power of 4.56 mW from a 1.2 V supply voltage. As shown in Fig. 12, capacitor arrays of the ADC consumes 67 % of total power, which approves the assumptions in Sect. 3. As shown in Fig. 13, applying a very slow ramp to find the transmission points results in a DNL less than 0.44/−0.46 LSB and INL less than 0.72/−0.83 LSB. These errors occur due to the layout imperfections and parasitic capacitance of switches and comparators.

Figures 14, 15, 16, and 17 show the discrete Fourier transform (FFT) plot and dynamic performance of the ADC for different input frequencies, from $f_{in} \cong \frac{f_s}{300}$ up to Nyquist rate or $f_{in} \cong \frac{f_s}{2}$. The signal-to-noise-and-distortion (SNDR) versus the input frequency is also plotted in Fig. 18. SNDR is almost constant at a range of input frequency as shown in Fig. 18; as a result, SNDR equals 37.8 dB and the spurious-free-dynamic-range (SFDR) equals 47.16 dB_{FS} at a 27.4 MHz input frequency can be reported. Therefore, the effective number of bits (ENOB) is about 6 bits. Simulation results show SNDR degradation for higher input frequencies. This is mainly because higher input frequencies or faster slew rates degrade the SNDR for a specified clock jitter level; i.e. the high-frequency analog input has a larger error with respect to the clock jitter. Due to the extra switching action in the analog de-multiplexor of the proposed ADC, in comparison to a conventional SAR ADC, SNDR shows slightly more degradation for higher input frequencies. Transient simulation of the ADC circuit in presence of supply noise, with 100 μV RMS value, is performed by Spectre and the result is illustrated in Fig. 19. According to Fig. 19, SNDR of the ADC at 27.4 MHz input frequency is 37.1 dB, which shows 0.7 dB degradation compared to the simulation with ideal supply voltage in Fig. 16. Despite the use of single ended architecture, this small degradation is due to the pseudo-differential structure of employed comparator.

The FOM of the proposed ADC, defined as $\frac{P}{2\times f_s \times 2^{ENOB}}$ is 433 fJ/conversion step at a 27.4 MHz input with 83.3 MS/s

Table 2 ADC performance summary

Ref	Arch.	Tech (nm)	SR (MS/s)	P (mW)	VDD (V)	SNDR/ SFDR (dB)	Resolution/ ENOB (bits)	INL/DNL (LSB)	Area (mm^2)	FoM (fJ/conv-step)
*	This work	180	83.3	4.56	1.2	37.8/47.16	7/5.98	0.83/0.46	0.0227	433
[21]*	Conventional	180	20	2.36	1.8	43.2	8/6,88	0.65/0.68	0.105	530
[11]	Pipeline with MDAC replacement	65	200	11.5	1	57.6	12/9.28	1/1.25	0.26	46.25
[8]	Pipeline with inter-stage shared MDAC	65	110	11.5	1.2	61	12/9.84	1.63/0.421	0.12	57.04
[9]	Pipeline with inter-channel shared MDAC	65	204	9.15	1	55.2/63.5	10/8.88	+0.90/0.74	0.22	47.6
[12]	Pipeline with passive residue transferring	65	210	5.3	1	63.48	12/10.25	1.45/0.66	0.48	10.36
[18]*	Assisted pipeline with flash	45	100	6.1	1	51.94/65.87	9/8.33	0.66/0.94	0.068	94.78
[16]*	TI of SARs	65	250	1.2	1.2	28.3	5/4.4	–	2.3	113.7

* Post layout simulation results

rate of sampling. Simulation results of the proposed ADC and performance of some other reported ADCs, mentioned in Table 1, are summarized in Table 2. As the CMOS technology scales down, the power (P) decreases and the sampling rate (fs) increases; Due to this significant impact of utilized CMOS technology on the FOM of the realized ADCs, it is not intended to compare the reported FOMs in this paper. However, according to the superior efficiency of the proposed ADC than the other architectures in terms of speed, power and area in Table 1, better FOM is predicted for implementation of the proposed technology-independent ADC in the same utilized technology of Table 2 architectures.

7 Conclusion

The architectural basic of a low power data converter, implemented by a novel technique of pipelining in SAR ADCs with asymmetrical time interleaved stages has been presented. Systematic comparing of the proposed architecture with similar SAR structures, at the same sampling rate and resolution, shows its lower power consumption and smaller area. By employing the passive residue conversion and symphonic collaboration of stages in this architecture, a low power, high speed, and accurate converter can be achieved. In addition, in this architecture every signal sample experiences equal comparator offset during its conversion due to the applied novel operation sequence, without adding redundancy or comparator rotation scheme. Linearity of the proposed ADC has been also analyzed, demonstrating a better performance compared to the conventional SAR ADC. By considering raised non-idealities in circuit implementation, efficient realization for a seven-bit model of the proposed ADC with sampling rate of 83 MS/s has been designed and simulated in 180-nm CMOS technology. The post layout simulation verifications support the correctness of systematic comparison.

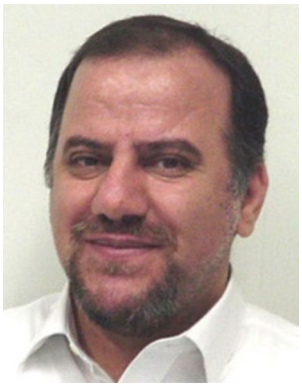
References

1. Damghanian, M., & Shamsi, H. (2014). Combination of DAC switches and SAR logics in a 720 MS/s Low bit successive approximation ADC. *Analog Integrated Circuits and Signal Processing, 80*, 263–272.
2. Khoshakhlagh, M., & Yavari, M. (2013). An efficient threshold voltage generation for SAR ADCs. Mixed signal letters. *Analog Integrated Circuits and Signal Processing, 75*, 161–169.
3. Zhangming Zhu, Yu., Xiao, L. X., Ding, H., & Yang, Y. (2013). An 8/10 bit 200/100MS/s configurable asynchronous SAR ADC. Mixed signal letters. *Analog Integrated Circuits and Signal Processing, 77*, 249–255.
4. Liang, Y., Zhu, Z., & Ding, R. (2015). SAR ADC architecture with 98.8% reduction in switching energy over conventional scheme. Mixed signal letters. *Analog Integrated Circuits and Signal Processing, 84*, 89–96.
5. Kuppambatti, J., & Kinget, P. R. (2014). Current reference precharging techniques for low-power zero-crossing pipeline-SAR ADCs. *IEEE Journal of Solid State Circuits, 49*(3), 581–594.
6. Wu, J.-J., Chang, S.-J., Lin, S.-H., Huang, C.-P., & Huang, G.-Y. (2014). Low power pipelined SAR ADC with loading free architecture. *IEEE, international symposium on VLSI design, automation and test (VLSI-DAT)*. doi:10.1109/VLSI-DAT.2014.6834906.
7. Huang, Y. C., & Lee, T. C. (2010). A 10b 100MS/s 4.5 mW pipelined ADC with a time sharing technique. *ISSCC Dig. Tech. Papers*. doi:10.1109/ISSCC.2010.5433927.
8. Wang, R., Chio, U.-F., Sin, S.-W., Seng-Pan, U., Wang, Z., & Martins, R. P. (2012). A 12-bit 110MS/s 4-stage single-opamp pipelined SAR ADC with ratio-based GEC technique. *Proceedings of the ESSCIRC*. doi: 10.1109/ESSCIRC.2012.6341336.
9. Jeon, Y.-D., Cho, Y.-K., Nam, J.-W., Kim, K.-D., Lee, W.-Y., Hong, K.-T., & Kwon, J.-K. (2010). A 9.15 mW 0.22 mm^2 10b 204MS/s pipelined SAR ADC in 65 nm CMOS. *Custom Integrated Circuits Conference (CICC)*. doi:10.1109/CICC.2010.5617457.
10. Jespers, P. G. A., et al. (1977). A fast sample and hold charge-sensing circuit for photodiode arrays. *IEEE Journal of Solid-State Circuits*. doi:10.1109/JSSC.1977.1050883.
11. Dolev, N., Kramer, M., & Murmann, B. (2013). A 12-bit, 200-MS/s, 11.5-mW pipeline ADC using a pulsed bucket brigade front-end. *Symposium on VLSI circuits digest of technical papers*, C98–C99.
12. Lin, C.-Y., & Lee, T.-C. (2014). A 12-bit 210-MS/s 5.3-mW pipelined-SAR ADC with a passive residue transfer technique. *Symposium on VLSI circuits digest of technical papers*. doi:10.1109/VLSIC.2014.6858452.
13. Lee, S., Chandrakasan, A. P., & Lee, H.-S. (2014). A 1GS/s 10b 18.9 mW time-interleaved SAR ADC with background timing-skew calibration. *IEEE international solid-state circuits conference*. doi:10.1109/ISSCC.2014.6757480.
14. Harpe, P., Busze, B., Philips, K., & de Groot, H. (2011). A 0.47-1.6mW 5bit 0.5-1GS/s time-interleaved SAR ADC for low-power UWB radios. *IEEE Journal of Solid State Circuits, 47*, 1594–1602.
15. Sin, S.-W., Ding, L., Zhu, Y., Wei, H.-G., Chan, C.-H., Chio, U-F., Seng-Pan, U., Martins, R. P., & Maloberti, F. (2010). An 11b 60MS/s 2.1 mW two-step time-interleaved SAR-ADC with reused S&H. *IEEE Proceedings of the ESSCIRC*. doi:10.1109/ESSCIRC.2010.5619890.
16. Ginsburg, B. P., & Chandrakasan, A. P. (2008). Highly interleaved 5-bit, 250-MSample/s, 1.2-mW ADC with redundant channels in 65-nm CMOS. *IEEE Journal of Solid-State Circuits, 43*(12), 2641–2650.
17. Sung, B. R. S., Cho, S.-H., Lee, C.-K., Kim, J.-I., & Ryu, S.-T. (2009). A time-interleaved flash-SAR architecture for high speed A/D conversion. *IEEE international symposium on circuits and systems, ISCAS*. doi:10.1109/ISCAS.2009.5117923.
18. Cho, Y.-K., Jung, J.-H., & Lee, K. C. (2012). A 9-bit 100-MS/s flash-SAR ADC without track-and-hold circuits. *IEEE, international symposium on wireless communication systems*. doi:10.1109/ISWCS.2012.6328494.
19. Gray, P. R., Hurst, P. J., Lewis, S. H., & Meyer, R. G. (2009). *Analysis and design of analog integrated circuits* (4th ed.). Wiley.
20. Saberi, M., Lotfi, R., Mafinezhad, K., & Serdijn, W. A. (2013). Analysis of power consumption and linearity in capacitive digital-to-analog converters used in successive approximation ADCs.

IEEE Transaction on Circuits and Systems-I: Regular Papers, 58, 1736–1748.
21. Atkin, E., & Normanov, D. (2014). Area-efficient low-power 8-bit 20-MS/s SAR ADC in 0.18 µm CMOS. PROC. *29th international conference on microelectronics*. doi:10.1109/MIEL.2014.6842188.
22. Zhu, Y., Chan, C.-H., Chio, U.-F., Sin, S.-W., Seng-Pan, U., Martins, R. P., & Maloberti, F. (2014). Split-SAR ADCs: Improved linearity with power and speed optimization. *IEEE Transaction on Very Large Scale Integration (VLSI) Systems, 22*(2), 372–383.
23. Rahman, L. F., Reaz, M. B. I., Yin, C. C., Ali, M. A. M. & Marufuzzaman, M. (2014). Design of high speed and low offset dynamic latch comparator in 0.18 µm CMOS Process. *PLoS One, 9*(10), e108634.
24. Meinerzhagen, P. (2008). *Design of a 12-bit low-power SAR A/D converter for a neurochip*. Master's Thesis, University of California, Lausanne, August 15, 2008.
25. Zhang, D., Bhide, A., & Alvandpour, A. (2012). A 53-nW 9.1-ENOB 1-kS/s SAR ADC in 0.13-m CMOS for medical implant devices. *IEEE Journal of Solid-State Circuits, 47*(7), 1585–1593.
26. Li, Y., Zhang, Z., Chua, D., & Lian, Y. (2014). Placement for binary-weighted capacitor array in SAR ADC using multiple weighting methods. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 33*(9), 1277–1287.

Ziba Fazel received the B.Sc. degree in Electrical Engineering from University of Tehran, Tehran Iran in 2012, and the M.Sc. degree from Sharif University of Technology, Tehran, Iran, in 2015, respectively. She is now working towards the Ph.D. degree in Sharif University of Technology. Her research interests include integrated circuits design for interface systems and data converters.

Saeed Saeedi received the B.Sc., M.Sc. and Ph.D. degrees in electrical engineering from Sharif University of Technology, Tehran, Iran in 2001, 2003 and 2010, respectively. He is currently an Assistant professor at Tarbiat Modares University, Tehran, Iran. His research interests include analog/RF integrated circuits for communication systems and high performance data converters.



Mojtaba Atarodi received his Ph.D. degree from the University of Southern California (USC) on the subject of analog IC design in 1993. He received the M.Sc. degree in electrical engineering from the University of California, Irvine, in 1987 and B.Sc. degree from Amir Kabir University of Technology in 1985. From 1993 to 1996 he worked with Linear Technology Corporation as a senior analog design engineer. He is currently a professor at Sharif University of Technology. His main research interests are integrated bioelectronics, RF/analog/mixed-signal ICs, and integrated circuits for digital TV receivers.