A 65 nm CMOS Wideband Radio Receiver With $\Delta\Sigma$-Based A/D-Converting Channel-Select Filters

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***Abstract*—This paper presents a wideband quadrature radio receiver employing $\Delta\Sigma$-based A/D-converting channel-select filters (ADCSFs). The output of the quadrature passive mixer is directly connected to the input of the ADCSFs, where a first-order $\Delta\Sigma$ modulator is incorporated into a fourth-order Butterworth channel-select filter (CSF) to provide sufficient dynamic range for a cellular system. A design methodology for the ADCSF is derived, where the transfer function of the CSF is preserved. The 65 nm CMOS receiver has a frequency range of 0.6–3.0 GHz and can be programmed to support the 2xLTE20, LTE20, and LTE10 bandwidths. The receiver noise figure varies from 2.3 to 3.9 dB, with a current consumption in 2xLTE20 mode between 33 mA at 0.6 GHz and 44 mA at 3.0 GHz from a 1.2 V supply, including 10–21 mA for LO phase generation and distribution. The SNDR is 47–51 dB at an LO frequency of 1.8 GHz.**

***Index Terms*—Channel-select filter, delta sigma modulator, filtering A/D converter, radio receiver, STF.**

I. Introduction

THE demanding requirements on the modern cellular radio receiver (RX) are increasing not only concerning bandwidth, power, and area consumption, but also the aggressive interferer rejection needed in communication standards such as LTE. Fig. 1(a) shows the architecture of a direct-conversion RX, where the RF front-end is operated in current mode. The low-noise transconductance amplifier (LNTA) performs voltage-to-current conversion and amplification, and its output current is fed to the passive quadrature mixer for frequency down-conversion. Thereafter, a transimpedance amplifier (TIA) boosts and converts the current-mode signal into voltage mode. Before final conversion into the digital domain, a low-pass channel-select filter (CSF) typically attenuates the interferers (both close-in and far-out), so that the dynamic range (DR) requirement on the analog-to-digital converter (ADC) is relaxed, ensuring a power-efficient implementation of the RX. A continuous-time (CT) $\Delta\Sigma$ modulator (DSM) is a favorable choice for the RX ADC, because of its robustness to circuit nonidealities and implicit anti-aliasing filtering [1].

Several recent works have targeted the codesign of CSF and DSM, to achieve an overall power and area reduction for the same functionality of the standard cascade of CSF and DSM. A possible approach is to embed the CSF within the DSM [2], [3], which relaxes the noise and linearity performance of the CSF, while the noise transfer function (NTF) of the DSM is unaffected by the embedded CSF.

A second approach, pioneered by Sosio et al. in [4], [5], and further developed in [6], [7], is the one adopted in this work and can be described as the dual of the first: the DSM is embedded inside the global feedback loop of the CSF [see Fig. 1(b)], with the advantage of an additional frequency shaping of the DSM noise by the CSF poles, thereby relaxing the quantization- and thermal-noise requirement on the DSM itself. Furthermore, by using a modest amount of gain in the first CSF integrator, the TIA can be incorporated into the CSF. Thus, the A/D-converting CSF (ADCSF) of Fig. 1(c) combines the functionalities of TIA, CSF, and ADC, improving at the same time power and (possibly) area consumption.

Embedding the ADC into the CSF introduces unavoidable extra phase shifts on the signal path, originating: 1) from the digital-to-analog conversion (DAC) in the feedback path of the ADCSF and 2) from the fact that the signal transfer function (STF) of the DSM is not equal to unity in general. Such phase shifts alter the CSF pole locations, and re-tuning of the CSF coefficients becomes necessary to restore the desired CSF STF. A design method accounting for DSM DAC delays has been developed in [7]. In that work, however, the DSM STF was still assumed to be unity, and this assumption is closer to reality for lower-order DSMs, which are therefore to be preferred in the context of ADCSF design.

In this paper, which is an extended version of [8], we present a single-ended RX where a wideband LNTA is followed by a current-mode quadrature passive mixer directly connected to two identical ADCSFs, one for each I/Q path. With respect to the filtering ADC presented in [7], the ADCSF in this paper exhibits a better behaved STF thanks to the use of a simpler first-order (instead of second-order) DSM. It also displays a stronger frequency selectivity, a higher ADCSF signal-to-noise-and-distortion ratio (SNDR), and a

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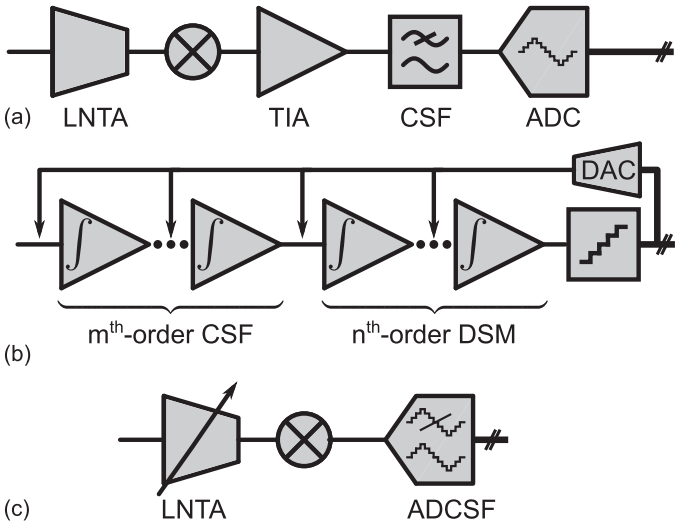

Fig. 1. (a) Direct-conversion RX with cascaded TIA, CSF and ADC. (b) Simplified view of an ADCSF with an nth-order DSM embedded into an mth-order CSF. (c) ADCSF-based direct-conversion RX.

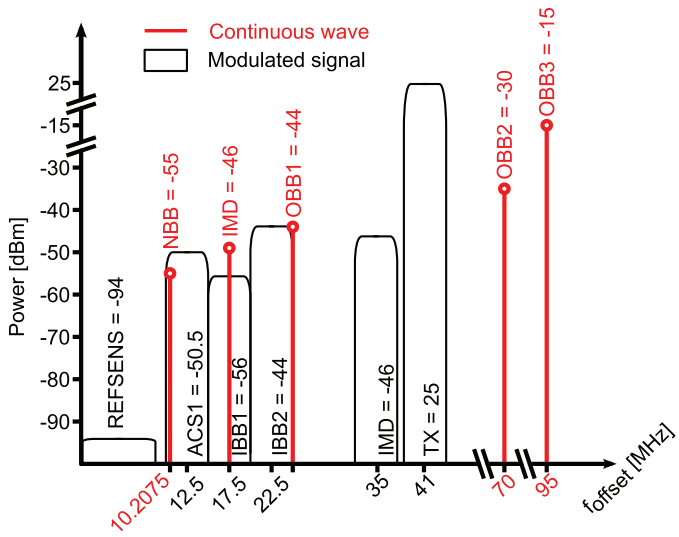

Fig. 2. Typical blocker power levels at the antenna port for LTE20 with the most stringent scenario on REFSENS, ACS, and duplex distance among the LTE bands.

better figure-of-merit (FoM). Compared to the RXs in [9]–[11], this RX achieves a lower noise figure, lower power consumption, and more aggressive filtering to attenuate adjacent channels.

This paper is organized as follows. Section II presents an overview of the RX design and discusses the interferer (blocker) profile. The design strategy for ADCSF synthesis is discussed in Section III, and the circuit implementations of both RF front-end and ADCSF are detailed in Section IV, followed by the measurement results for the stand-alone ADCSF (Section V) and for the whole RX (Section VI). Finally, conclusions are drawn in Section VII.

II. System Overview

We target a wideband receiver that can be used for multiple RF bands. The RX does not utilize harmonic rejection, since an antenna filter (in TDD mode) or a duplexer (in FDD mode) is assumed to reject far out-of-band (OOB) signals at the odd harmonics of f_{LO}. A wideband single-ended-to-differential LNTA with tunable transconductance, providing variable gain, drives the quadrature current-mode passive mixer, as shown in Fig. 1(c). The down-converted signal is then processed by the ADCSFs, delivering the digital quadrature signal for further processing in the digital baseband. As already discussed, the ADCSF incorporates the functionalities of TIA, CSF, and ADC. The ADCSF provides a transimpedance of 10kΩ, resulting in a nominal overall RX voltage gain of 50 dB, calculated from LNTA input to differential ADCSF output. The RX bandwidth can be configured to support LTE10, LTE20, or two contiguously aggregated LTE20 channels (2xLTE20).

One of the main challenges in RX design is to handle the weak desired channel in the presence of strong interferers. Typical test cases defined by 3GPP [12] for LTE20 are shown in Fig. 2, with frequency offset f_{offset} from the carrier frequency. The reference sensitivity (REFSENS), which refers to the minimum power level of the in-band (IB) signal to be detected at the antenna port, may be as low as −94 dBm. For LTE, REFSENS assumes a QPSK modulation with a code rate of 1/3, yielding a signal-to-noise ratio (SNR) requirement of approximately −1 dB for 95% of the maximum achievable throughput [13]. The RX sensitivity at room temperature (300 K) is defined as [13]

$$P_{\text{sens}}[\text{dBm}] = -174 + 10\log_{10}(BW_{\text{RF}}) + \text{NF} + \text{SNR} - 3 \quad (1)$$

where BW_{RF} is the RF channel bandwidth, NF is the noise figure of the RX, and a 3 dB diversity gain is assumed (according to the 3GPP LTE specifications). With a 2 dB duplexer attenuation from antenna to RX port, NF should be at least lower than 9 dB, but, in commercial state-of-the-art implementations, NF is close to 3 dB. Together with a weak desired signal, interferers (modeled as either continuous waves or modulated signals with a 5 MHz bandwidth) may be present at various frequencies, which may desensitize the RX. Test cases related to the interferers include narrow-band blockers (NBB), adjacent channel selectivity (ACS), IB blockers (IBB), out-of-band blockers (OBB), intermodulation distortion (IMD) and transmitter (TX) leakage. The TX power can be as high as +25 dBm at the antenna, yielding a TX port output power of +27 dBm, assuming 2 dB of duplexer attenuation from TX port to antenna. This TX power is attenuated at the RX input by some 55 dB provided by the duplexer [14] in an FDD scenario, which means that a TX leakage close to −28 dBm appears at the RX input. Furthermore, as the duplex distance from RX to TX may be as small as 41 MHz in band 20 (LTE20 mode), or even 30 MHz in bands 12, 14, and 17 (LTE10 mode), the TX leakage is one of the most critical blockers to be handled by the RX.

The closest blockers (i.e., those relative to the NBB and ACS specifications), on the other hand, can not be attenuated by the duplexer, as they are located inside the desired RX band. A CSF is instrumental in rejecting the TX leakage and far-out blockers, but has a somewhat limited effect on close-in

blockers; therefore, the (close-in) RX DR is mainly determined by the moderate suppression of NBB and ACS. A pessimistic DR estimation, i.e. without considering the relaxed requirement on REFSENS when blockers are present, is approximately ACS - REFSENS = 45 dB. In the RX presented here, the targeted close-in DR is in the vicinity of 50 dB, to provide some margin for the high peak-to-average ratio (PAR) of modulated OFDM interferers and, especially, to accommodate more than one interferer in a real-life application.

III. ADCSF Design Considerations

A. RX SNDR and ADCSF SQNR

One of the key parameters in the ADCSF synthesis is its signal-to-quantization-noise ratio (SQNR). The ADCSF SQNR requirement can be derived from the RX specifications introduced in the previous section. In order to achieve an RX NF of 3 dB, the noise floor P_N at the RX input in LTE20 mode should be $P_N = -174 + 10\log_{10}(\mathrm{BW_{RF}}) + \mathrm{NF} \approx -98$ dBm. With a differential full-scale voltage of $\pm$600 mV for the DSM quantizer and an RX gain of 50 dB, an input signal of -45 dBm produces 0 dBFS at the RX output. To avoid clipping in the DSM quantizer, we further assume that the maximum RX SNDR occurs at a -3 dBFS output (i.e. for an input-referred signal power of $-45 - 3 = -48$ dBm). The resulting IB RX SNDR is then easily calculated as $(-48) - (-98) = 50$ dB. To ensure that most P_N is contributed by the RF front-end, the noise floor of the ADCSF should be at least 10 dB lower than P_N. Furthermore, in a power-efficient DSM design (in our case, ADCSF design), the quantization noise should be at least 10 dB lower than the thermal noise [15]. Thus, the SQNR of the ADCSF should be at least 70 dB.

The filtering constraints on the ADCSF, on the other hand, can be deduced from the blocker profile described in the previous section. If NBB and ACS test cases are to dominate the ADCSF DR requirement, interferers from other test cases, together with the TX leakage, must be sufficiently attenuated before entering the DSM, and thus an aggressive filtering is called for. The tradeoff between sensitivity and selectivity of the ADCSF is dealt with in Section III-D.

B. ADCSF Versus DSM Order

To highlight the importance of the DSM order, a general model of an ADCSF (Fig. 3) is used, where the overall STF $\mathrm{STF_{ADCSF}}(s) = V(s)/U(s)$, is

$$\mathrm{STF_{ADCSF}}(s) = \frac{L_{F0}(s)\mathrm{STF_{DSM}}(s)}{1 - L_{F1}(s)\mathrm{DAC}_F(s)\mathrm{STF_{DSM}}(s)} \quad (2)$$

Obviously, the nature of $\mathrm{STF_{DSM}}$ may have a large impact on $\mathrm{STF_{ADCSF}}$. Fig. 4(a) and (b) show the simplified designs of first- and second-order CT DSMs, straightforwardly derived from their discrete-time counterparts MOD1 and MOD2 [15]. The internal quantizer is modeled as an ideal sampler with a sampling frequency f_s of 296 MHz, corresponding to the case when the ADCSF is operated in LTE20 mode, and non-return-to-zero (NRZ) DACs are used. The allocated time delay, T_d, between quantizer and feedback DAC is set to half of the sampling period, while the nominal DSM NTF is restored by the addition of a direct feedback path k_0 around the quantizer. The magnitude and phase responses of $\mathrm{STF_{DSM}}$ are shown in Fig. 5 for a zeroth-order, a first-order, and a second-order DSM (where the zeroth-order DSM is a simple flash ADC). When the order of the DSM is decreased from second to first, the phase lag is reduced by approximately 30° at 50 MHz. The direct path k_0 would require an extra summer before the quantizer. To save power, one commonly used alternative is to insert a zero in the last integrator [16], turning it into a proportional-integral (PI) component, as shown in Fig. 4(c), where the path formed by k_{pi} and a_1 is equivalent to k_0 in Fig. 4(b). Additionally, the feedforward path k_{pi} introduces a zero in $\mathrm{STF_{DSM}}$, which extends the flatness of STF_{DSM} and reduces its phase shift (Fig. 5). As can be understood from (2), the magnitude variations and phase shifts of $\mathrm{STF_{DSM}}$ alter $\mathrm{STF_{ADCSF}}$; therefore, a low-order DSM, such as the first-order DSM of Fig. 4, is preferred to achieve a robust $\mathrm{STF_{ADCSF}}$. One further step in DSM simplification is avoiding a DSM loop filter altogether, reducing the DSM to a simple flash ADC, with $\mathrm{STF_{DSM}} = 1$ at all frequencies (assuming that $\mathrm{DAC_D}$ in Fig. 3 is not necessary in this case). This would be the perfect DSM choice for the ADCSF, were it not for the lack of quantization noise shaping in such a DSM. Nevertheless, it will be shown later that an ADCSF with zeroth-order DSM is a perfectly viable choice, if the SNDR and the filtering profile of the ADCSF are not too stringent.

In the following, we will refer to an $m - n$ ADCSF when the CSF section of the ADCSF is mth-order, and the DSM section

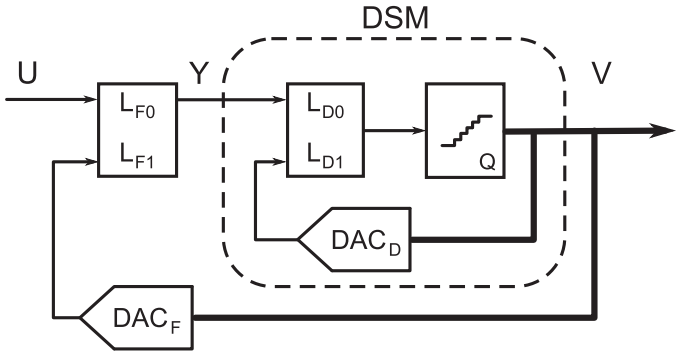

Fig. 3. General model of an ADCSF. As clear from Fig. 1(b), $\mathrm{DAC_F}$ and/or $\mathrm{DAC_D}$ may represent several feedback paths.

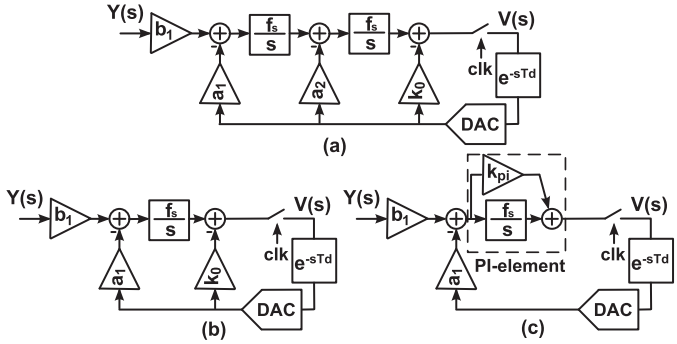

Fig. 4. Schematic models of a (a) second-order DSM, (b) first-order DSM, and (c) first-order DSM with PI element.

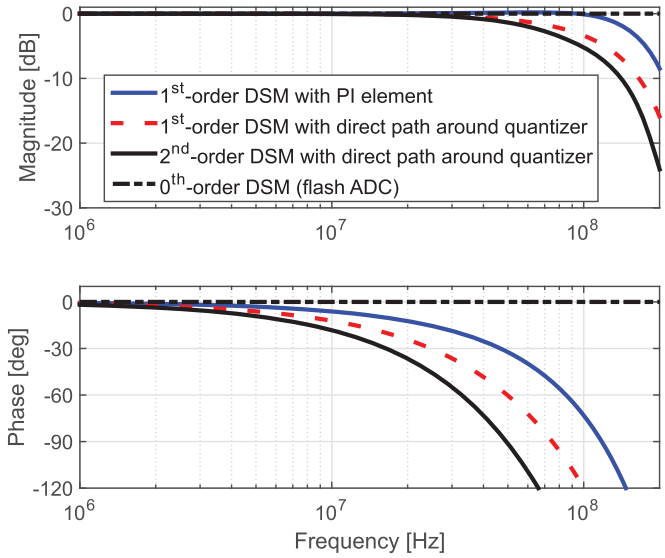

Fig. 5. Magnitude and phase responses of $\mathrm{STF}_{\mathrm{DSM}}$.

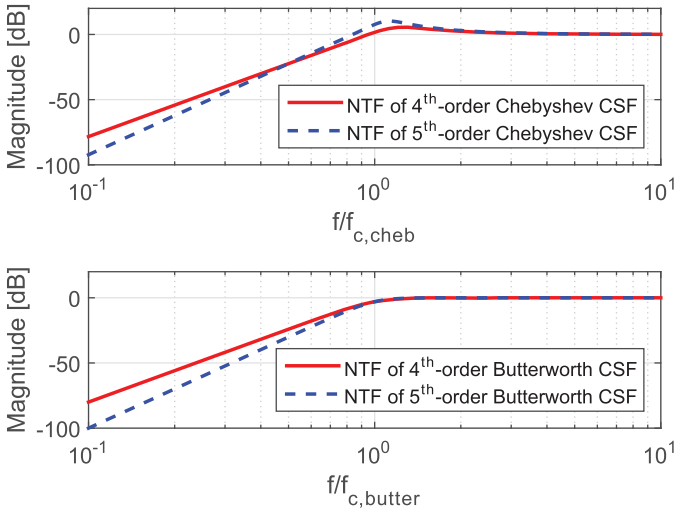

Fig. 6. NTFs of Chebyshev CSFs (top) and Butterworth CSFs (bottom); $f_{c,\mathrm{cheb}}$ is the last 0 dB-crossing of the Chebyshev STF, while $f_{c,\mathrm{butter}}$ is the -3 dB bandwidth of the Butterworth STF.

is nth-order. Thus, a 2-2 ADCSF was presented in [4], a 2-3 ADCSF in [6], and a 3-2 ADCSF in [7].

C. ADCSF Versus Order and Type of CSF

As the order of the DSM is reduced, the suppression of its quantization noise relies heavily on the NTF of the CSF portion of the ADCSF (in the same way as in a conventional DSM, the CSF NTF is defined as the transfer function of a noise source located at the output of the last CSF integrator). Because both STF and NTF share the same poles, and the CSF poles are determined entirely by the desired filtering action of the CSF, the in-band noise suppression afforded by the CSF is closely related to the choice of filter type and filter order, and crucially to the ratio r_{CSF} of CSF cutoff frequency f_c to channel (signal) bandwidth f_{sig}[5].

The conventional DSM design usually benefits from an increase in the order of the loop filter, as long as stability is ensured. This is, however, not always the case for the ADCSF. Fig. 6 shows the NTF magnitude response of a CSF with a Chebyshev Type I STF and a Butterworth STF. The frequency is normalized to the CSF cutoff frequencies $f_{c,\mathrm{cheb}}$ and $f_{c,\mathrm{butter}}$, where $f_{c,\mathrm{cheb}}$ is the last 0 dB-crossing of the Chebyshev STF, while $f_{c,\mathrm{butter}}$ is the -3 dB bandwidth of the Butterworth STF. As the filter order increases from fourth to fifth, the Chebyshev NTF peaking increases and moves closer to the band limit, degrading the noise suppression (which may, in fact, even become a noise boost). In contrast, the Butterworth noise suppression keeps increasing when the filter order increases. In all cases, quantization-noise suppression can be enhanced, as in a conventional DSM design, by judiciously placing NTF zeros across the CSF bandwidth, without affecting the CSF STF.

D. Selectivity Versus Sensitivity

We have already mentioned that the tradeoff between CSF selectivity and DSM noise suppression in the ADCSF is a strong function of the parameter r_{CSF}. Fig. 7 depicts the achievable SQNR versus r_{CSF} for a 4-1 ADCSF and a 5-0 ADCSF making use of Butterworth CSFs, with a DSM oversampling ratio of 16 and a 3-bit DSM quantizer in both cases. As r_{CSF} increases, the achievable SQNR increases as well, indicating a higher quantization noise suppression for a reduced selectivity [5], [17]. A suitable value of r_{CSF} can be chosen from the plots in Fig. 7, based on the overall system requirements. In the case of the 5-0 ADCSF, the DSM itself can only provide an SQNR of 32 dB, and to reach the required SQNR of 70 dB, $r_{\mathrm{CSF}} > 1.8$ is needed, which results in a rather poor attenuation of close-in interferers. Therefore, a 4-1 ADCSF is adopted with $r_{\mathrm{CSF}} \approx 1.36$, to achieve the required SQNR with only a minor deterioration in close-in selectivity. As shown in Fig. 8, in this case the 4-1 ADCSF yields an additional DSM noise suppression of 23 dB, boosting the overall SQNR to 72 dB compared to the 49 dB of the conventional CSF-DSM cascade,

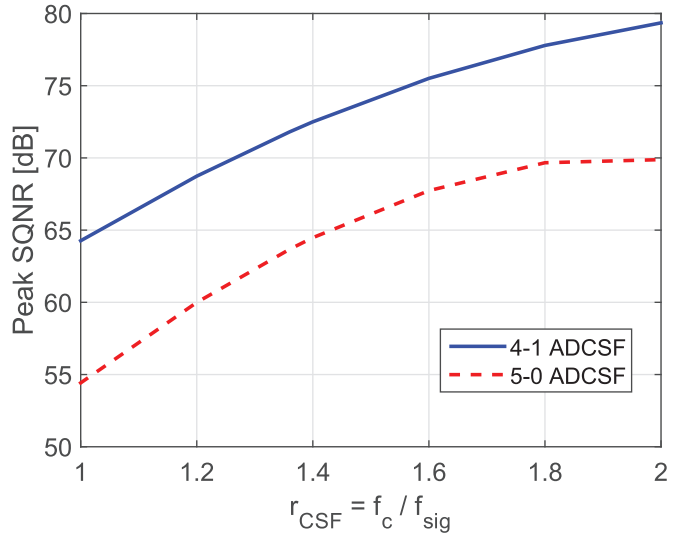

Fig. 7. Achievable SQNR with a 4-1 ADCSF with fourth-order Butterworth CSF (top), and with a 5-0 ADCSF with fifth-order Butterworth CSF (bottom).

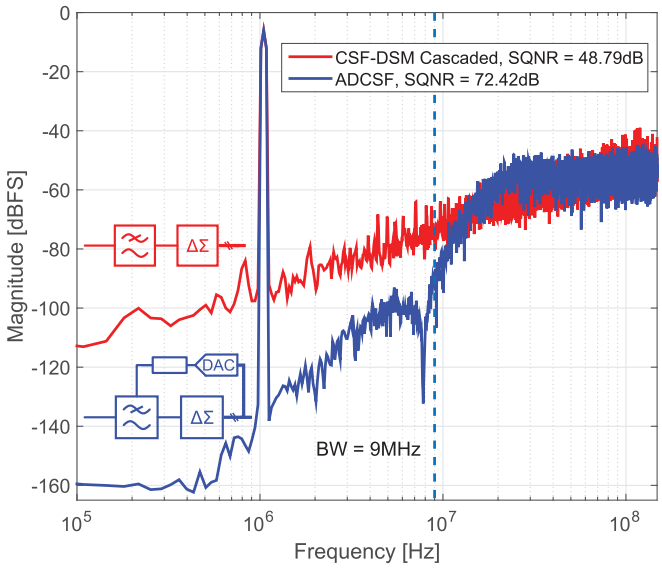

Fig. 8. Simulated quantization-noise spectra for 4-1 ADCSF (blue), and standard CSF-DSM cascade (red). The two designs implement the same STF.

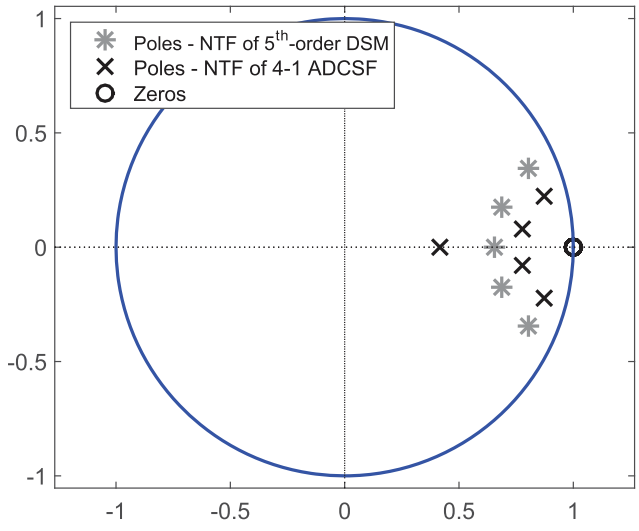

Fig. 9. Pole-zero plots for a 4-1 ADCSF and a conventional fifth-order DSM.

while the STF remains unaffected. As a final remark, and still assuming $r_{\mathrm{CSF}} \approx 1.36$, we point out that a 3-1 ADCSF would still yield a sufficient selectivity, but an SQNR of only 67 dB.

E. ADCSF Versus Conventional DSM

As already done in [7], it is worth pointing out that the $m-n$ ADCSF of Fig. 1(b) may be topologically identical to a conventional $(m+n)$th-order DSM. In fact, this is the case for the implemented 4-1 ADCSF described in Section IV-B.

There is, however, an essential difference between ADCSF and conventional DSM, i.e., the placement of the respective poles: in the ADCSF, it reflects a tradeoff between IB quantization-noise suppression and OOB blocker filtering, while only the former is relevant in a conventional DSM.

As an example, Fig. 9 shows the z-domain pole-zero plots of the NTFs of a 4-1 ADCSF and a conventional fifth-order DSM. Both NTFs are maximally flat and with a gain of 6 dB

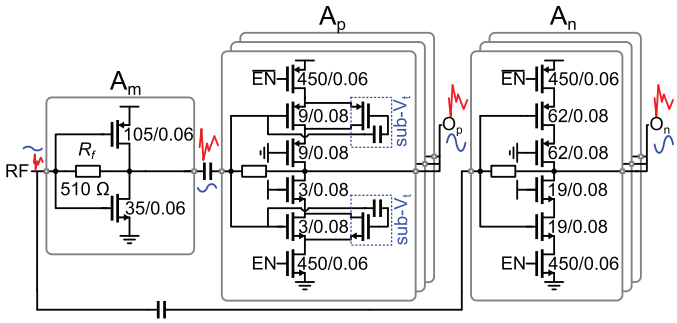

Fig. 10. Wideband, shunt-feedback, noise-canceling, single-ended-to-differential LNTA.

at very high frequencies, and all zeros have been kept at DC for simplicity. In the conventional fifth-order DSM, all five poles are placed at high frequencies to aggressively minimize the IB quantization noise, but they cannot provide any filtering close to baseband. In the 4-1 ADCSF, on the other hand, four low-frequency CSF poles (mainly) perform filtering and one high-frequency DSM pole accomplishes a first-order shaping of the quantization noise, which, most importantly, is further suppressed by the four low-frequency CSF poles. The conventional fifth-order DSM provides a much lower IB quantization noise than the ADCSF, since its poles are optimized for noise performance, but this, besides the lack of filtering, is an unnecessary overkill: the key advantage of the ADCSF is not that its CSF poles implement an optimal noise shaping, but rather that they offer a substantial additional noise shaping almost for free, without deteriorating the filtering capability of the ADCSF.

IV. RX Implementation

A. RF Front-End

With the introduction of a larger number of frequency bands in LTE, it is important that the RF front-end be flexible, with a topology that can be easily matched to a suitable duplexer or antenna filter for any given scenario. Furthermore, absence of inductors in the LNTA is desirable to reduce the area, and the number of LNTA inputs should be minimized, favoring a single-ended topology.

To provide a wide frequency range of operation, a wideband noise-canceling LNTA based on a shunt-shunt feedback was implemented, as shown in Fig. 10. The first part of the LNTA consists of the voltage-mode amplifier $\mathrm{A_m}$, which provides wideband impedance match to the source impedance R_s by means of the feedback resistance R_f, provided the condition $|A_v| = R_f/R_s - 1$ is satisfied, with $|A_v|$ the voltage gain of $\mathrm{A_m}$ (here set to 5). The output voltage of $\mathrm{A_m}$ is fed to a bank of transconductance cells, $\mathrm{A_p}$, implemented with inverter-based cascode stages that can be enabled or disabled. This bank performs voltage-to-current conversion and delivers an output current in phase with the LNTA voltage input, with a total gain of

$$G_{m,\mathrm{main}} = \left(1 - \frac{R_f}{R_s}\right)(-G_{mp}) \tag{3}$$

where $-G_{mp}$ is the total transconductance of $\mathrm{A_p}$. In parallel to $\mathrm{A_m}$ and $\mathrm{A_p}$, a second bank, $\mathrm{A_n}$, with a total transconductance of G_{mn} is employed. Implemented in the same way as $\mathrm{A_p}$, $\mathrm{A_n}$ produces a current in phase opposition to the LNTA input; thereby, single-ended to differential signal conversion can be achieved at the LNTA output. The differential output is balanced when the gain of $\mathrm{A_n}$ is identical to (3), i.e., when

$$G_{mn} = G_{m,\mathrm{main}} = \left(1 - \frac{R_f}{R_s}\right)(-G_{mp}). \tag{4}$$

The LNTA also cancels the channel noise produced by the transistors in $\mathrm{A_m}$ [18]–[20]. In fact, a noise source v_n at the $\mathrm{A_m}$ output is amplified by $\mathrm{A_p}$ before reaching the LNTA output $\mathrm{O_p}$; the same v_n, attenuated by the factor $1 + R_f/R_s$, is also found at the LNTA input, and is subsequently amplified by $\mathrm{A_n}$ before reaching $\mathrm{O_n}$. Since the resulting noise at $\mathrm{O_n}$ has the same polarity as the fully correlated noise at $\mathrm{O_p}$, their overall impact is greatly attenuated by the common-mode rejection of the quadrature mixers and ADCSFs. Optimal noise cancelation occurs when the condition

$$\frac{G_{mn}}{G_{mp}} = \frac{R_f}{R_s} + 1 \tag{5}$$

is fulfilled.

Assuming ideally balanced signals and perfect common-mode suppression, the LNTA noise factor is

$$\begin{aligned} F = 1 &+ \frac{4R_f(r_{om}G_{mp}(R_sG_{mm}+1)+R_sG_{mn})^2}{R_s(r_{om}R_sG_{mm}+r_{om}+R_f+R_s)^2(G_m)^2} \\ &+ \frac{4r_{om}^2\gamma G_{mm}((R_f+R_s)G_{mp}-R_sG_{mn})^2}{R_s(r_{om}R_sG_{mm}+r_{om}+R_f+R_s)^2(G_m)^2} \\ &+ \frac{4r_{om}((R_f+R_s)G_{mp}-R_sG_{mn})^2}{R_s(r_{om}R_sG_{mm}+r_{om}+R_f+R_s)^2(G_m)^2} \\ &+ \frac{4\gamma G_{mp}}{R_s(G_m)^2} + \frac{4\gamma G_{mn}}{R_s(G_m)^2} \end{aligned} \tag{6}$$

where $G_m = (1 - R_f/R_s)(-G_{mp}) + G_{mn}$ (i.e., G_m is the total gain of the LNTA), r_{om} is the output impedance of A_m, and G_{mm} is the transconductance of A_m. Assuming r_{om} is large, the input impedance of the LNTA is equal to $1/G_{mm}$; further assuming ideal impedance matching, i.e., $1/G_{mm} = R_s$, (6) can be simplified as

$$\begin{aligned} F = 1 &+ \frac{4R_fG_{mp}^2}{R_sG_m^2} + \frac{\gamma G_{mm}((R_f+R_s)G_{mp}-R_sG_{mn})^2}{R_sG_m^2} \\ &+ \frac{4\gamma G_{mp}}{R_sG_m^2} + \frac{4\gamma G_{mn}}{R_sG_m^2}. \end{aligned} \tag{7}$$

When (5) is fulfilled, the second fraction in (7) is nulled, and F is determined only by R_f and the noise contributions from $\mathrm{A_p}$ and $\mathrm{A_n}$. However, since the conditions for balanced signals (4) and noise cancelation (5) cannot be satisfied at the same time, a tradeoff must be made between the two, based on the value of G_{mn}. From Fig. 11, where (6) is plotted as a function of G_{mn}, it is clear that the value of G_{mp} enforcing perfectly balanced outputs does not coincide with the value for minimum

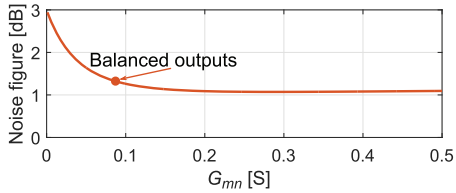

Fig. 11. LNTA NF versus G_{mn}, according to (6).

NF; the NF deterioration, however, is only 0.2 dB. It should be noted that, due to the actual values of the various LNTA components, NF is almost constant with an increasing G_{mn}. If the noise sources in $\mathrm{A_p}$ and $\mathrm{A_n}$ are removed, however, a clearly distinguishable NF minimum appears for a G_{mn} value close to that yielding balanced signals. To maintain a high second-order linearity in presence of unavoidable mismatches in the double-balanced passive mixers, the design of the LNTA is optimized for balanced outputs, accepting the 0.2 dB NF increase. Furthermore, in order to reduce the noise contribution from R_f while achieving a good compromise between input matching and noise, R_f is slightly increased beyond its value for optimal input matching. The simulated LNTA transconductance from the single-ended input to each differential output is 80 mS. The final simulated NF is below 1.6 dB for a total LNTA current consumption of 10 mA from 1.2 V.

In order to increase the third-order linearity of the LNTA, limited by $\mathrm{A_p}$ due to the relatively large voltage swing at its input, derivative superposition linearity enhancement is used, enabled by MOS transistors operated in sub-threshold and placed in parallel to the main transistors of $\mathrm{A_p}$ [21], as shown in Fig. 10. This ensures a simulated input-referred third-order intercept point (IIP3) of approximately 0 dBm. The bias voltages for the sub-threshold transistors are chosen to provide optimum IIP3 close to compression, and are generated through an on-chip resistive voltage division. On-chip calibration is required to secure the robustness of the linearity improvement. By disabling some of the $\mathrm{A_n}$ and $\mathrm{A_p}$ cells, the gain of the LNTA can be decreased in steps of 3, 6 or 12 dB, providing gain control at RF.

To deliver quadrature LO phases to the quadrature mixer, the current-mode frequency divide-by-2 circuit from [22] is used, producing 25% duty-cycle phases at f_{LO} from a differential oscillation at $2f_{\mathrm{LO}}$. By using AND gates driven both by f_{LO} and $2f_{\mathrm{LO}}$ signals, low-phase-noise LO phases were generated [23]. The LO phases are then buffered and fed to the quadrature mixer, whose nMOS switch size is 20/0.06 μm.

B. Analog Baseband

The schematic of the ADCSF used in each of the two I/Q paths is shown in Fig. 12. As we have already disclosed, the ADCSF consists of a fifth-order continuous-time loop filter, a 3-bit flash quantizer, and 5 NRZ feedback DACs. The loop filter is implemented by five active-*RC* integrators, which provide better linearity compared to their $\mathrm{G_m}$-C counterparts, and the overall cascade-of-integrators-in-feedback topology avoids STF peaking [2]. Resistive DACs were preferred to current-steering ones because of their lower thermal noise [24]. The

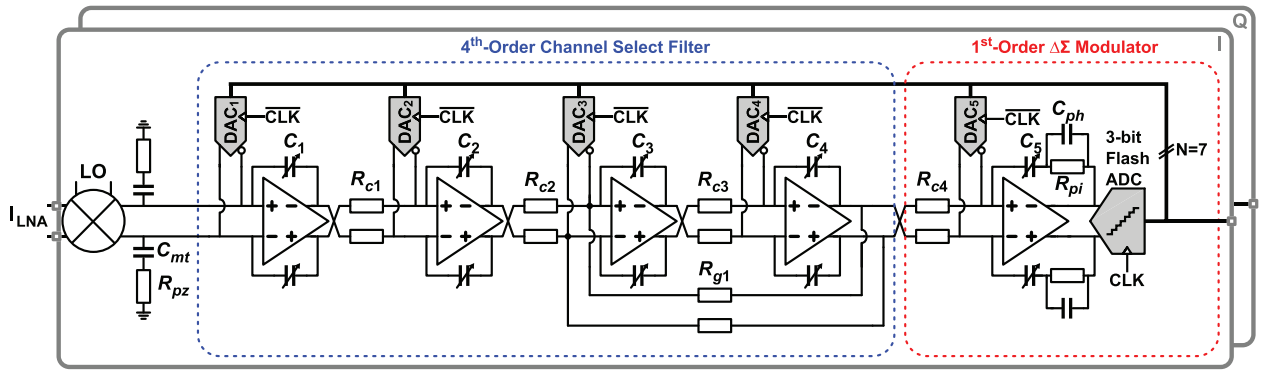

Fig. 12. ADCSF with fourth-order Butterworth CSF and first-order DSM.

ADCSF channel bandwidth is tunable to 4.5 MHz (LTE10 mode), 9.0 MHz (LTE20 mode) and 18.5 MHz (2xLTE20 mode) by programming the integration capacitors while scaling the sampling frequency to maintain an oversampling ratio of 16. Furthermore, all capacitors can be fine-tuned with a 4-bit word to account for process variations. The total RX gain at the differential output of either I or Q path is 50 dB in nominal conditions, set by the product of LNTA+mixer transconductance and DAC_1 resistance. To enable a high OOB linearity, 10 pF shunt capacitors have been added after the mixers (Fig. 12), together with 25 Ω series resistors to enhance the stability of the first ADCSF integrator (an issue treated in detail in Section IV-C).

As discussed in Section III, the ADCSF is partitioned into a 4-1 topology, where the first 4 integrators implement a fourth-order Butterworth CSF, while a first-order DSM is implemented by the last integrator. As in a standard DSM design, resistance R_{g1} introduces a resonance close to the bandwidth limit of the received signal [15], locally boosting the ADCSF loop gain to minimize the in-band power of the quantization noise (see Fig. 8). It may be worth noticing that, once again, we use the (boosted) gain of the CSF section of the ADCSF to further suppress the noise from the ADCSF DSM.

The ratio r_{CSF} is set to be 1.36 to secure a good tradeoff between CSF filtering and CSF noise suppression. DR scaling at the internal nodes allocates 48 dB of the total 50 dB of gain to the first integrator, ensuring an insignificant noise contribution from the following integrators while still guaranteeing a sufficient linearity of the first integrator.

The OOB gain of the DSM NTF is close to 6 dB in order to aggressively push quantization noise out-of-band, resulting in a DSM SQNR of 49 dB. The DSM loop delay, including the fixed half sampling period DAC delay, the finite switching DAC speed, and the finite gain-bandwidth product (GBW) of the integrators, is compensated by inserting resistor R_{pi} in series with C_5. A phantom zero, created by C_{ph} in parallel with R_{pi}, is introduced for phase margin enhancement. Finally, to account for the quantizer/DAC delays in the feedback loop of the ADCSF, a recalculation of the CSF coefficients is performed to restore the correct $\mathrm{STF}_{\mathrm{ADCSF}}$ [7], followed by an additional and post-layout fine tuning. Table I presents both ideal (i.e., without delays of any sort in the ADCSF) and post-layout-adjusted component values for the ADCSF.

TABLE I
COMPONENT VALUES FOR THE ADCSF

Component	Ideal Value	Post-layout-adjusted Value
R_{c1}	3.94 kΩ	1.95 kΩ
R_{c2}	2.50 kΩ	2.50 kΩ
R_{c3}	6.74 kΩ	6.74 kΩ
R_{c4}	4.35 kΩ	4.39 kΩ
R_{g1}	12.8 kΩ	13.0 kΩ
$R_{DAC1}{}^*$	10 kΩ	10 kΩ
$R_{DAC2}{}^*$	5 kΩ	5 kΩ
$R_{DAC3}{}^*$	3.27 kΩ	6.29 kΩ
$R_{DAC4}{}^*$	9.68 kΩ	14.7 kΩ
$R_{DAC5}{}^*$	8.69 kΩ	8.75 kΩ
R_{pi}	2.17 kΩ	2.26 kΩ
C_1	2.09 pF	4.98 pF
C_2	1.92 pF	3.89 pF
C_3	2.4 pF	2.4 pF
C_4	500 fF	550 fF
C_5	388 fF	388 fF
C_{ph}	44 fF	44 fF

$^*R_{DACn}$: Equivalent differential output resistance of DAC_n

C. OTA Frequency Compensation

The operational transconductance amplifiers (OTAs) in Fig. 12 are two-stage amplifiers with a differential input stage and an AC-coupled push-pull common-source output stage [6]. A simplified schematic of the first integrator, together with mixer and mixer termination, is shown in Fig. 13(a). The current-mode mixer is terminated with capacitors C_{mt} to provide a low impedance at the virtual-ground node for OOB signal, thereby improving the mixer linearity. There is a tradeoff, though, between the OTA GBW and the impedance at the mixer output: as C_{mt} loads the OTA input, GBW is degraded, causing the OTA input impedance to increase earlier than otherwise.

The amplifier is stabilized in differential mode mainly by resistor R_{pz}, without degrading the mixer linearity noticeably. R_{pz} introduces a zero

$$z_1 = \frac{-1}{C_{mt}R_{pz}} \tag{8}$$

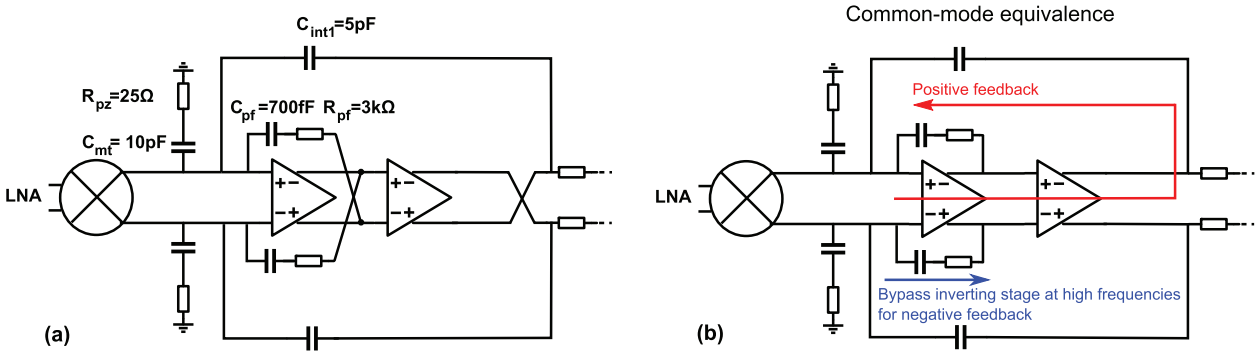

Fig. 13. (a) Schematic view of the first ADCSF integrator. (b) Equivalent circuit for common-mode signals.

near the unity loop-gain frequency, resulting in a phase margin of 64° at 1 GHz. For comparison, a Miller compensation with the same phase margin achieves a GBW of only 500 MHz. A positive-feedback compensation (PFC) is also implemented, by means of C_{pf} and R_{pf}. Compared to the PFC in [6], resistor R_{pf} is added, in order to add a degree of freedom in placing the phase-advancing zero at a suitable frequency, to mitigate the GBW loss caused by C_{pf}.

As a matter of fact, the main purpose of C_{pf} and R_{pf} here is not differential-mode PFC, but rather standard negative-feedback compensation for common-mode stability, which is also impaired by the large capacitance at the mixer output. While negative feedback in differential mode is achieved by cross-coupling the signal path, as explicitly shown at the output of the second inverting OTA stage in Fig. 13(a), a common-mode signal is not inverted by the same cross coupling. The two inverting stages are therefore cascaded without common-mode signal inversion, causing a positive-feedback loop via the integrator capacitors, as shown in the common-mode equivalent circuit of Fig. 13(b) [25], [26]. The positive loop can be suppressed with an additional strong common-mode feedback (CMFB) loop and a sufficient common-mode rejection in the differential input stage of the OTA. Achieving a high common-mode rejection, however, becomes increasingly difficult in nm CMOS processes, due to reduced voltage headroom for the tail current source of the differential input stage, while a high-gain and wide-band CMFB is power consuming.

Our solution to improve common-mode stability is to use a CMFB with sufficient gain at low frequencies, and to bypass the first inverting OTA stage at high frequencies, thereby enforcing negative feedback instead of positive. The bypass is performed by the differential-mode PFC, which in common-mode introduces a non-inverting path, as illustrated in Fig. 13(b). To show the effectiveness of the PFC, a simulation of the common-mode loop gain with and without PFC has been performed (Fig. 14). The internal CMFB of the OTA dominates at low frequencies, with a 43 dB gain at DC. When the PFC path is enabled, the phase margin improves from $-5°$ to 67°, stabilizing the common mode. The PFC is therefore instrumental in preventing harmful positive common-mode feedback. The PFC technique is only used in the first OTA, since the remaining OTAs are not loaded by the output capacitance of the mixer.

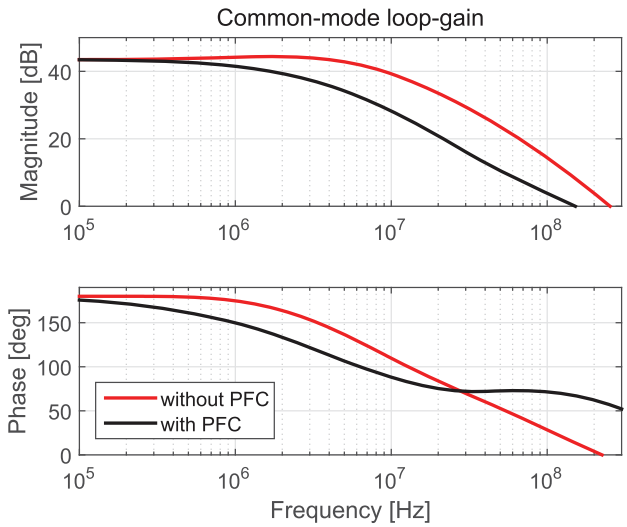

Fig. 14. Amplitude (top) and phase (bottom) response of the common-mode loop gain for the amplifier in Fig. 13.

V. Stand-alone ADCSF Measurement Results

The RX has been manufactured in STMicroelectronics 65 nm CMOS process. The ADCSFs can be programmed to interface either to the output of the quadrature mixers for regular operation, or to a 1 kΩ differential resistor, mimicking the output resistance of the mixer, for testing purposes. In the latter configuration, the differential input of the ADCSF is terminated with a 50 Ω off-chip resistance per side to provide matching to the signal generator. The stand-alone ADCSF displays a voltage gain of 20 dB, and Fig. 15 shows the measured ADCSF spectrum in 2xLTE20 mode with a -3.5 dBFS output tone at 1 MHz. The SNR/SNDR are 62/60 dB, very close to the simulated values of SNR/SNDR of 63/61 dB, and in line with the ADCSF requirement derived in Section III-A. The second-order and third-order harmonic distortions are -86 dBc and -70 dBc. The OOB IIP3 is 35 dBm, measured with two tones at 40 MHz and 80 MHz to capture the stringent half-duplex test case. The OOB input-referred second-order intercept point (IIP2) is 82 dBm. Assuming an RX gain of 50 dB, the OOB IIP3 and IIP2 are 5 dBm and 52 dBm respectively when referred to the RX input. Fig. 15 also shows both ideal (fourth-order Butterworth) and measured ADCSF STF in 2xLTE20 mode, normalized to 0 dB passband gain. The discrepancy between

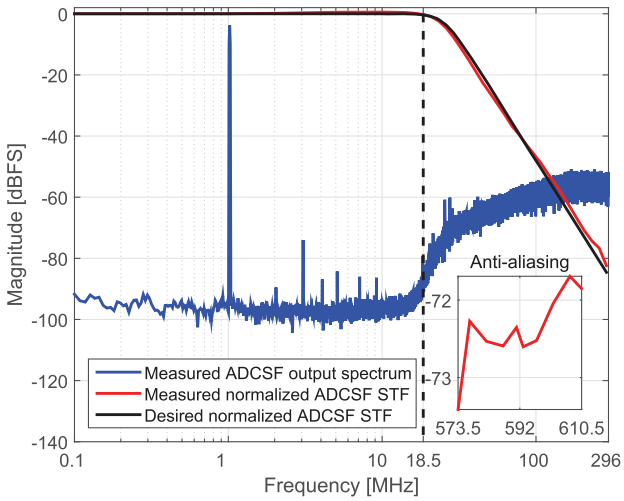

Fig. 15. Measured ADCSF output spectrum with a −3.5 dBFS output tone, and ADCSF STFs in 2xLTE20 mode.

the two STFs is less than 0.5 dB in the passband, and less than 2 dB OOB up to $f_s/2$, which is a significant improvement compared to e.g. the ADCSFs described in [6] and [7]. It should be appreciated that the ADCSF provides an amount of filtering already at the first adjacent channel, thanks to the low value of r_{CSF} discussed in Section III-D. The anti-alias ADCSF response is −72 dB in 2xLTE20 mode, and increases to −90 dB in both LTE10 and LTE20 modes. To benchmark the ADCSF performance in terms of DR, noise and linearity, we adopt two FoMs often used for both filters and filtering ADCs (where the ADCSF is, of course, a filtering ADC), given by

$$\mathrm{FoM1} = \frac{P}{(2^{(DR-1.76)/6.02} \cdot 2 \cdot BW)} \tag{9}$$

and

$$\mathrm{FoM2} = \frac{P}{N \cdot BW \cdot 10^{2/3 \cdot (\mathrm{IIP3} - P_{\mathrm{noise}})/10}} \tag{10}$$

where P is the total power consumption, $P_{\mathrm{noise}} = 10\log_{10}(IRN^2 \cdot BW)$ is the input-referred noise in dBV_{rms} integrated over the channel bandwidth BW, IRN is the input-referred noise power spectral density, and N is the number of filter poles. FoM1 is the Walden FoM [27], where the OOB (instead of IB) DR is used to account for filtering. The DR is measured at four times the BW, where the worst-case TX leakage is assumed to be located. FoM2, on the other hand, is frequently used when evaluating filters [28], and includes both noise and third-order intermodulation distortion performance. The ADCSF achieves a FoM1 of 22.7 fJ/conversion and a FoM2 of 3 aJ. The ADCSF performance is summarized in Table II and compared with recently published filtering ADCs. The ADCSF displays a higher filter order, the lowest OOB FoM2, and high FoM1 and OOB IIP3 when gain is accounted for.

VI. RX Measurement Results

Manufactured in STMicroelectronics 65 nm CMOS process, the pad-limited die measures 2 ×1 mm^2, and has an active area of 0.7 mm^2 (see Fig. 16). Four additional pads for testing the stand-alone ADCSF are clearly visible close to the middle of the circuit. Dies have been wire-bonded to FR-4 printed circuit boards (PCBs) and measured. Thanks to the single-ended LNTA, no external balun was needed at the RF input. The PCB/cable/combiner losses have been de-embedded in all measurements to follow, which have been taken at maximum RX gain.

The RX is powered by 6 different 1.2 V supply domains, to allow the measurement of the current consumption for the individual blocks. The LNTA current is 10.0 mA, while the LO input buffer, divider, and distribution consume between 9.6 mA and 20.6 mA, depending on the LO frequency. The ADCSFs, I and Q together, consume 10.0/11.1/13.6 mA for LTE10/LTE20/2xLTE20, including clock buffering and distribution. A sinusoid at $2f_{\mathrm{LO}}$ was provided by an Agilent E8257D, from which differential signals were generated by a Marki BAL-0006 and fed to the LO divider. The ADCSF outputs, buffered by differential on-chip LVDS drivers, were sampled by an Agilent 16902B logic analyzer. Finally, the data was post-processed in MATLAB.

TABLE II
ADCSF Versus Other Filtering ADCs

Parameter	This work	[7]	[29]	[3]
fs (MHz)	**592**	576	1036	256
BW (MHz)	**18.5**	18.5	18.3	2
SNDR (dB)	**60**	56.4	57.9	74.4
Filter order	**4**	3	3	2
Avg. IRN in BW ($\mathrm{nV}/\sqrt{\mathrm{Hz}}$)	**6.0***	5.1	–	40**
Gain setting (dB)	**20**	26	–	0
Out-of-band IIP3 ($\mathrm{dBV}_{\mathrm{rms}}$)	**22**	20	–	34**
IM3 Two-Tone test offset (MHz)	**40,80**	60,120	–	4.75,10.5
f_{-3dB} (MHz)	**25.2**	25.0	–	4
Power (mW)	**8.2**	7.9	14.3	5
Tech. (nm)	**65**	65	28	130
Vdd (V)	**1.2**	1.2	1.1	1.4
DR at BW×4 (dB)	**81.5**	82	78.6	90.5
FoM1 at BW×4 (fJ/c.)	**22.7**	21	78	45
FoM2, OOB IIP3 (aJ)	**3**	4	–	15

*Incl. off-chip matching resistance.
**Calculated from data in [3].

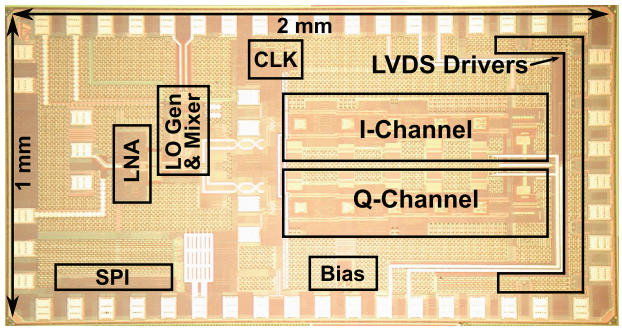

Fig. 16. Die photograph of the RX, with a core area of 0.7 mm^2.

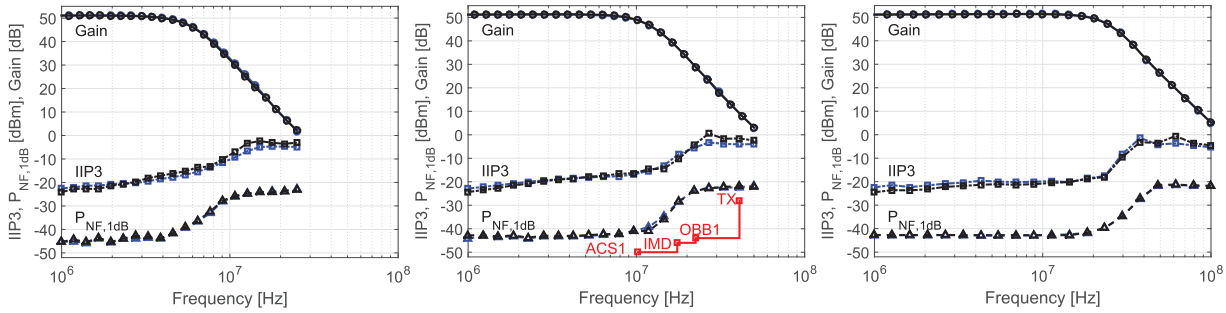

Fig. 17. STF, $\mathrm{P_{NF,1dB}}$, and IIP3 of the RX in LTE10 (left), LTE20 (middle) and 2xLTE20 (right) mode, with an LO of 1.778 GHz.

The RX performance versus baseband frequency is presented in Fig. 17 for the 3 different LTE bandwidths at the mid-band LO frequency of 1.776 GHz, measured at a positive frequency offset. In order to select the different bandwidths, the value of the ADCSF integration capacitors was changed via a serial-to-parallel digital interface, and the ADCSF sampling frequency f_s, generated by an R&S SMT 03, was set to 148, 296 and 592 MHz for LTE10, LTE20 and 2xLTE20 mode, respectively, to maintain a constant oversampling ratio of 16.

The RX gain has been measured up to a frequency of 5 times the channel bandwidth, with the input signal generated by an R&S SMIQ 06B. Again, the RX STF follows the nominal fourth-order Butterworth roll-off very closely, as previously shown for the ADCSF stand-alone measurements in Fig. 15. The RX STF was also measured for negative frequency offset, and the difference between positive and negative frequency-offset STFs is less than 0.1 dB.

For desensitization measurements, we define $\mathrm{P_{NF,1dB}}$ as the power of the blocker for which NF rises by 1 dB, compared to its value when no blocker is present. This performance metric captures a desensitization in the ADCSF occurring mostly via an increase of the noise floor, rather than via a compression of the desired signal, particularly for IB and close OOB blocker. Thus, $\mathrm{P_{NF,1dB}}$ is a more accurate metric than the traditional small-signal 1 dB compression point $\mathrm{CP_{1dB}}$. The IB and OOB $\mathrm{P_{NF,1dB}}$ values are -45dBm and -20 dBm, respectively, for all bandwidth settings (Fig. 17). The blockers were generated by a low-phase-noise generator (R&S SMHU) to ensure that desensitization is not caused by a possibly high noise floor associated to the strong signal level of the generator. The IIP3 was measured versus frequency f_{off} with two tones placed at $f_{\mathrm{LO}} + f_{\mathrm{off}}/2 + 100$ kHz and $f_{\mathrm{LO}} + f_{\mathrm{off}}$, with results shown in Fig. 17. The IB $\mathrm{P_{NF,1dB}}$ and IIP3 are limited by the ADCSF, while OOB they are limited by the LNTA. It should be added the difference between OOB $\mathrm{P_{NF,1dB}}$ and OOB $\mathrm{CP_{1dB}}$ is very small. A blocker mask based on the blocker test cases for LTE20 discussed in Section II is added to the LTE20 data in Fig. 17, demonstrating that all test cases are fulfilled with some margin.

The RX performance versus LO frequency, with the baseband in LTE10 mode, is presented in Fig. 18. The LO frequency is increased in steps of f_s (148 MHz for LTE10), from $4f_s$ (592 MHz) to $20f_s$ (2960 MHz). The RF-to-digital gain, measured at a baseband frequency of 1 MHz, is approximately 50 dB, as expected. $\mathrm{P_{NF,1dB}}$, measured with a blocker at

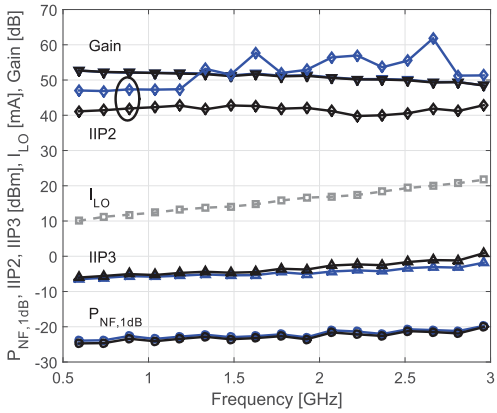

Fig. 18. RX gain, LO current consumption, IIP3 and $\mathrm{P_{NF,1dB}}$ versus LO frequency in LTE10 mode.

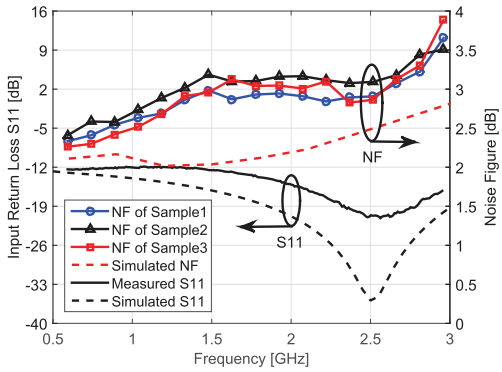

Fig. 19. RX NF and S_{11} versus LO frequency in LTE10 mode.

25 MHz, is between -24 and -20 dBm, and IIP3, measured with an f_{off} of 25 MHz, is between -6 and 0 dBm. The IIP2 is higher than 40 dBm for the worst of the two I/Q channels, with two tones place at $f_{\mathrm{LO}} + 24.9$ MHz and $f_{\mathrm{LO}} + 25$ MHz. For the other channel, IIP2 varies between 47 and 60 dBm, and similar values were observed for two RX samples.

As shown in Fig. 19, the wideband shunt-feedback LNTA achieves a good input impedance match, with an S_{11} (measured with an R&S ZVL) below -12 dB over the entire 0.6–3.0 GHz range. The notch in S_{11}, caused by the resonance of bond-wire inductance and various parasitic capacitances, is well predicted by post-layout simulations.

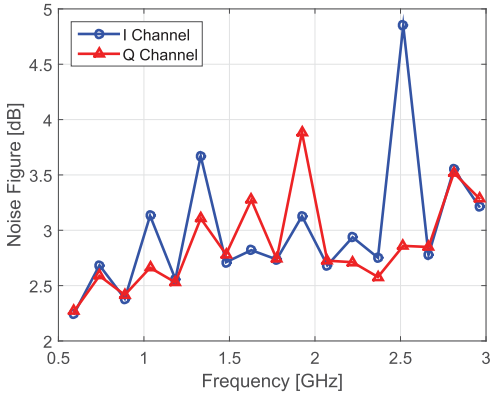

Fig. 20. RX I/Q NF versus LO frequency in LTE20 mode. The NF peaks occur when $f_{\rm LO}$ is an odd multiple of $f_s/2$.

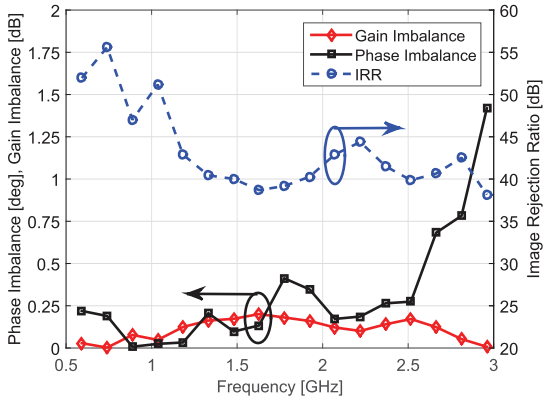

Fig. 21. I/Q gain and phase imbalance versus LO frequency, measured at 1 MHz baseband frequency.

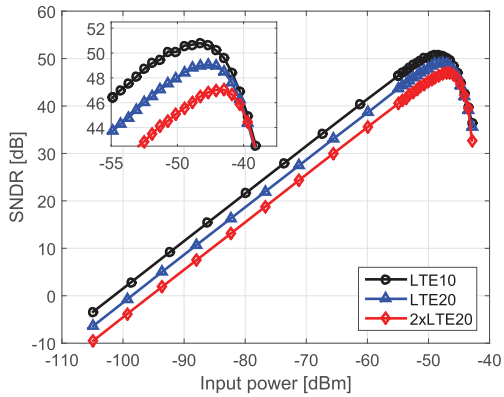

Fig. 22. RX SNDR in LTE10, LTE20, and 2xLTE20 mode, with $f_{\rm LO} = 1.776$GHz.

The RX NF was measured using the Y-factor method together with an HP 346A 5 dB ENR noise source, while the RX was in LTE10 mode. NF was measured for three samples, and the worst-case result (either from the I or the Q channel) for each sample is presented in Fig. 19, together with the simulated NF. The NF data from the three samples are very similar, the discrepancies being within the measurement accuracy, and the difference between measured and simulated NF is less than 1 dB. The maximum measured NF is below 3.2 dB up to 2.5 GHz, and not higher than 3.9 dB at 3 GHz.

Nevertheless, and unexpectedly, NF depends on the ratio between f_{LO} and f_s adopted in the actual measurements. As an example, Fig. 20 shows the NF, measured at both I and Q channels, with the RX working in LTE20 mode, where f_s is 296 MHz. The frequencies at which the NF was measured coincide with those shown in Fig. 19 for the LTE10 mode, i.e. they are integer multiples of 148 MHz (the value of f_s in LTE10). This means that each frequency step in Fig. 20 is equal to $f_s/2$ for LTE20. Clearly, every other NF value in Fig. 20 is in average 1–2 dB higher than expected, while the other values are identical to those in Fig. 19. A closer look at Fig. 20 reveals that the higher-than-expected NF data correspond to values of $f_{\rm LO}$ that are not integer multiples of f_s in LTE20 mode. It should be added directly that this behavior has been impossible to reproduce in post-layout simulations, despite the introduction of large mismatches in both quadrature mixer and feedback DACs in the ADCSFs. Nevertheless, the fact that the NF discrepancy varies greatly between I and Q channel (e.g. at $f_{\rm LO} = 2.5$ GHz the Q-channel NF displays the largest degradation, while the I-channel NF does not show any degradation at all), and in a seemingly rather random fashion, this phenomenon is most likely not caused by a first-order effect. One possible explanation emerges from the analysis of the frequency content of the ADCSF output. Due to noise shaping, the noise power spectral density at the ADCSF output reaches a maximum at $f_s/2$, but local maxima are present also at frequencies $f_s/2 + nf_s$, where n is an integer. If this noise can find its way, either on-chip or off-chip, to the mixer input, and $f_{\rm LO}$ is an odd multiple of $f_s/2$ (i.e., $f_{\rm LO} = f_s/2 + nf_s$), the strong noise at a local maximum is down-converted by the LO, deteriorating the NF.

Gain and phase imbalance between I and Q channels are displayed in Fig. 21. Measured at a baseband frequency of 1 MHz, the absolute value of phase imbalance is below 0.5° up to 2.5 GHz, increasing to 1.5° at 3 GHz, while the gain imbalance is below 0.25 dB. The image rejection ratio (IRR) calculated from these data exceeds 40 dB over almost the complete frequency range.

Finally, Fig. 22 shows that the RX SNDR is between 47 and 51 dB for the three bandwidths, when the LO is placed at a mid-band frequency of $f_{\rm LO} = 1.776$ GHz. Measurements were taken with an input tone placed at $f_{\rm LO} + 100$ kHz, to make sure that the most important harmonics produced by the ADCSF fall in-band. The measured SNDR for all bandwidth settings versus LO varies between 45 and 52 dB.

The RX is compared to other DSM-based RXs in Table III. With respect to [9], we achieve a lower NF at a lower power consumption. Furthermore, [9] uses a high $r_{\rm CSF}$ of 2.1 (compared to our $r_{\rm CSF}$ of 1.36), which means that the first adjacent channel is not filtered at all. To summarize, we achieve the widest carrier bandwidth with a good linearity and the lowest NF and power consumption, at a comparable RX frequency range.

TABLE III
PERFORMANCE OF THE RX COMPARED TO OTHER DSM-BASED RXS

	Type	RF Freq. [GHz]	NF [dB]	Power [mW]	Supply [V]	IIP3 [dBm]	SNDR [dB]	RF Carrier BW [MHz]	Area [mm^2]	Process [nm]
This work	**RX with $\Delta\Sigma$-CSF**	**0.6–3**	**2.4–3.5**	**35.5–53.0**	**1.2**	**-6–0**	**45–52**	**10, 20, 40**	**0.7**	**65**
[9]	Direct $\Delta\Sigma$ RX	0.7–2.7	5.9–8.8	90	1.1	-2	40–43	1.4, 15	1	40
[10]	Direct $\Delta\Sigma$ RX	0.4–4	16	17–70.5	1.5/1.2	+13.5	52-68	4, 10	0.56	65
[11]	RX with filtering A/D	0.04–1	2.7–3.5*	221.4	1.8/1	-13	–	5, 6, 7, 8	5.6**	80

*Estimated,
**Incl. PLL and DSP.

VII. CONCLUSION

This paper has presented a wideband RX where an ADCSF incorporates the functionalities of TIA, CSF and A/D conversion, increasing the overall power efficiency. A systematic design approach has been demonstrated to achieve the target performance. With an aggressive fourth-order filtering, the ADCSF achieves a high linearity. The RX supports operation over a wide frequency range, with a low noise figure and a good linearity at a competitive power consumption.

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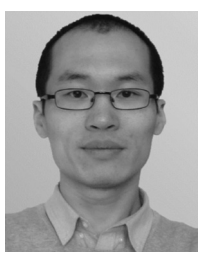

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