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Asymmetric Multi-Level Inverter

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***Abstract*— This paper proposes a multi-level inverter (MLI) which has two or more unequal DC voltage source with lesser number of components. The proposed MLI composed of many basic DC source units, where each basic DC source unit are stacked in series to get higher voltage levels. The proposed topology of MLI is derived from a basic MLI cascaded H-bridge inverter. The designed AMLI is capable of handling negative current and hence capable of operating in all 4 quadrants due to absence of components like diode which is seen in the proposed topology, the phase opposition disposition PWM technique is used to trigger the switches. By utilizing three different DC voltage source as input to AMLI, we get an output waveform in staircase form of 15 level. The THD of output staircase waveform is 8.25% in which it has majority of higher harmonics distortion, by using LCL filter the THD of 0.1% can be achieved. The work is carried out on MATLAB / SIMULINK 2020Ra.**

Keywords—multi-level inverter, components, phase opposition disposition AMLI, PWM, THD

I. INTRODUCTION

The demand of energy is increasing rapidly and the renewable energy is getting more popular day by day. The photovoltaic is one of rapidly growing energy because of, most affordable, accessible, and prevalent. Today, most solar panels are between 15% and 20% efficiency only, and this 15%-20% energy need to converted into electrical standards for utility utilization, converter losses are mainly due to higher values of input current and output voltage. So to get maximum possible energy from renewables like solar cells, it is necessary to design a most possible efficient converters [1].

As greenhouse gas emission covers the Earth, the heat of the sun is trapped. Climate change and global warming are the results of this action. The Earth is currently warming at a rate that has never been seen before. In the recent years the production of renewable energy sources such as photovoltaic power systems, wind energy and other is steadily expanding. PV systems, on the other hand, become the most demanding in RES because to their clean functioning [2]. Because the energy provided by RES is still insufficient in comparison to fossil fuels so we can't handle high energy losses so an efficient energy converter is required. The resect literatures shows the MLI are efficient power converters [3,4]. However efforts have been made in this project to design and simulate AMLI of 15 level inverter using three batteries of 1:2:4 ratios as voltage sources [5].

Multilevel inverters have got a lot of attention from the academic and industry areas. Multilevel inverters approaches not only increase the converter's output power quality, but they also In power electronic converters, allow for higher amounts of voltage and power. Using commercially available low-medium voltage semiconductor switches, higher power levels can be achieved [6]. The switches are connected in serial it is required to make a high power converter utilizing typical 2-level converters. Multilevel converters have numerous uses [7], including UPS systems, hybrid photovoltaic-UPS systems, traction, ships, renewable systems, drive, and power quality. Despite their unique characteristics, multilevel inverters typically employ a large number of switches, due to this losses and cost of the inverter increases. The required control is also complex. Multilevel converters can be divided into four categories based on the number of voltage sources and their voltage levels: asymmetrical, symmetrical, hybrid, and single DC source multilevel converters. Multilevel symmetric and single DC source inverters such as neutral point diode clamped (NPDC), cascaded H-bridge (CHB), and flying capacitor (FC) inverters are examples of traditional multilevel inverters [8]. In literatures the proposed topologies are typically derivations or combinations of these old converters. These converters are made up of basic units, and the output voltage levels of the converter are enhanced by connecting these units in series.

The proposed asymmetrical multilevel inverter allows the use of DC voltage sources with varying voltage magnitude. The suggested inverter has a substantially lower switch count and a significantly bigger number of output voltage levels. Multilevel inverters outperform single-level inverters due to higher power quality, reduced THD and a fewer switching losses.

This converter is designed for high-power applications such as solar power plant. and also for applications where high quality power is needed like grid connected inverter (GCI) [9], hospitals and industries.

II. PROPOSED TOPOLOGY

The topology of proposed inverter is a improvement over the inverter proposed [5], The topology is divided into two units which are shown in Fig.1, The first unit near the source side consists of basic units connected in series and the second unit, on load side, consists of H-bridge to provide alternative output voltages.

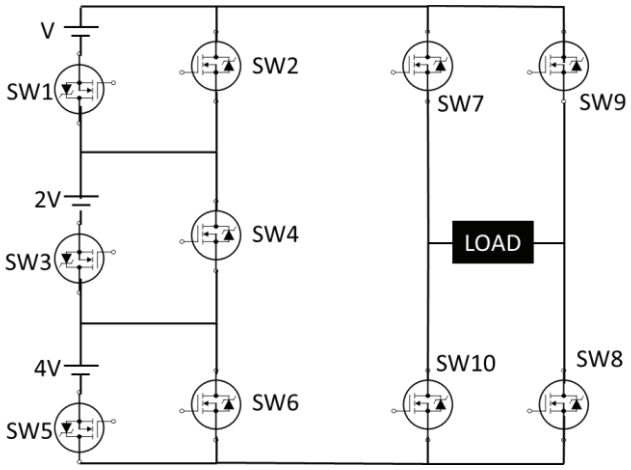

Fig. 1. Proposed single-phase 15 level AMLI.

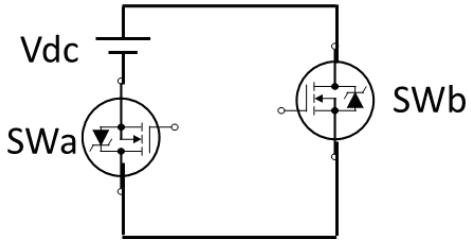

Fig. 2. Basic unit of proposed topology.

The basic unit shown in Fig.2 consists of a DC source and two switches, SWa and SWb. Switch SWa is connected in series with the DC source and SWb is connected anti-parallel across switch SWa and DC source. Each basic unit has different DC voltage source and the switches are selected accordingly. These basic units are connected in series, if we consider the top basic unit as 1^{st} unit and bottom most basic unit as nth unit, then the magnitude of DC voltage sources used are of order 1:2:4:8:16: … :$2^{(n+1)}$-1. The designed simulation consists of only three basic units so the DC voltage sources used are of ratio 1:2:4.

The proposed topology is analyzed and the power switching conditions for the Fig.1 circuit is obtained where we can obtain fifteen different voltage level output are tabulated in Table.1.

TABLE I. SWITCHING STATES OF PROPOSED TOPOLOGY.

No. of Level	Voltage Level	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1
1	7V	0	0	1	1	0	1	0	1	0	1
2	6V	0	0	1	1	0	1	0	1	1	0
3	5V	0	0	1	1	0	1	1	0	0	1
4	4V	0	0	1	1	0	1	1	0	1	0
5	3V	0	0	1	1	1	0	0	1	0	1
6	2V	0	0	1	1	1	0	0	1	1	0
7	V	0	0	1	1	1	0	1	0	0	1
8	Zero	0	1	0	1	1	0	1	0	1	0
9	-V	1	1	0	0	1	0	1	0	0	1
10	-2V	1	1	0	0	1	0	0	1	1	0
11	-3V	1	1	0	0	1	0	0	1	0	1
12	-4V	1	1	0	0	0	1	1	0	1	0
13	-5V	1	1	0	0	0	1	1	0	0	1
14	-6V	1	1	0	0	0	1	0	1	1	0
15	-7V	1	1	0	0	0	1	0	1	0	1

In general, the number of output voltages and the number of power semiconductor switches used in the proposed topology is represented as follows.

- Number of switches required = 2n+4
- Number of output voltage levels = $2^{(n+1)}$-1

Where n represents the number of DC voltage sources used in the proposed AMLI.

III. WORKING AND MODES OF OPERATION.

Whenever the switch SWa in the basic unit conducts, it will add the DC voltage source in that basic unit to the topology and whenever the switch SWb conducts it bypass the DC voltage source. We have to make sure both SWa and SWb does not conduct at the same time. By using the three basic units which has a DC voltage source of ratio 1:2:4 respectively, we can generate maximum peak voltage of $7V_{dc}$ on load. H-bridge is used to get alternative positive and negative voltages across the load.

There are 15 modes of operation of the proposed inverter to obtain 15 different voltages levels, they are illustrated in Fig.3 to Fig.17 below. The switches used in the topology are MOSFET's since MOSFET's are symmetrical in structure it allows current to flow in the both the directions, hence we can use RL load also where we get negative current. By using MOSFET's in this fashion we can make the inverter works in all 4 quadrants.

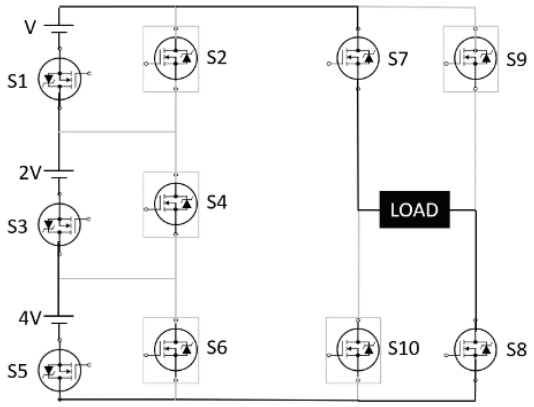

Fig. 3. Mode 1, Vo = 7V

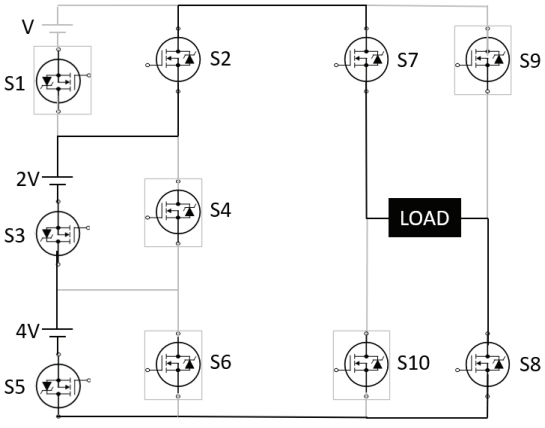

Fig. 4. Mode 2, Vo = 6V

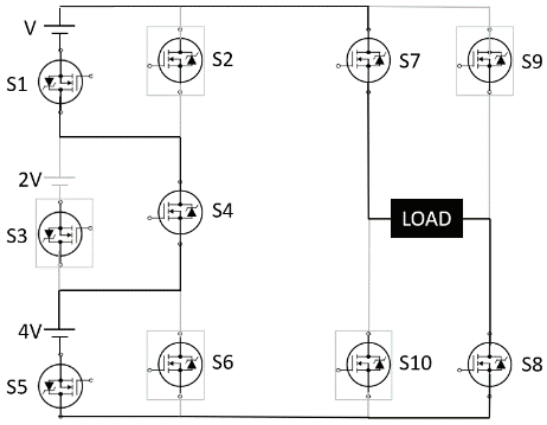

Fig. 5. Mode 3, Vo = 5V

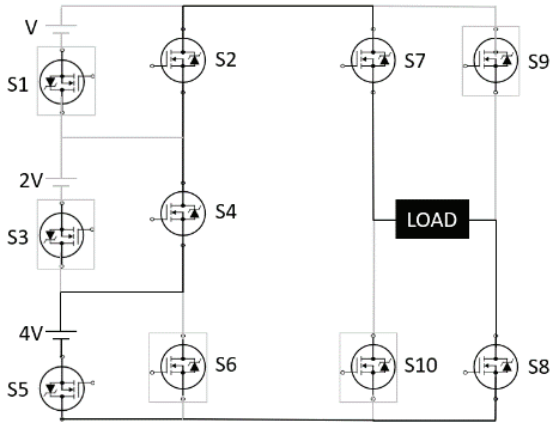

Fig. 6. Mode 4, Vo = 4V

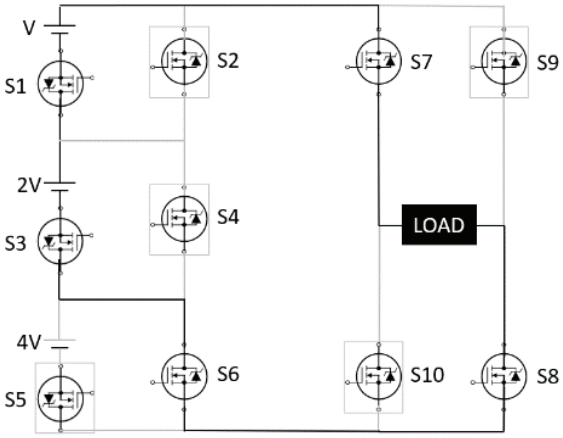

Fig. 7. Mode 5, Vo = 3V

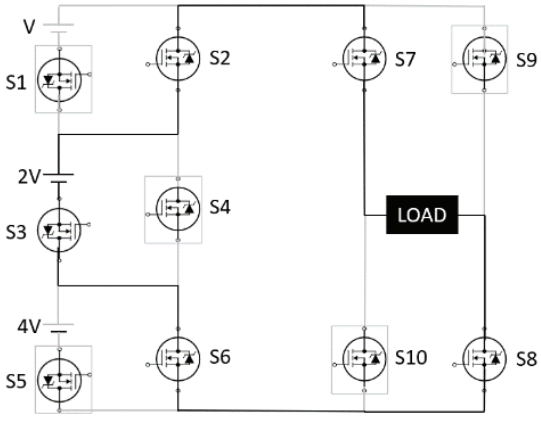

Fig. 8. Mode 6, Vo = 2V

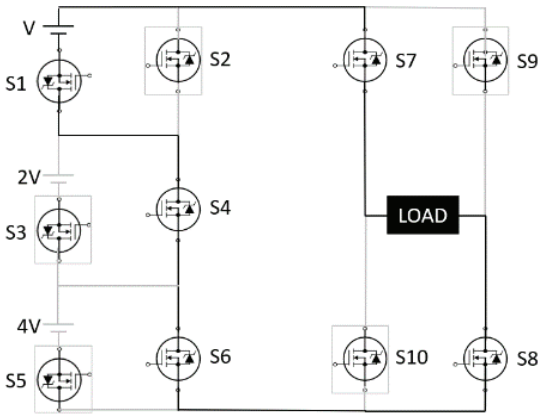

Fig. 9. Mode 7, Vo = 1V

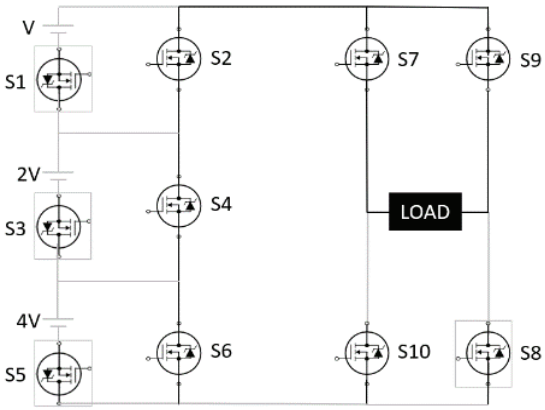

Fig. 10. Mode 8, Vo = 0V

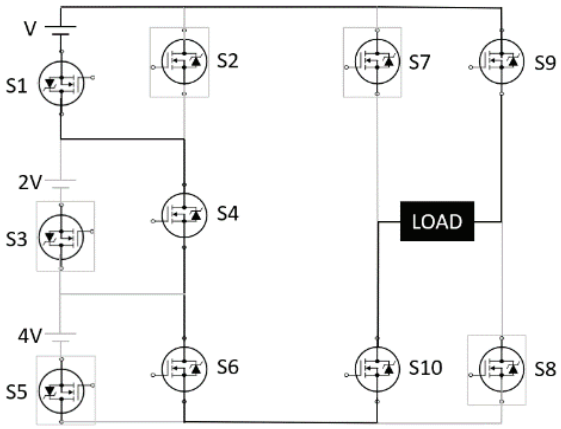

Fig. 11. Mode 9, Vo = -1V

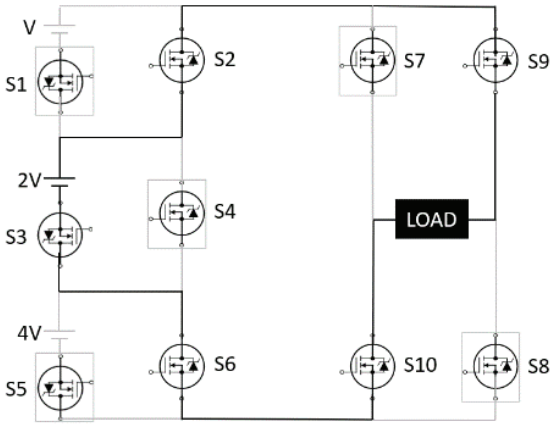

Fig. 12. Mode 10, Vo = -2V

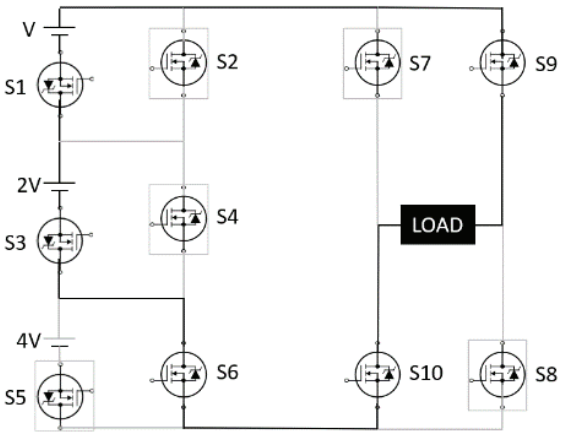

Fig. 13. Mode 11, Vo = -3V

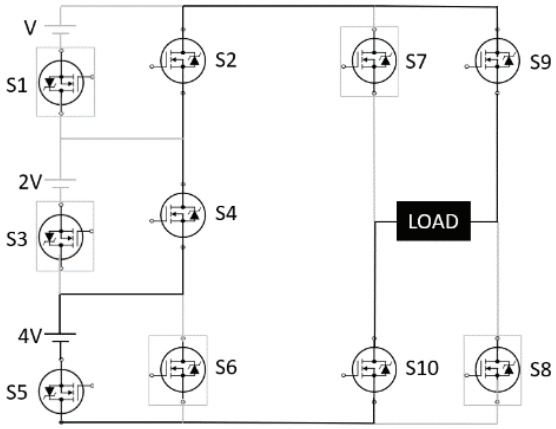

Fig. 14. Mode 12, Vo = -4V

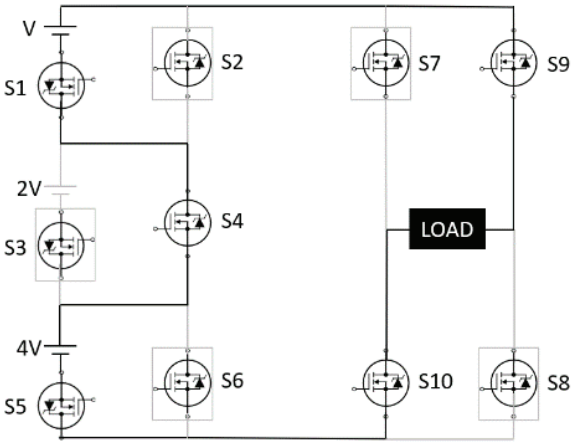

Fig. 15. Mode 13, Vo = -5V

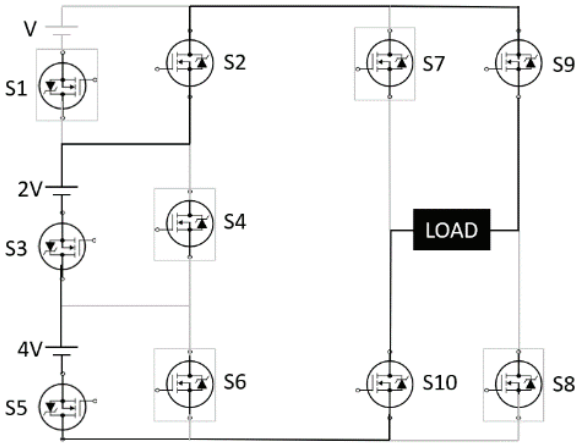

Fig. 16. Mode 14, Vo = -6V

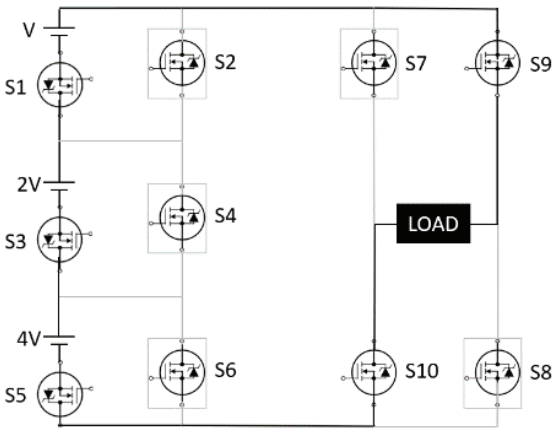

Fig. 17. Mode 15, Vo = -7V

IV. PWM TECHNIQUES

The level shifted PWM technique suits for the proposed topology. The triggering signals of a proposed AMLI is configured by utilizing a sine wave reference control signal and fourteen carrier triangular wave signals of equal frequency and amplitude. The signals are generated based on the comparison between the vertically shifted triangular carrier signals and sinusoidal reference control signal is as shown in Fig.18.

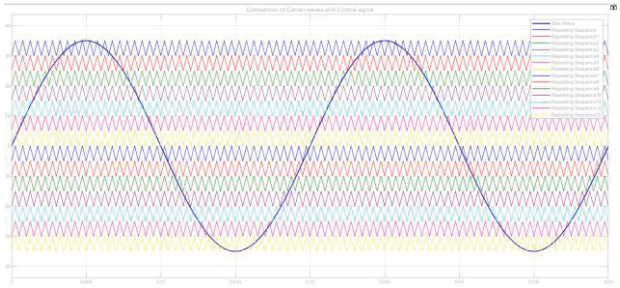

Fig. 18. Comparison of carrier signals and control signal.

The above explained PWM techniques can be differentiated based on carrier wave signals [10] as Phase Disposition (PD), Alternate Phase Opposition Disposition (APOD) and Phase Opposition Disposition (POD). N level Multi-level inverters typically use N-1 carrier waves. Each method has its own sets of drawbacks and benefits. The carrier waves in the PD technique as shown Fig.19 are all in phase, the carrier waves below and above the zero point are out of phase in the POD technique shown in Fig.20 and the carrier waves in the APOD technique shown in Fig.21 are 180 degrees phase displaced from top to bottom alternatively.

- PD Technique: The +ve and -ve sides of the output voltages are asymmetrical.

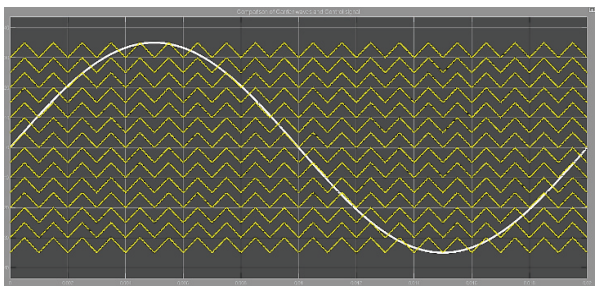

Fig. 19. PD technique of PWM generation

- POD Technique: The +ve and -ve sides of the output voltages are symmetrical.

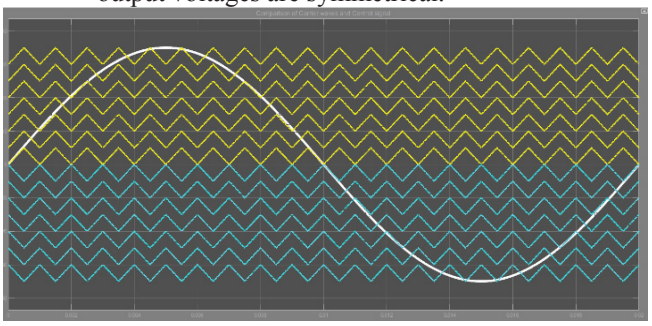

Fig. 20. POD technique of PWM generation

- APOD Technique: The +ve and -ve sides of the output voltages are symmetrical.

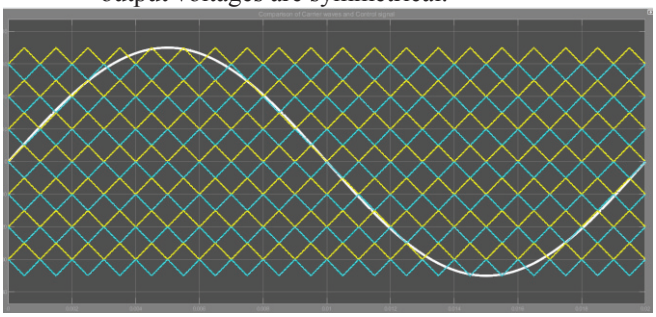

Fig. 21. APOD technique of PWM generation

In this paper, fourteen triangular signals each with a frequency of 1 kHz are level shifted such that they do not overlap, and these signals are utilized as carrier signals. The desired triggering pulses for all switches in MLI is obtained by level shifted triangular carrier waves compared to a pure sine wave with reference amplitude (Vsin) where Vtri is the amplitude of the carrier wave, which is defined as the peak to peak value. The amplitude of sine wave is converted into switching time which is shown in Fig.22 to Fig.29.

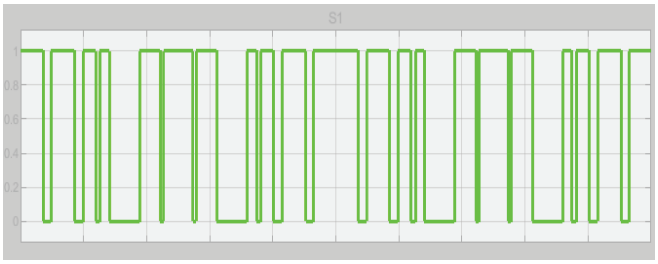

Fig. 22. Switching pattern for switch S1

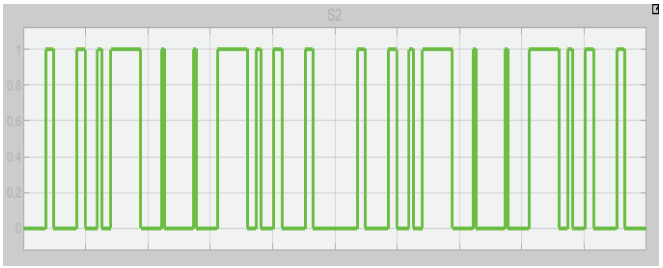

Fig. 23. Switching pattern for switch S2

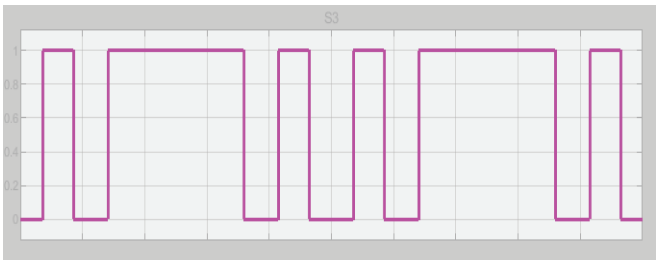

Fig. 24. Switching pattern for switch S3

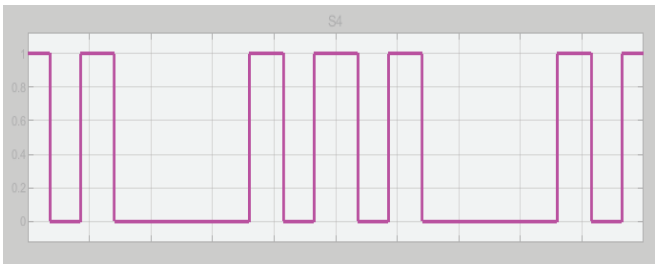

Fig. 25. Switching pattern for switch S4

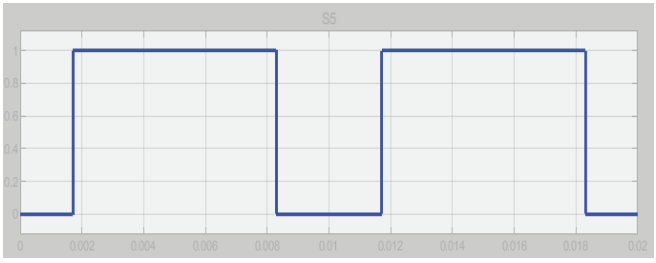

Fig. 26. Switching pattern for switch S5

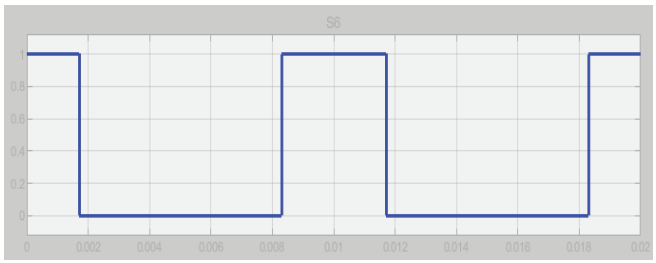

Fig. 27. Switching pattern for switch S6

Fig. 28. Switching pattern for switch S7 & S8

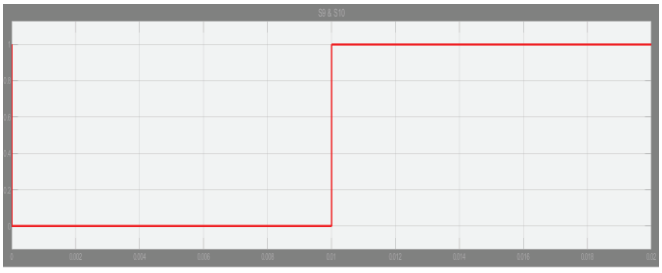

Fig. 29. Switching pattern for switch S9 & S10

V. SIMULATION & RESULTS

The asymmetrical multi-level inverter consist of three asymmetrical DC voltage sources, an H-bridge and a RL load as shown in figure 30. Three switches, S1, S3, and S5, control the three asymmetrical voltage sources. To the DC source and switch combination, the switches S2, S4, and S6 are connected in anti-parallel.

The proposed topology's simulation is shown below, and it consists of a gating signal in which the sine wave is compared to a level shifted triangular waveforms, which is known as the Phase Disposition approach. Individual switch switching patterns are depicted in the Fig.22 to Fig.29. The signals are delivered to switches S5, S3, and S1. The complement signals of switches S5, S3, and S1 are given to switches S6, S4, and S2, respectively, according to switching state table.1 indicates. The switches S7 and S9 are conducting in the opposite direction. During the positive half of the cycle switches S7 and S8 turn ON. During the negative half of the cycle switches S9 and S10 turn ON.

The output from inverter is stepped waveform, it consists of high order harmonics, to reduce the harmonics a LCL filter is used to get smooth output waveform. Which gets further smoothened by using LCL filter.

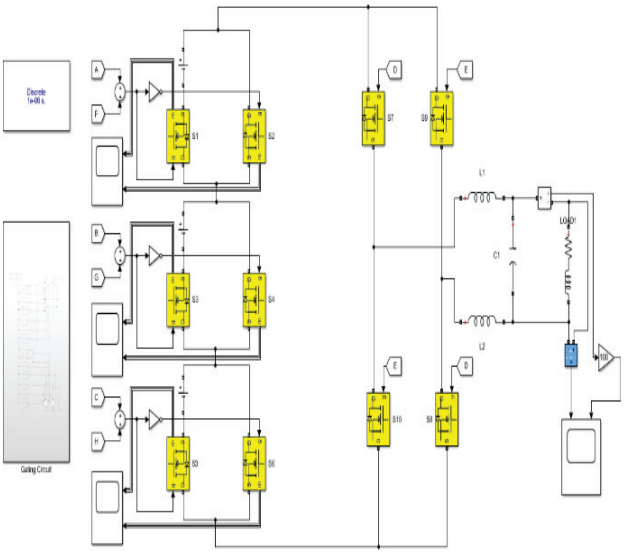

Fig. 30. Simulation of AMLI

The output voltage of 350V AC peak-peak voltage of 15 level and 50 Hz frequency is obtained at the output without LCL filter as shown in Fig 31, the output without filter is having higher order harmonics is shown in Fig.32which is further reduced by using LCL filter to achieve smooth output waveform as shown in Fig.19

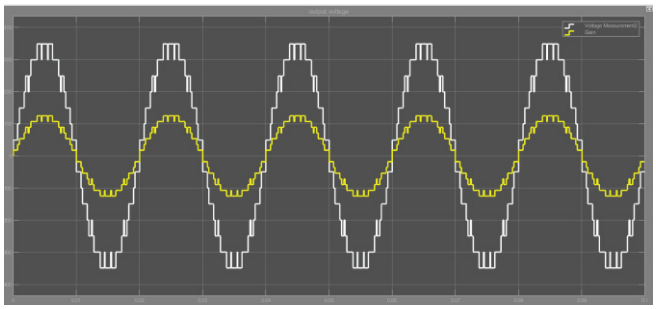

Fig. 31. Output of inverter without filter.

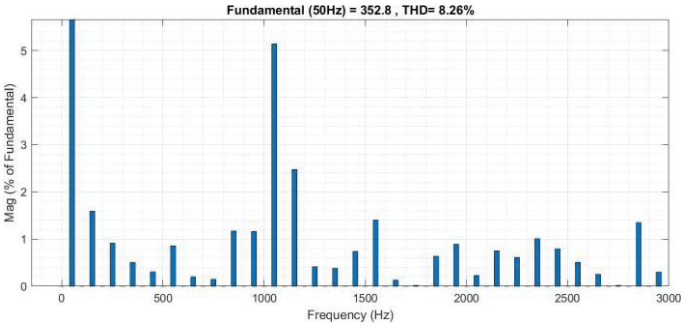

Fig. 32. THD analysis of waveform without filter.

Fig.32 shows a output wave form of proposed inverter from MATLAB platform, this output is of voltage 325V AC peak to peak of 50Hz. That meets 230V RMS standard waveform. The LCL filter is used to get smooth output waveform.

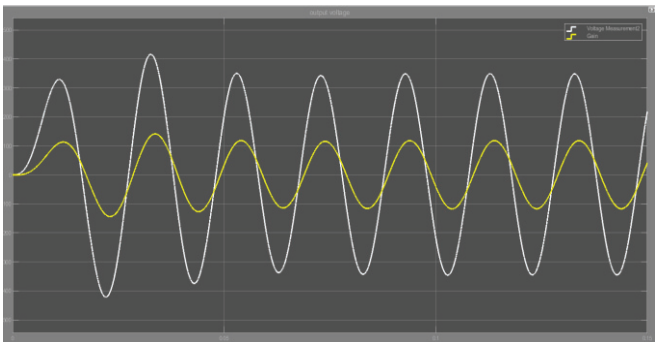

Fig. 33. Output of inverter with filter.

The THD analysis of the final output waveform with filter as been obtained with the voltage magnitude of fundamental waveform of 50Hz is 323.5 volts, resulted in THD of 0.1% as shown in Fig.34.

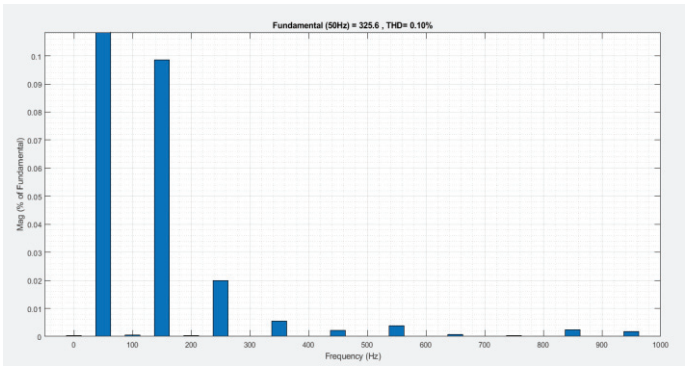

Fig. 34. THD Analysis of waveform with filter.

TABLE II. COMPARISON OF SOME 15 LEVEL MULTI-LEVEL INVERTERS WITH A PROPOSED TOPOLOGY IN THIS PAPER.

Paper → Difference □	Proposed Topology in paper [3]	Proposed Topology in paper [5]	Proposed Topology
MOSFET used	18	7	10
Diodes used	4	3	0
Number of quadrants working	2 Quadrants operation	2 Quadrants operation	4 Quadrants operation
THD (without filter)	7.38%	5.6%	8.25% (majority of higher order harmonics.)

The above table.2 shows a comparison of two other multi-level inverters of 15 level inverters with our proposed 15 level AMLI. The proposed inverter is having 10 MOSFET's and zero diodes due to this condition the inverter works in all the 4 quadrants, The proposed inverter is having highest THD than other two inverters this is due to presence of higher order harmonics which can be easily mitigated further using filters.

VI. CONCLUSION

A new topology of asymmetric multilevel inverter was proposed in this paper. The three asymmetrical inputs from the DC voltage sources 50V, 100V, and 200V are applied as the input of the multilevel inverter. The main emphasis is to handle negative currents use to inductive loads and diodes are eliminated hence contribute to the lesser number of components and also leads to 4 quadrant operation, Only ten switches were used in this MLI, which eliminated the need for clamping diodes and capacitors. The proposed converter's design has been successfully built and presented in MATLAB, with the simulated results showing a close match to the optimal output required. If the load is just resistive, the multilevel inverter transforms 350V DC to 350V AC peak to peak. With a designed LCL filter and RL (280ohm and 200mH) load the multilevel inverter transforms 350V DC to 230V RMS AC output. This multi-level inverter has a full load current rating of 8A and operates in the 230V RMS AC voltage range and obtained THD of 0.1% was achieved.

REFERENCES

[1] Cathrine E. S. Feloups, Ahmed I. M. Ali, Essam E. M. Mohamed, "Single-Phase Seven-Level PWM Inverter for PV Systems Employing Multi-level Boost Converter", IEEE- 17632965, Conference Paper, 10.1109/ITCE.2018.8316658 , 15 March 2018.

[2] Saeed Yousofi-Darmian, S. Masoud Barakati, "A New Asymmetric Multilevel Inverter With Reduced Number of Components", IEEE-20115077, Vol: 8, Issue: 4, pp. 4333 - 4342, Dec. 2019.

[3] P. Vimala, S. Jaisiva, T. Gokulapriya "Design of Multilevel Inverter Topology for Cascaded Voltage Source Architectures", Conference Paper, 10.1109/ICSCAN53069.2021.9526344, 06 September 2021.

[4] E. Babaei, S. Alilu and S. Laali, "A new general topology for cascaded multilevel inverters with reduced number of components based on developed H-bridge," IEEE Trans. Ind. Electron., vol. 61, no. 8, pp. 3932–3939,Aug. 2014.

[5] Ravi Kumar V , Sanjay N, "Design and Development of Asymmetrical MultiLevel Inverter for solar energy" ICEECCOT 14-15, dec 2018.

[6] Erfan Hallaji, Ossein Madadi Kojabadi, "Novel switched-capacitor-based multilevel inverter topology for renewable energy" PEDSTC, 78-1-6654-0366-5/20/$31.00, IEEE, 2021.

[7] Kaushik Kushalappa Naik, Dr.Venugopal N, "1kW Home Inverter using cascaded Current Fed Push Pull Converter and SPWM Inverter", IEEE – 43488, 9th ICCCNT 2018 July 10-12, 2018, IISC, Bengaluru.

[8] T. Sunitha, K. Udhayakumar, T. Annamalai, C. Gopinath, "A New 23 Level Cascaded Multi-Level Inverter with Optimum Structure", IEEE- 18043468, Conference Paper, 23 August 2018.

[9] Wooyoung Choi, Bulent Sarlioglu, " Comparative Analysis on Performance of Power Quality Improvement of Grid-Connected Inverters", IEEE-19192476, Conference Paper, 10.1109/ECCE.2019.8912488, 28 November 2019.

[10] K. Leela Madhav, Challa Babu, P. Ponnambalam, Ashutos Mahapatra, "Fuzzy Logic Controller for Nine Level Multi-Level Inverter with Reduced Number of Switches", International Conference on Innovations in Power and Advanced Computing Technologies, 10.1109/IPACT.2017.8244938, 21-22 April 2017.